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Team Nexperia

74LVT16652A

3.3 V 16-bit bus transceiver/register; 3-state

Rev. 03 — 12 January 2005 Product data sheet

1. General description

The 74LVT16652A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output enable (OEAB and $\overline{OE}$BA) inputs are provided to control the transceiver functions. Select control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A LOW input level selects real-time data, and a HIGH input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by LOW-to-HIGH transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select control or output enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OE}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high- impedance, each set of bus lines remains at its last level configuration.

2. Features

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

PHILIPS

3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	-	2.1	-	ns
t_{PHL}	propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	-	2.4	-	ns
C_I	input capacitance control pins	V_I = 0 V or 3.0 V	-	3	-	pF
$C_{I/O}$	I/O pin capacitance	outputs disabled; V_I = 0 V or 3.0 V	-	9	-	pF
I_{CC}	quiescent supply current	outputs disabled; V_{CC} = 3.6 V	-	70	-	µA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16652ADGG	–40 °C to +85°C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
74LVT16652ADL	–40 °C to +85°C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1

5. Functional diagram

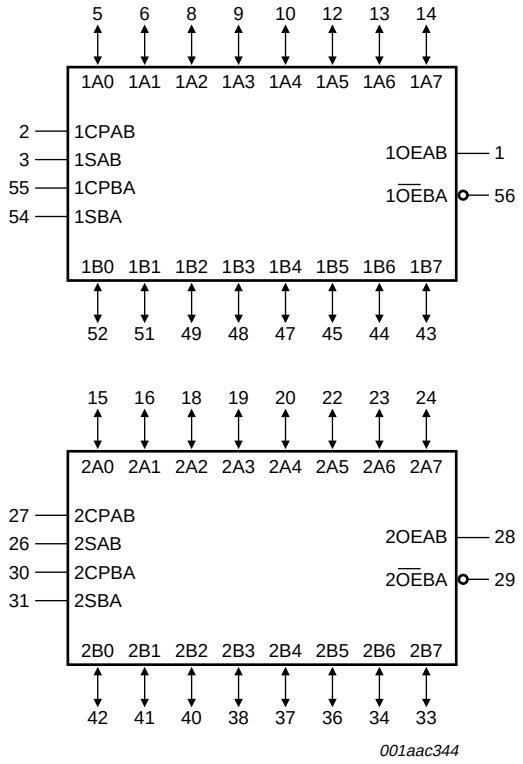


Fig 1. Logic symbol

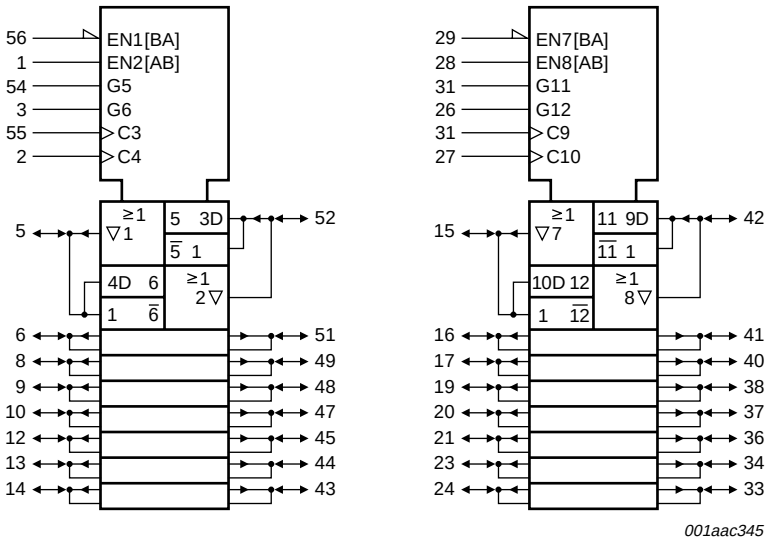


Fig 2. IEC Logic symbol

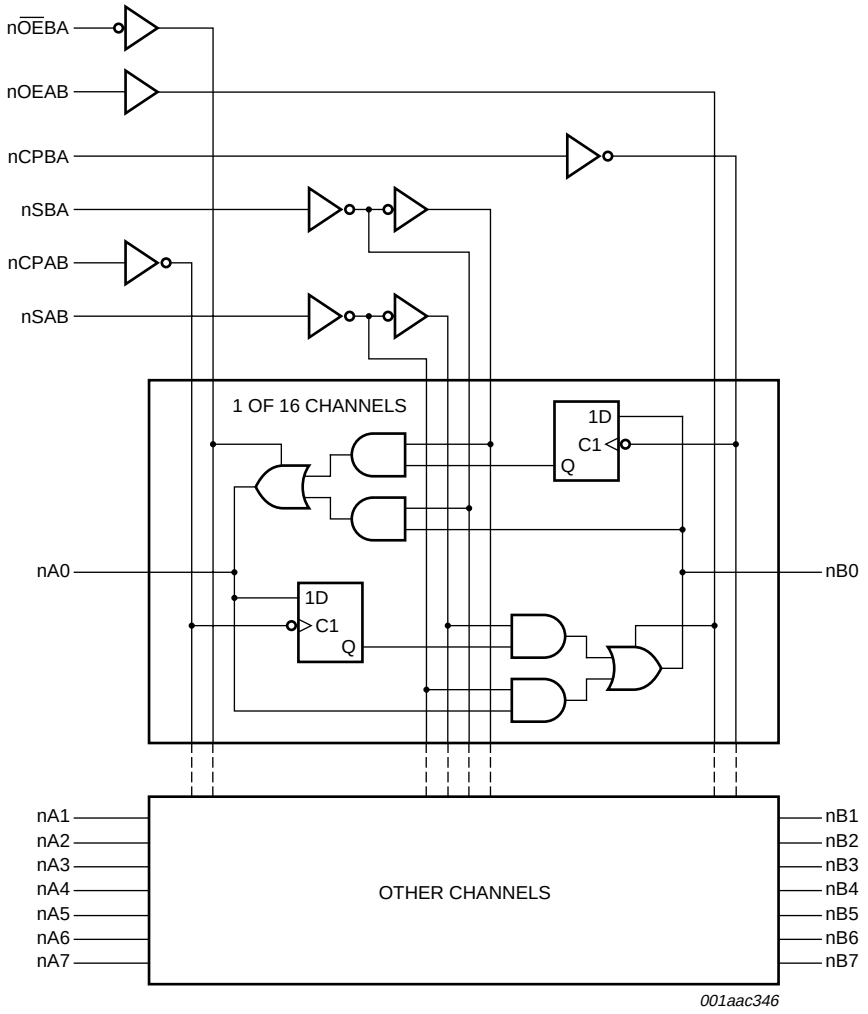


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

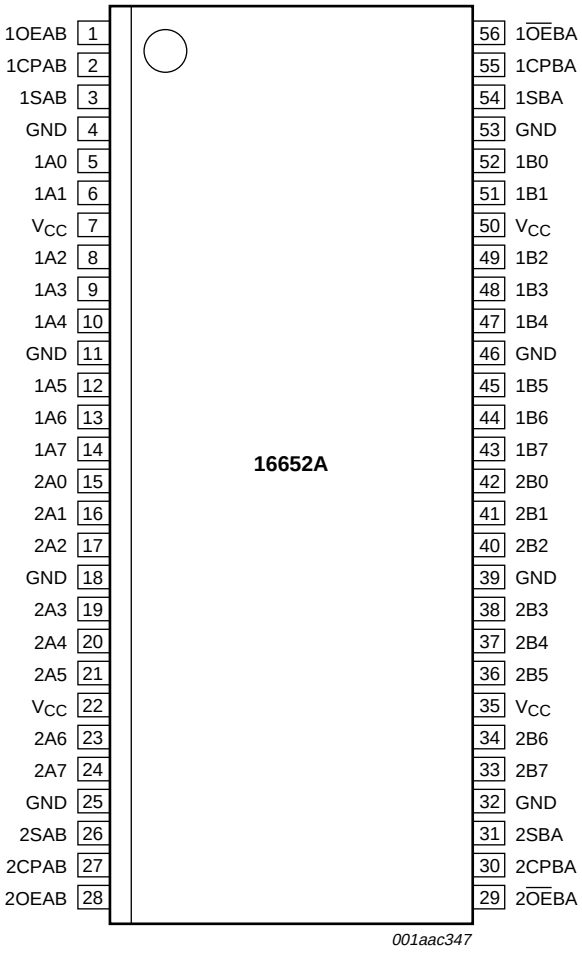


Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1OEAB	1	A to B output enable input
1CPAB	2	A to B clock input
1SAB	3	A to B select input
GND	4	ground (0 V)
1A0	5	data input or output (A-side)
1A1	6	data input or output (A-side)
V_{CC}	7	supply voltage
1A2	8	data input or output (A-side)

Table 3: Pin description *...continued*

Symbol	Pin	Description
1A3	9	data input or output (A-side)
1A4	10	data input or output (A-side)
GND	11	ground (0 V)
1A5	12	data input or output (A-side)
1A6	13	data input or output (A-side)
1A7	14	data input or output (A-side)
2A0	15	data input or output (A-side)
2A1	16	data input or output (A-side)
2A2	17	data input or output (A-side)
GND	18	ground (0 V)
2A3	19	data input or output (A-side)
2A4	20	data input or output (A-side)
2A5	21	data input or output (A-side)
V_{CC}	22	positive supply voltage
2A6	23	data input or output (A-side)
2A7	24	data input or output (A-side)
GND	25	ground (0 V)
2SAB	26	A to B select input
2CPAB	27	A to B clock input
2OEAB	28	A to B output enable input
$2\overline{OE}BA$	29	B to A output enable input
2CPBA	30	B to A clock input
2SBA	31	B to A select input
GND	32	ground (0 V)
2B7	33	data input or output (B-side)
2B6	34	data input or output (B-side)
V_{CC}	35	supply voltage
2B5	36	data input or output (B-side)
2B4	37	data input or output (B-side)
2B3	38	data input or output (B-side)
GND	39	ground (0 V)
2B2	40	data input or output (B-side)
2B1	41	data input or output (B-side)
2B0	42	data input or output (B-side)
1B7	43	data input or output (B-side)
1B6	44	data input or output (B-side)
1B5	45	data input or output (B-side)
GND	46	ground (0 V)
1B4	47	data input or output (B-side)
1B3	48	data input or output (B-side)
1B2	49	data input or output (B-side)

Table 3: Pin description *...continued*

Symbol	Pin	Description
V_{CC}	50	supply voltage
1B1	51	data input or output (B-side)
1B0	52	data input or output (B-side)
GND	53	ground (0 V)
1SBA	54	B to A select input
1CPBA	55	B to A clock input
$1\overline{OE}BA$	56	B to A output enable input

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input						Data I/O	
	nOEAB	$n\overline{OE}BA$	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx
Isolation	L	H	H or L	H or L	X	X	input	input
Store A and B data	L	H	↑	↑	X	X	input	input
Store A, hold B	X	H	↑	H or L	X	X	input	unspecified output [2]
Store A in both registers	H	H	↑	↑	[3]	X	input	unspecified output [2]
Hold A, store B	L	X	H or L	↑	X	X	unspecified output [2]	input
Store B in both registers	L	L	↑	↑	X	[3]	unspecified output [2]	input
Real-time B data to A bus	L	L	X	X	X	L	output	input
Store B data to A bus	L	L	X	H or L	X	H	output	input
Real-time A data to B bus	H	H	X	X	L	X	input	output
Store A data to B bus	H	H	H or L	X	H	X	input	output
Stored A data to B bus and stored B data to A bus	H	L	H or L	H or L	H	H	output	output

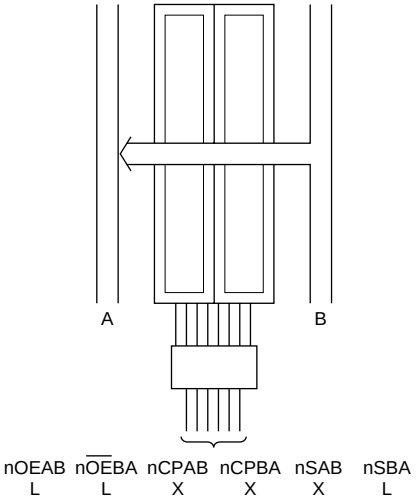
[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition.

[2] The data output function may be enabled or disabled by various signals at the $n\overline{OE}BA$ and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

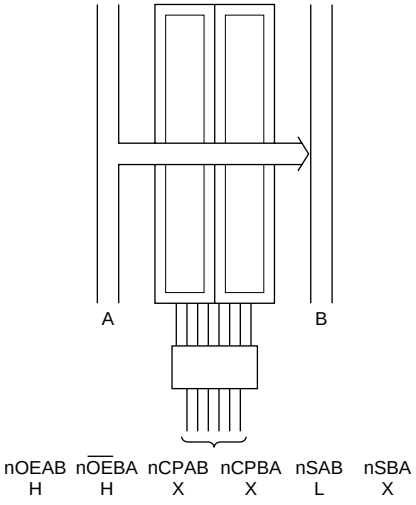
[3] If both select controls (nSAB and nSBA) are LOW, then clocks can occur simultaneously. If either select control is HIGH, the clocks must be staggered in order to load both registers.

7.2 Bus management function

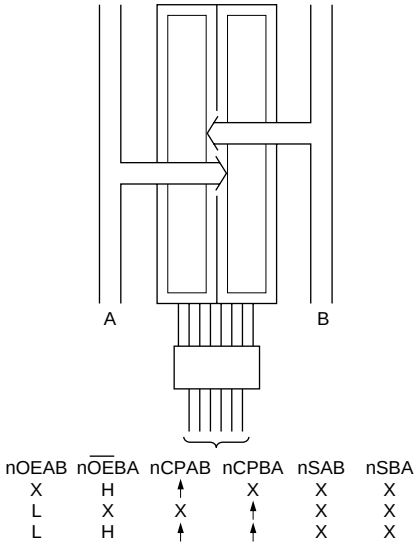
Figure 5 demonstrates the four fundamental bus management functions that can be performed with the 74LVT16652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.



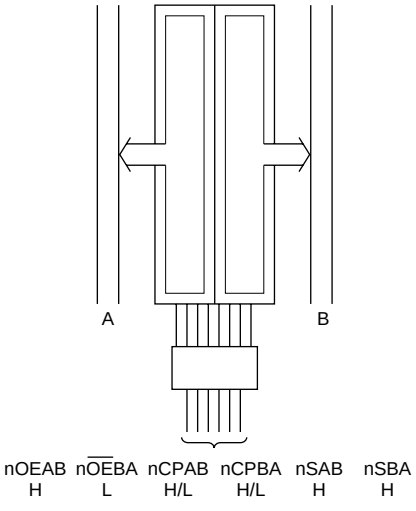
a. Real-time bus transfer bus B to bus A



b. Real-time bus transfer bus A to bus B



c. Storage from bus A only, bus B only, or bus A plus bus B



d. Transfer stored data to bus A or bus B

Fig 5. Example of bus management functions

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	DC supply voltage			–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$ V		–50	-	mA
V_I	DC input voltage		[2]	–0.5	+7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V		–50	-	mA
V_O	DC output voltage	output in OFF or HIGH-state	[2]	–0.5	+7.0	V
I_O	DC output current	output in LOW-state		-	128	mA
		output in HIGH-state		–64	-	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[1]	-	150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current		-	-	32	mA
		duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature		–40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
V_{IK}	input clamp voltage	V_{CC} = 2.7 V; I_{IK} = −18 mA		-	−0.85	−1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = −100 µA		V_{CC} − 0.2	V_{CC}	-	V
		V_{CC} = 2.7 V; I_{OH} = −8 mA		2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = −32 mA		2.0	2.3	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA		-	0.07	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA		-	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA		-	0.4	0.55	V
V_{RST}	power-up output low voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}	[2]	-	0.11	0.55	V
I_{LI}	input leakage current						
	control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.1	10	µA
	I/O data pins	V_{CC} = 3.6 V; V_I = 5.5 V	[3]	-	0.1	20	µA
		V_{CC} = 3.6 V; V_I = V_{CC}	[3]	-	0.1	10	µA
		V_{CC} = 3.6 V; V_I = 0 V	[3]	-	+0.1	−5	µA
I_{OFF}	output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA
I_{HOLD}	bus-hold current A or B outputs	V_{CC} = 3 V; V_I = 0.8 V	[4]	75	135	-	µA
		V_{CC} = 3 V; V_I = 2.0 V	[4]	−75	−140	-	µA
		V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	[4]	±500	-	-	µA
I_{EX}	current into an output in the HIGH-state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 3.0 V		-	45	125	µA
I_{PU}, I_{PD}	power-up or down 3-state output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; pins nOEAB and $n\overline{OE}BA$ are don't care	[5]	-	35	±100	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC} and I_O = 0 A					
	outputs HIGH			-	0.07	0.12	mA
	outputs LOW		[6]	-	4.9	6	mA
	outputs disabled		[7]	-	0.07	0.12	mA

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{CC}	additional supply current per input pin	V_{CC} = 3.3 V ± 0.3 V; one input at V_{CC} − 0.6 V; other inputs at V_{CC} or GND	[8]	-	0.1	0.2	mA
C_I	input capacitance control pins	V_I = 0 V or 3.0 V		-	3	-	pF
$C_{I/O}$	I/O pin capacitance	outputs disabled; V_I = 0 V or 3.0 V		-	9	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus-hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[6] I_{CC} is measured with 16 outputs LOW.

[7] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[8] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; test circuit see Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
f_{max}	maximum clock frequency	V_{CC} = 2.7 V or 3.3 V ± 0.3 V; see Figure 6	150	180	-	MHz
t_{PLH}	propagation delay nAx to nBx or nBx to nAx	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	0.5	2.1	3.4	ns
		V_{CC} = 2.7 V	-	-	3.9	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.5	4.2	ns
		V_{CC} = 2.7 V	-	-	4.7	ns
	propagation delay nSAB to nBx or nSBA to nAx	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.3	4.5	ns
		V_{CC} = 2.7 V	-	-	5.4	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; test circuit see Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	propagation delay nAx to nBx or nBx to nAx	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	0.5	2.4	3.4	ns
		V_{CC} = 2.7 V	-	-	3.9	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.7	4.2	ns
		V_{CC} = 2.7 V	-	-	4.7	ns
	propagation delay nSAB to nBx or nSBA to nAx	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.5	4.5	ns
		V_{CC} = 2.7 V	-	-	5.4	ns
t_{PZH}	output enable time $n\overline{OE}BA$ to nAx	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.7	4.3	ns
		V_{CC} = 2.7 V	-	-	5.0	ns
	output enable time nOEAB to nBx	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.6	4.2	ns
		V_{CC} = 2.7 V	-	-	4.9	ns
t_{PZL}	output enable time $n\overline{OE}BA$ to nAx	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.1	4.3	ns
		V_{CC} = 2.7 V	-	-	5.0	ns
	output enable time nOEAB to nBx	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.9	4.2	ns
		V_{CC} = 2.7 V	-	-	4.9	ns
t_{PHZ}	output disable time $n\overline{OE}BA$ to nAx	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.1	4.9	ns
		V_{CC} = 2.7 V	-	-	5.3	ns
	output disable time nOEAB to nBx	see Figure 9				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.4	5.2	ns
		V_{CC} = 2.7 V	-	-	5.8	ns
t_{PLZ}	output disable time $n\overline{OE}BA$ to nAx	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.8	4.4	ns
		V_{CC} = 2.7 V	-	-	4.6	ns
	output disable time nOEAB to nBx	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.0	4.4	ns
		V_{CC} = 2.7 V	-	-	4.6	ns

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

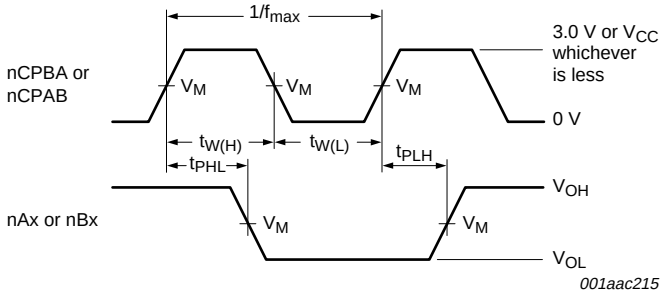
Table 9: Dynamic characteristics setup requirements

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
$t_{su(H)}$	set-up time HIGH nAx to nCPAB or nBx to nCPBA	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.6	-	ns
		V_{CC} = 2.7 V	1.1	-	-	ns
$t_{su(L)}$	set-up time LOW nAx to nCPAB or nBx to nCPBA	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.9	0.5	-	ns
		V_{CC} = 2.7 V	2.4	-	-	ns
$t_{h(H)}$	hold time HIGH nAx to nCPAB or nBx to nCPBA	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.4	-	ns
		V_{CC} = 2.7 V	1.0	-	-	ns
$t_{h(L)}$	hold time LOW nAx to nCPAB or nBx to nCPBA	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.5	-	ns
		V_{CC} = 2.7 V	1.0	-	-	ns
$t_{W(H)}$	pulse width HIGH nCPAB or nCPBA	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	2.6	2.2	-	ns
		V_{CC} = 2.7 V	2.6	-	-	ns
$t_{W(L)}$	pulse width LOW nCPAB or nCPBA	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	2.8	2.4	-	ns
		V_{CC} = 2.7 V	2.8	-	-	ns

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

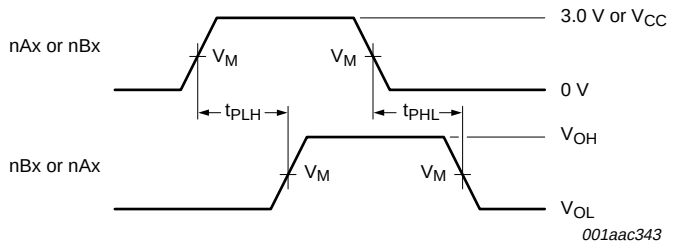
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

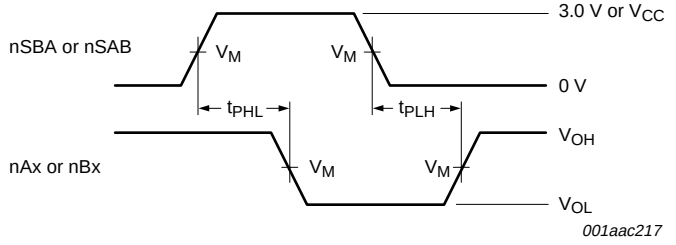
Fig 6. Propagation delay clock input to output, clock pulse width and maximum clock frequency



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

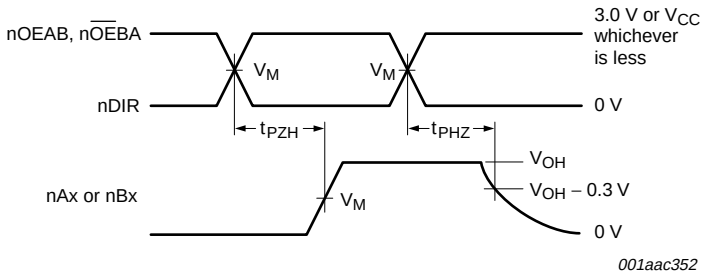
Fig 7. Propagation delay nAx to nBx or nBx to nAx



V_M = 1.5 V.

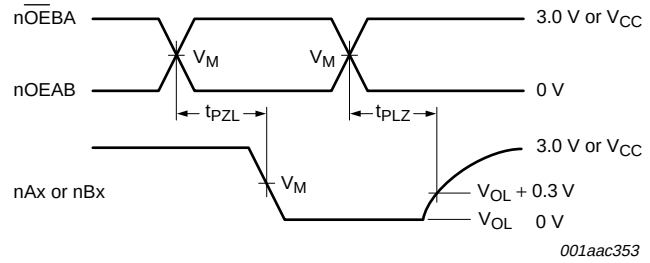
V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 8. Propagation delay SBA to nAx or SAB to nBx



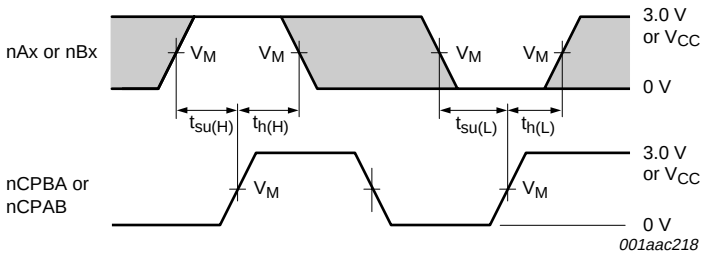
V_{OH} is typical voltage output drop that occur with the output load.

Fig 9. 3-state output enable time to HIGH-level and output disable time from HIGH-level



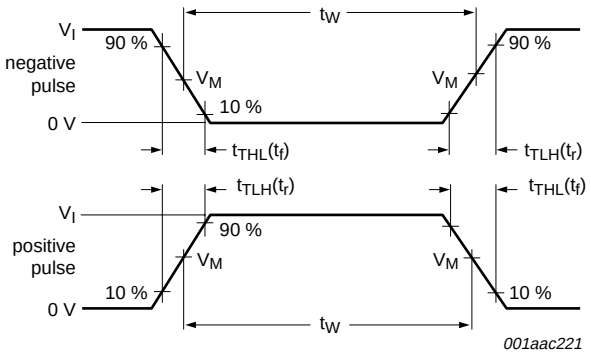
V_{OL} is typical voltage output drop that occur with the output load.

Fig 10. 3-state output enable time to LOW-level and output disable time from LOW-level



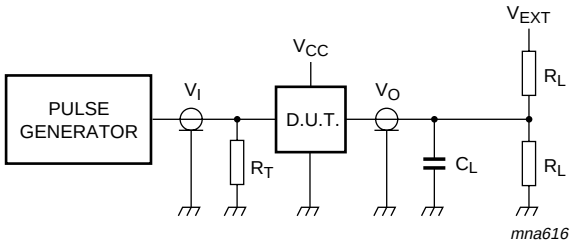
Remark: The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 11. Data set-up and hold times



V_M = 1.5 V.

a. Input pulse definition



Test data is given in Table 10.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

V_{EXT} = Test voltage for switching times.

b. Test circuit

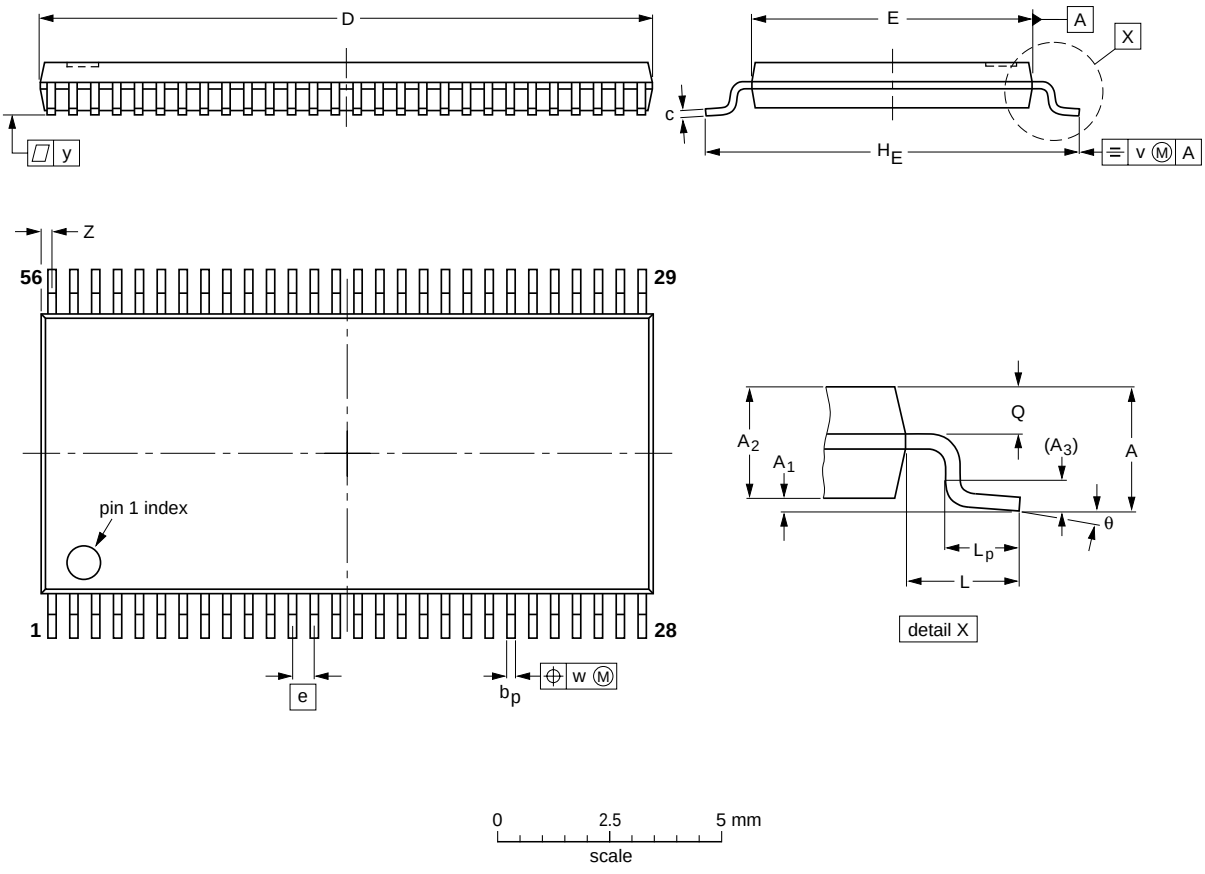
Fig 12. Load circuitry for switching times

Table 10: Test data

Input				Load		V_{EXT}		
V_I	Repetition rate	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

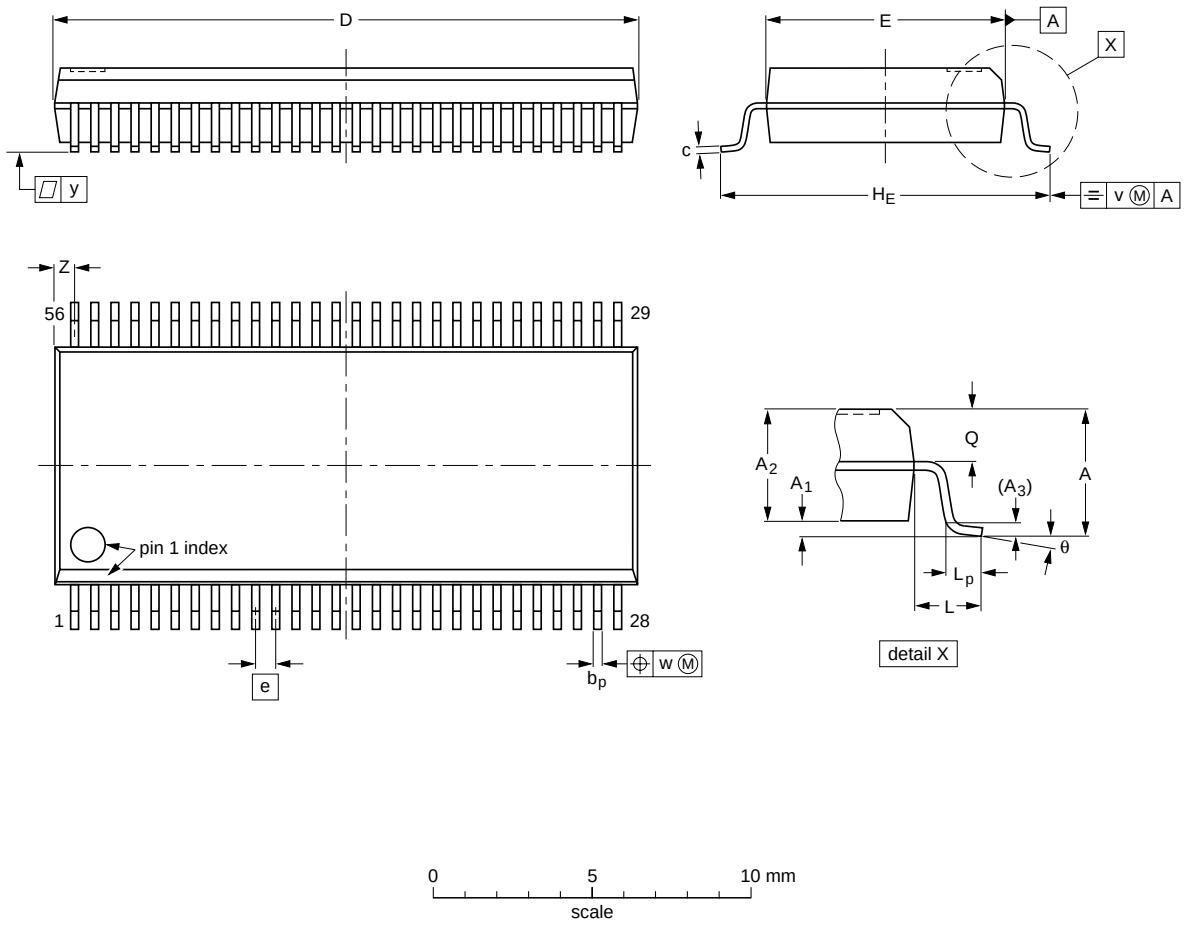
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT364-1 (TSSOP56)

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT371-1 (SSOP56)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT16652A_3	20050112	Product data sheet	-	9397 750 14402	74LVT16652A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Product title modified • Section 2 “Features”: modified JEDEC Std 17 into JESD78 • Section 3 “Quick reference data”: modified values for t_{PLH} and t_{PHL} • Section 11 “Dynamic characteristics”: modified various timing values.				
74LVT16652A_2	19980219	Product specification	-	9397 750 03561	74LVT16652A_1
74LVT16652A_1	1994	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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