

Advance Information

MC92460EC/D Rev. 1.0, 5/2002

MC92460 HDLC Controller Hardware Specifications





NCSD Applications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MC92460 Multichannel HDLC Controller.

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Figure 1 shows a block diagram of the MC92460.

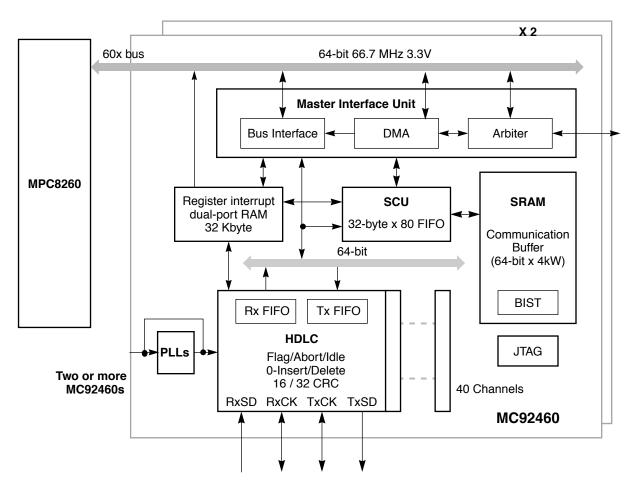


Figure 1. MC92460 Block Diagram

1.1 Features

The following is an overview of the MC92460 feature set:

- Channels
 - 40 full-duplex HDLC channels
 - Programmable channel assignment (any logical channel to any signal)
 - Each channel has a default of 64 buffer descriptors (Rx and Tx) but the number of buffer descriptors per channel is configurable
- Controllers
 - Maximum throughput of 1919 Mbps; individual controllers operate up to 66.7 Mbps
 - All communication controllers operate asynchronously
 - Programmable frame size (maximum 65,535 bytes)
 - Transparent memory access with internal memory controller
- 60x Bus
 - MC92460 directly connects with a 64-bit data and 32-bit address 60x bus
 - Supports 66.7 MHz 60x bus speed, with aggregate bandwidth of up to 1919 Mbps depending



- on the type of main memory used
- Up to four MC92460's may be connected in parallel on the 60x bus
- Bus supports multiple master design
- Communication Buffers
 - Data Buffer
 - 256 Kbits on-chip memory for data buffers
 - 256 Kbit communication buffer can store up to 819 bytes per frame.
 - 80 channel virtual DMA functionality executes between off-chip memory and the communication buffer
 - BD Buffer
 - 32 Kbyte on-chip dual-port RAM for buffer descriptors
 - A total of 4096 buffer descriptors (2048 TxBD and 2048 RxBD)
- JTAG Support
 - Supports the IEEE1149.1 JTAG controller standard
- Power and Clocks
 - Supports single-beat and burst accesses
 - On-chip PLL for baud rate generator (maximum of 66.7 MHz)
 - Separate power supplies for core internal logic (1.8V) and for I/O (3.3V)
- Package
 - 480 pin TPGA, 1.27 mm pitch



1.2 Electrical and Thermal Characteristics

This section provides AC and DC electical specifications and thermal characteristics for the MC92460.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MC92460. Table 1 shows the maximum electrical ratings.

Table 1. Maximum Temperatures and Voltages

Rating	Symbol	Value Name	Unit
Core supply voltage	VDD	-0.3 – 2.5	V
I/O supply voltage	VDDH	-0.3 – 3.6	V
Input voltage	VIN	GND-0.3 – 3.6	V
Junction temperature	Tj	120	°C
Storage temperature range	T _{STG}	-55 – 150	°C
Ambient temperature	T _A	-40 - 85	°C

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.65 – 1.95	V
I/O supply voltage	VDDH	3.15 – 3.465	V
Input voltage	VIN	GND -0.3 – 3.6	V
Junction temperature	Tj	105	°C

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics

TA=0 to 85° C; VDD= $2.0\pm5\%$ Vdc; VDDH= $3.3\pm5\%$ Vdc; GND=0Vdc; Load Capacitance < 10pF

Characteristics	Conditions	Symbol	Min	Max	Unit
Input high voltage		V _{IH}	2.0	3.465	V
Input low voltage		V_{IL}	GND	0.8	V
Input leakage current	V _{IN} =VDDH	I _{IN}	_	10	uA
HI-Z leakage current	V _{IN} =VDDH, GND	l _{OZ}	-10	+10	uA
Signal low input current	V _{IL} =0.8V	I _{IL}	_	60	uA
Signal high input current	V _{IH} =2.0V	I _{IH}	_	60	uA
Output high voltage	I _{OH} =-7.0mA	V _{OH}	2.4	-	V



Table 3. DC Electrical Characteristics (continued)

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Output low voltage BR BG ABB TS A[0-31] AP[0-3] APE TT[0-4] TBST TSIZ[0-2] GBL CI WT LBCLAIM BTO INT TC[0-1] AACK ARTRY DBG DBWO DBB DH[0-31],DL[0-31] DP[0-7] DPE DBDIS TA	I _{OL} =7.0mA	V _{OL}	0.4	V
Output low voltage Rx CLK[0-39] Tx CLK[0-39] Tx SD[0-39] TDO SBG SDBG SBR SIRQ CS0 CS1	I _{OL} =5.0mA	V _{OL}	0.4	V



1.2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Maximum Temperatures and Voltages

Characteristics	Symbol	Thermal Resistance Value	Unit	Air Flow		
Thermal resistance for 480 TBGA		10.48	°C/W	0 LFM		
	$\theta_{\sf JA}$	8.61	°C/W	100 LFM		
		θ_{JA}	$ heta_{JA}$	$ heta_{JA}$	7.78	°C/W
		6.89	°C/W	400 LFM		
		5.52	°C/W	800 LFM		

LFM = Linear Feet per Minute

1.2.3 Power Considerations

The average chip-junction temperature, Tj, can be obtained from the following:

$$T_{J} = T_{A} + (P_{D} \bullet \theta_{JA})$$

where

 θ_{IA} = package thermal resistance, junction to ambient, °C/W

 $T_A = ambient temperature, °C$

Power equations are the following:

 $P_{D} = P_{VDD} + P_{VDDH} = chip total power dissipation, W$

 $P_{VDD} = I_{VDD} \times VDD = \text{chip core power, W}$

 $P_{VDDH} = I_{VDDH} \times VDDH$

= user-determined power dissipation on input/output pins, W

1.2.4 Power Dissipation

Table 5 describes maximum chip core power dissipation.

Table 5. Maximum Core Power Dissipation (PVDD)

VDD(V)	SYSCLK Frequency (MHz)	IVDD (mA)	PVDD (mW)	Pvddh(mW)
1.95	66.7	650	980	920



1.2.5 AC Specifications

These AC specifications are target specifications.

1.2.5.1 SYSCLK Timing

Table 6 shows the system clock timing.

Table 6. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	60.0	66.7	MHz
Clock period		15.0	16.7	nS
Clock pulse width	t _{CL} ,t _{CH}	7	8	nS
SYSCLK input high voltage	V _{IHC}	2.4	3.465	V
SYSCLK input low voltage	V _{ILC}	GND	0.4	V
SYSCLK Jitter			±200	pS

Figure 2 shows the SYSCLK.

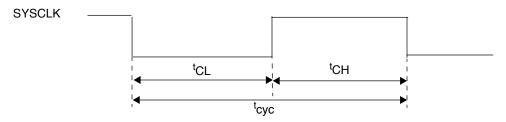


Figure 2. SYSCLK

1.2.5.2 EXCLK Timing

Table 7 shows the external clock timing.

Table 7. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	14.0	16.0	MHz
Clock duty		40	60	%
Clock Pulse width	t _{CL} ,t _{CH}	25	42.8	nS
EXCLK input high voltage	V _{IHC}	2.4	3.465	V
EXCLK input low voltage	V _{ILC}	GND	0.4	V
EXCLK Jitter			<u>+</u> 200	pS



Electrical and Thermal Characteristics

Figure 3 shows the EXCLK.

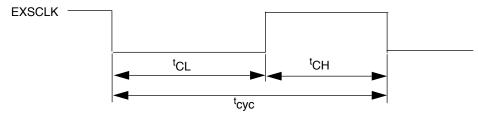


Figure 3. EXCLK

1.2.5.3 **AC Timing**

Figure 4 shows the HDLC external clock with polarity not inverted. All time specifications were measured at expected load capacitance C_L =8pF.

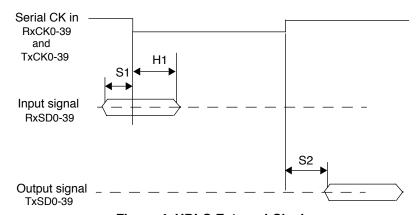


Figure 4. HDLC External Clock

Figure 5 shows an HDLC internal clock (TxCK/RxCK output mode) whose polarity is not inverted.

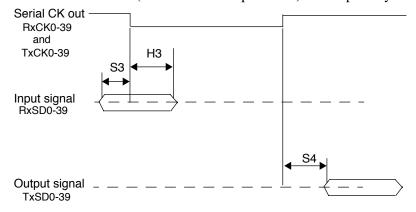


Figure 5. HDLC Internal Clock



Table 8 shows the AC electrical characteristics. The frequency is 20 MHz.

Table 8. AC Electrical Characteristics

Spec Num	Characteristic	Min	Max	Unit
S1	HDLC input- external clock setup time	2		nS
H1	HDLC input -external clock hold time	1		nS
S2	HDLC output- external clock setup time		14	nS
S3	HDLC input- internal clock setup time	12		nS
H3	HDLC input- internal clock hold time	0		nS
S4	HDLC output- internal clock setup time		4	nS

Figure 6 shows the interaction of several bus signals.

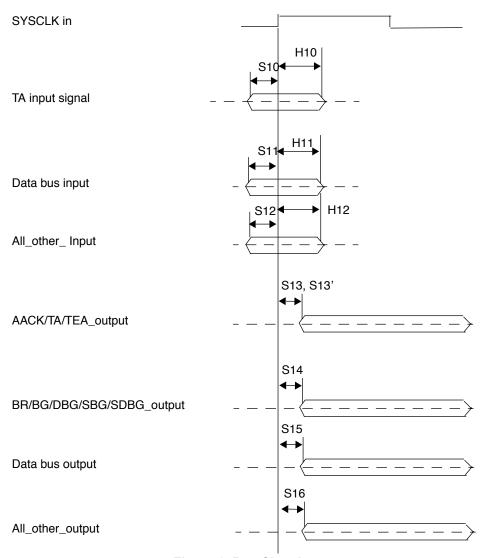


Figure 6. Bus Signals



Electrical and Thermal Characteristics

Table 9 shows the bus signal I/O characteristics. The frequency is 20 MHz.

Table 9. Bus Input/Output Characteristics

Spec Num	Characteristic	Min	Max	Unit
S10	TA/TEA input	6		nS
H10	TA/TEA input		1	nS
S11	Data bus input signals	7		nS
H11	Data bus input signals		1	nS
S12	All other input signals	7		nS
H12	All other input signals		1	nS
S13	AACK/TEA output	1	7	nS
S13'	TA output	1	8.5	nS
S14	BR/BG/DBG/SBG/SDBG output	1	7	nS
S15	Data bus output signals	1	8.5	nS
S16	All other output signals	1	7	nS



1.3 Pinout

Table 10. Pin Assignments

Ball	A	В	၁	Q	E	124	Ů	н	r	K	ı	M	z	Ь	~	H	n	>	W	Y	AA	AB	AC	AD	AE	AF	AG	ЧΥ	Υ	Ball
-	PowVdd5	PowVdd6	Pow/vdd30	DP3	CoreGnd0	CoreVdd0	житку	112	Pow Gnd2	SBG	Pow Grid3	A8	SBR	A15	CoreVdd2	A18	A22	A25	A29	Į.	вто	ЧΗ	CSA4	CSA7	ComVdd4	TxSD0	PowVdd31	PowVdd13	PowVdd12	-
7	PowVdd7 F	PowVdd4 F	PP-	DP2	PowGnd0 C	12	AACK	DPE	SDBG	A1	A4	A7	M1	A12	CoreGnd2 C	124	CoreVdd20	A26	V30	CoreVdd3	CSA6	AP2	PowGnd10	TC1	SYSCLK	ACoreGnd1	TxSD1 P	PowVdd11 Pi	PowVdd14 Pi	7
3	PowVdd29	DP5	PowVdd3	DP0	15/20	DBG	78B	£ E	¥E	CoreGnd1	CoreVdd1	BR	A10	PowGnd5	A17	A19	A23	A27	PowGnd8	SIRG	AP0	APE	MODE	CoreGnd4	ACoreVdd1	Packo	PowVdd10	TXCK1	PowVdd32	3
4	DP4	D56	8	PowVdd2	¥	TSIZ1	0_DBG	PowGnd1	£	AO	А3	A6	PowGnd4	A14	A16	PowGnd6	A24	A28	A31	LBCLAIM	PowGnd9	WT	GBL	TxCK0	PxSD0	PowVdd9	PxSD1	TxOK2	TxSD2	4
w	D31	D39	D47	8	PowVdd1	TBST	18122	98	Ē	DBB	A2	A5	6V	A13	CoreGnd20	V50	PowGnd7	Ē	CoreGnd3	DRITRY	AP3	Ø	TC0	PIT10	PowVdd8	Pack1	CSA8	PACK2	TxSD3	ĸ
9	CoreGnd19	D23	Core Vdd25	PowGnd35	D63																				PowGnd11	PxSD2	CoreVdd5	TxCK3	PxCK3	9
7	D54	D62	PowGnd34	D15	CoreVdd19																				CoreGnd5	RxSD3	TxCK4	RxSD4	RxCK4	7
∞	PowGnd33	D30	Core@nd25	D46	70																				TxSD4	TxSD5	TxCK5	P _M CK5	PowGnd12	œ
6	19G	8	D14	D22	860																				PxSD5	TxSD6	TxCK6	CoreGnd21	PxCK6	6
10	D45	PowGnd32	DS3	CoreVdd18	DP6																				RxSD6	TxSD7	TxCK7	CoreGnd6	RxSD7	10
11	D24	DP7	029	CoreGnd18	D37																				Pack7	CoreVdd6	TxSD8	TXCK8	PxSD8	11
12	D62	09G	D5	PowGnd31	D13																				RxCK8	TxSD9	TxCK9	RxSD9	RxCK9	12
13	D28	PowGnd30	980	D44	scan_out_i																				PowGnd13	TxSD 10	TxCK10	CoreVdd21	PxSD10	13
14	CoreVdd17	D20	D4	D40	D12																				TxSD11	TxCK11	PoSD11	PacK10	PacK11	14
15	69 C	CoreGnd17	PowGnd29	D43	D51																				TxCK12	CareGnd7	PxSD12	TxSD12	CoreVdd7	15
16	980	PowGnd28	CoreVdd24	D27	D19																				PxSD13	TxCK13	TxSD13	PxCK13	PxCK12	16
17	PH .	D3	D58	CoreGnd24	D90																				PxSD14	CoreGnd22	TxCK14	TxSD14	PowGnd14	17
18	D42	PowGnd27	D34	D26	D18																				PxCK15	PxSD15	TxCK15	TxSD15	PxCK14	18
19	D32	D10	CoreVdd16	D2	PowGnd26																				PxCK16	CoreGnd8	PxSD16	TxCK16	TxSD16	19
20	D67	CareGnd16	D49	140	D33																				PowGnd15	PsSD17	TxCK17	CoreVdd8	TxSD17	20
21	CoreVdd23	D25	PowGnd25	D17	D16																				TxSD19	CoreVdd22	TxCK18	TxSD18	PxCK17	21
22	60	Б	D56	D48	D24																				PxSD20	PxSD19	TxCK19	PacK18	PxSD18	22
23	PowGnd24	scan_out_h	scan_out_g	scan_out_f	0SO																				CoreVdd9	TxSD21	TxCK20	TxSD20	PxCK19	23
42	CareGnd23	8	CoreVdd15	CSA2	CS2																				Ps:SD22	PowGnd16	CoreGnd9	TxCK21	PwCK20	7,7
25	PowGrd23	CoreGnd15	scan_out_j	scan_out_e	PowVdd22	AMODE	CoreVdd14	CSA0	TIMS	ACoreGnd2	TxCK39	TxCK38	TxCK37	PxCK35	PxCK34	Pack33	TxCK32	TxSD31	TxCK30	TxCK29	PacK27	scan_in_k	CareGnd10	TxCK24	PowVdd15	PaCK22	TxSD22	PacK21	PsSD21	25
26	scan_out_e	scan_out_k	PowGnd22	PowVdd23	SMODE1	scan_out_d	CareGnd14	HRESET	ОДІ	PACK39	CareGnd13	PowGrd20	TxSD37	PxSD35	PxSD34	PowGnd19	PvSD32	TxCK31	CoreVdd11	PxCK29	8ZDS%	TxCK27	Core Vdd 10	TxCK25	TxSD24	PowVdd16	TxSD23	TxCK22	scan_in_j	26
72	Pow\Vdd36	TESTO	PowVdd24	SMODEO	TEST3	DBWO	DBDIS	ΙŒ	EXCIK	CoreVdd13	TxSD39	TxSD38	Pac K36	TxCK35	scan_out_b	TxSD34	Pac K32	PicSD31	Ps/SD30	PowGnd18	PACK28	Ps/SD27	PxSD26	TxSD26	TxSD25	PACK23	PowVdd17	TxCK23	Pow\vdd33	27
28	PowVdd28	PowVdd25	TEST2	POR	CSA3	PowGnd21	TEST1	TRSII	ACoreVdd2	Px SD39	Вк.СК38	PxCK37	Px.SD36	TxSD36	CoreGnd12	Px SD33	TxSD33	PxCK31	scan_out_a	TxSD30	TxSD29	TxSD28	PxCK26	PowGnd17	PxSD25	PxCK24	PxSD23	PowVdd18	PowVdd20	28
29	PowVdd26	PowVdd27	PowVdd35	SEN	CSA5	CSA1	PCMD	TCK	PLL20	scan_out_c	PxSD38	PxSD37	TxCK36	CoreVdd12	TxSD35	TxCK34	TxCK33	TxSD32	PxCK30	CareGnd11	PxSD29	TxCK28	TxSD27	TxCK28	PxCK25	PxSD24	PowVdd34	PowVdd21	PowVdd19	29
	V	В	၁	Q	Ħ	14	ڻ ن	н	r	K	П	M	Z	Ь	~	T	n	>	×	Y	AA	AB	AC	ΑD	AE	AF	AG	ΑH	ΥŊ	











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