INTEGRATED CIRCUITS

DATA SHEET

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- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4047B MSI
Monostable/astable multivibrator

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

Monostable/astable multivibrator

HEF4047B MSI

DESCRIPTION

The HEF4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include + TRIGGER, – TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (Master Reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between C_{TC} and RC_{TC}, and an external resistor (R_t) must be connected between R_{TC} and RC_{TC} (continued on next page).

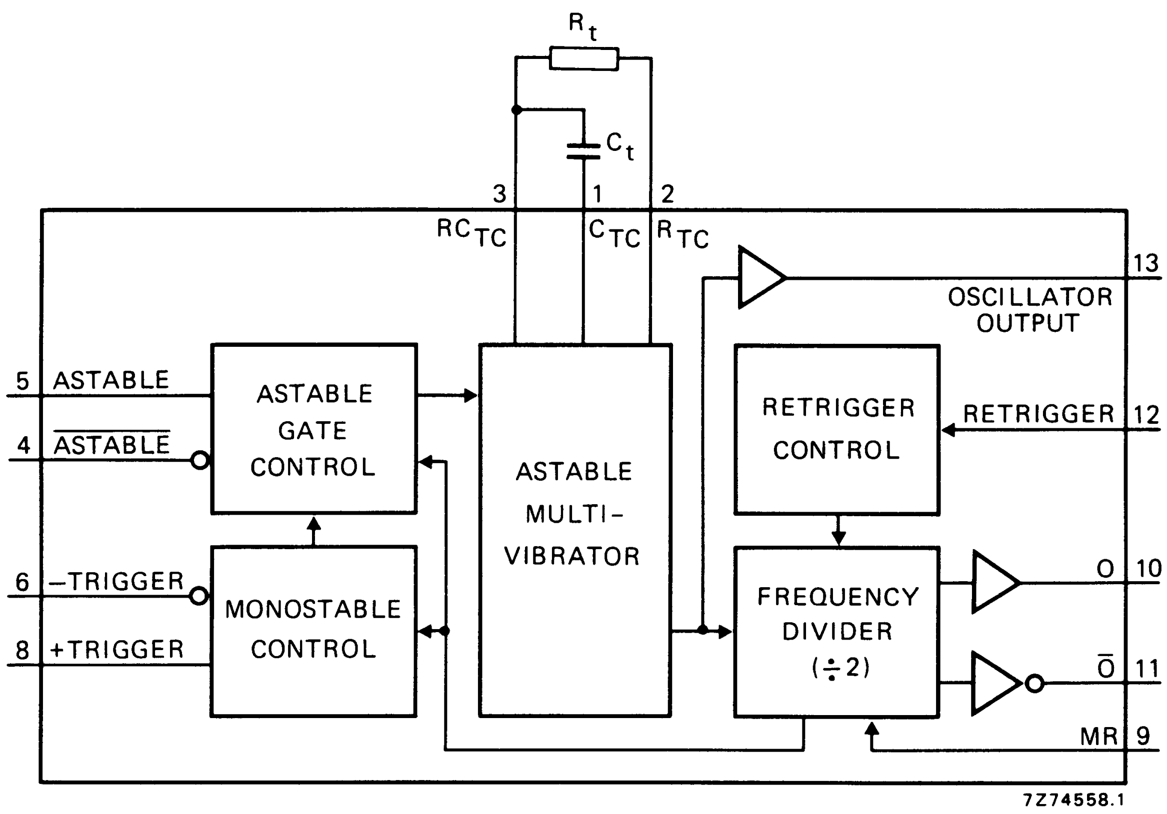


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Monostable/astable multivibrator

Astable operation is enabled by a HIGH level on the $\overline{\text{ASTABLE}}$ input. The period of the square wave at O and $\overline{\text{O}}$ outputs is a function of the external components employed. ‘True’ input pulses on the ASTABLE or ‘complement’ pulses on the $\overline{\text{ASTABLE}}$ input, allow the circuit to be used as a gatable multivibrator. The OSCILLATOR OUTPUT period will be half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the + TRIGGER input and a LOW level to the – TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the – TRIGGER and a HIGH level to the + TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and + TRIGGER inputs. In this mode the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option can be implemented by coupling O to an external ‘N’ counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

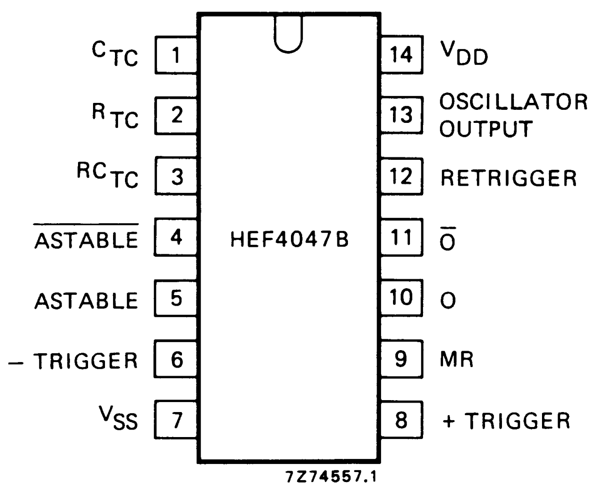


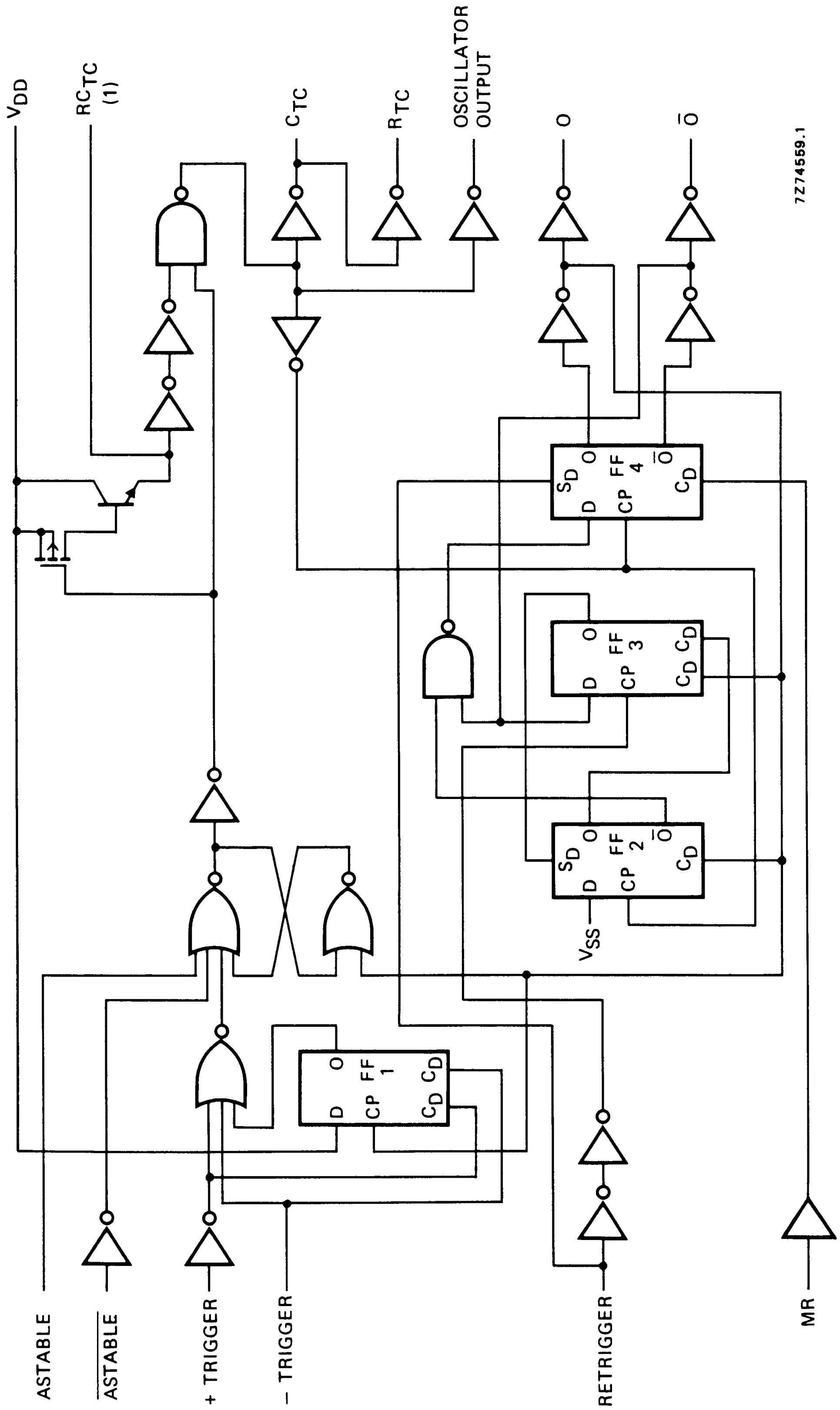
Fig.2 Pinning diagram.

HEF4047BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4047BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4047BT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America



(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard input protection pin 3 is more sensitive to static discharge; extra handling precautions are recommended.

Fig.3 Logic diagram.

FUNCTIONAL CONNECTIONS

FUNCTION	PINS CONNECTED TO			OUTPUT PULSE FROM PINS	OUTPUT PERIOD OR PULSE WIDTH
	V_{DD}	V_{SS}	INPUT PULSE		
astable multivibrator					
free running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	at pins 10, 11:
true gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A = 4,40 R_tC_t
complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	at pin 13: t_A = 2,20 R_tC_t
monostable multivibrator					
pos. edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	
neg. edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	at pins 10, 11:
retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M = 2,48 R_tC_t
external count down(1)	14	5, 6, 7, 8, 9, 12	–	10, 11	

Notes

1. Input pulse to RESET of external counting chip; external counting chip output to pin 4.
2. In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

DC CHARACTERISTICS

V_{SS} = 0 V; inputs at V_{SS} or V_{DD}

	V_{DD} V	SYMBOL	T_{amb} (°C) −40 MAX.	+ 25 MIN.	+ 25 MAX.	+ 85 MAX.		
Leakage current pin 3; output transistor OFF	15	I_3	0,3	–	0,3	1	µA	pin 3 at V_{DD} or V_{SS}

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
ASTABLE, $\overline{ASTABLE}$ → OSC. OUTPUT	5			95	190	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	43 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
	5			85	170	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
ASTABLE, $\overline{ASTABLE}$ → O, $\overline{O}$	5			150	300	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			130	260	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	49 ns + (0,23 ns/pF) C_L
	15			45	90	37 ns + (0,16 ns/pF) C_L
+/– TRIGGER → O, $\overline{O}$	5			160	320	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			155	310	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
+ TRIGGER, RETRIGGER → $\overline{O}$	5			65	130	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	19 ns + (0,23 ns/pF) C_L
	15			25	50	17 ns + (0,16 ns/pF) C_L
+ TRIGGER, RETRIGGER → O	5			95	190	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
MR → O	5			100	200	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L
MR → $\overline{O}$	5			100	200	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	9 ns + (0,42 ns/pF) C_L
	15			20	40	6 ns + (0,28 ns/pF) C_L
	5			60	120	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	9 ns + (0,42 ns/pF) C_L
	15			20	40	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum MR pulse width; HIGH	5		60	30		
	10	t_{WMRH}	30	15		
	15		20	10		
Minimum input pulse width; any input exept MR	5		220	110		
	10	t_W	100	50		
	15		70	35		

APPLICATION INFORMATION

General features:

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

Monostable multivibrator features:

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

Astable multivibrator features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

1. Astable mode design information

a. Unit-to-unit transfer-voltage variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for free running (astable) operation.

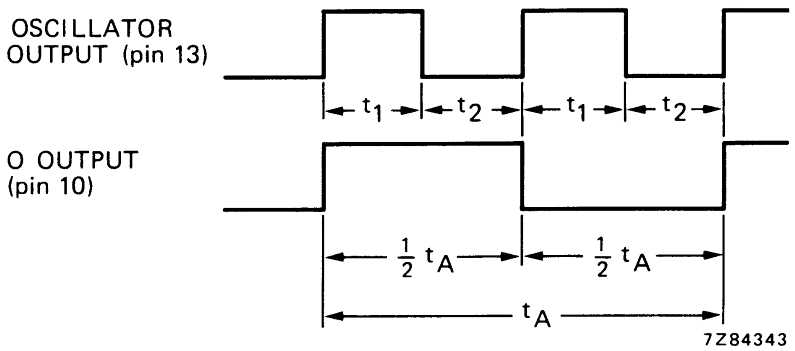


Fig.4 Astable mode waveforms.

$$t_1 = -R_tC_t \ln\frac{V_{TR}}{V_{DD}+V_{TR}}$$

$$t_2 = -R_tC_t \ln\frac{V_{DD}-V_{TR}}{2V_{DD}-V_{TR}}$$

$$t_A = 2(t_1+t_2) = -2R_tC_t \ln\frac{(V_{TR})(V_{DD}-V_{TR})}{(V_{DD}+V_{TR})(2V_{DD}-V_{TR})}$$, where t_A = Astable mode pulse width.

Values for t_A are:

	typ. :	$V_{TR} = 0{,}5\ V_{DD}$;	$t_A = 4{,}40\ R_tC_t$
V_{DD} = 5 or 10 V	min. :	$V_{TR} = 0{,}3\ V_{DD}$;	$t_A = 4{,}71\ R_tC_t$
	max.:	$V_{TR} = 0{,}7\ V_{DD}$;	$t_A = 4{,}71\ R_tC_t$
V_{DD} = 15 V	min. :	V_{TR} = 4 V;	$t_A = 4{,}84\ R_tC_t$
	max.:	V_{TR} = 11 V;	$t_A = 4{,}84\ R_tC_t$

thus if $\mathbf{t_A = 4{,}40\ R_tC_t}$ is used, the maximum variation will be (+ 7,0%; –0,0%) at 10 V.

b. Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD}. Typical variations are presented graphically in Figs 5 and 6 with 10 V as a reference.

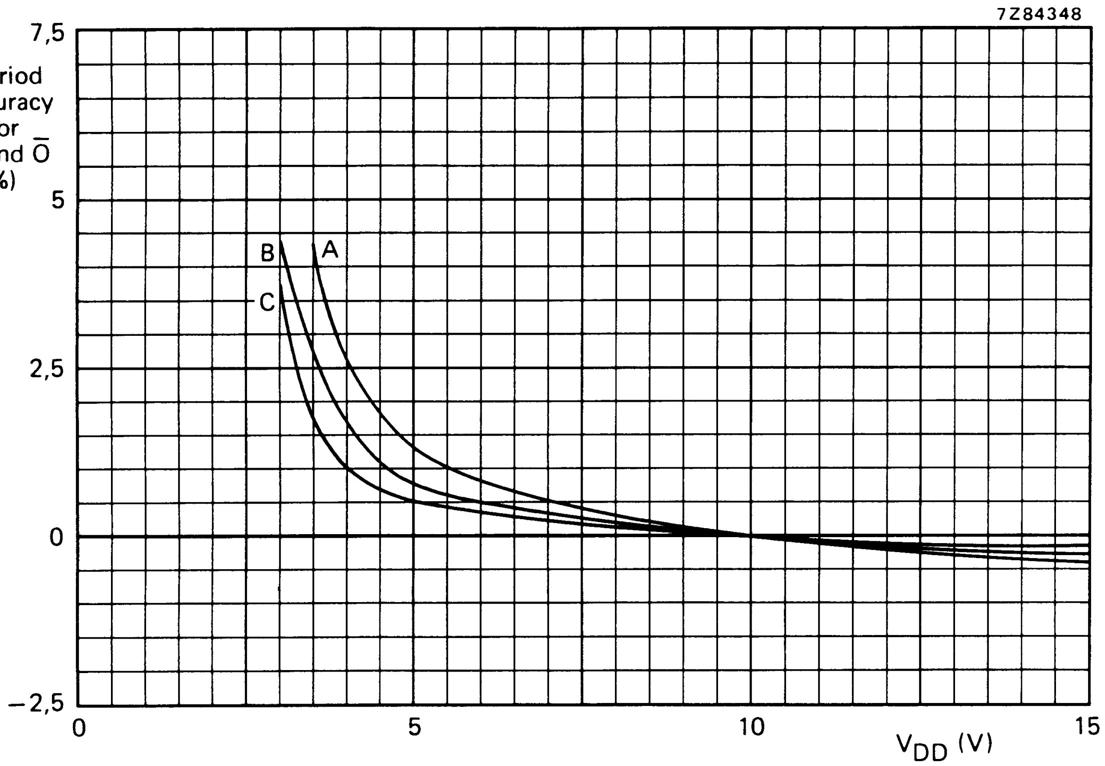


Fig.5 Typical O and Ō period accuracy as a function of supply voltage; astable mode; T_{amb} = 25 °C.

CURVE	**f_O kHz**	**C_t pF**	**R_t kΩ**
A	10	100	220
B	5	100	470
C	1	1000	220

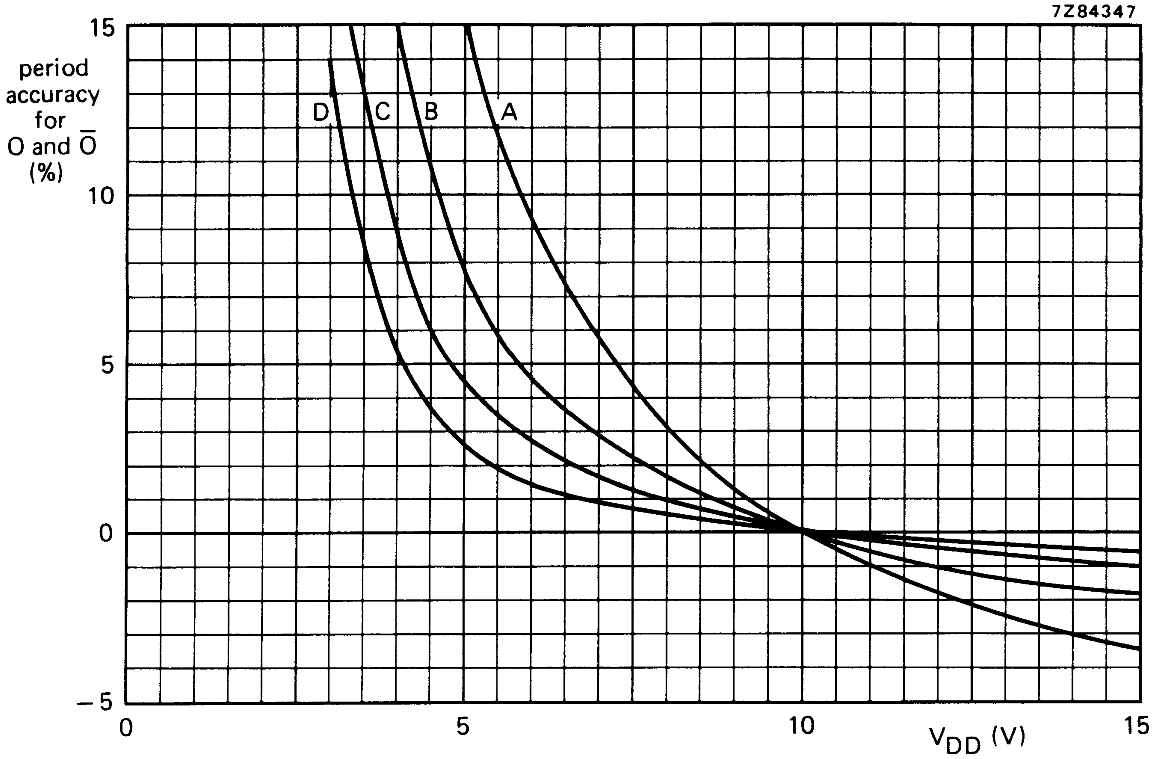


Fig.6 Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode; T_{amb} = 25 °C.

CURVE	f_O kHz	C_t pF	R_t kΩ
A	500	10	47
B	225	100	10
C	100	100	22
D	50	100	47

2. Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for one-shot (monostalbe) operation.

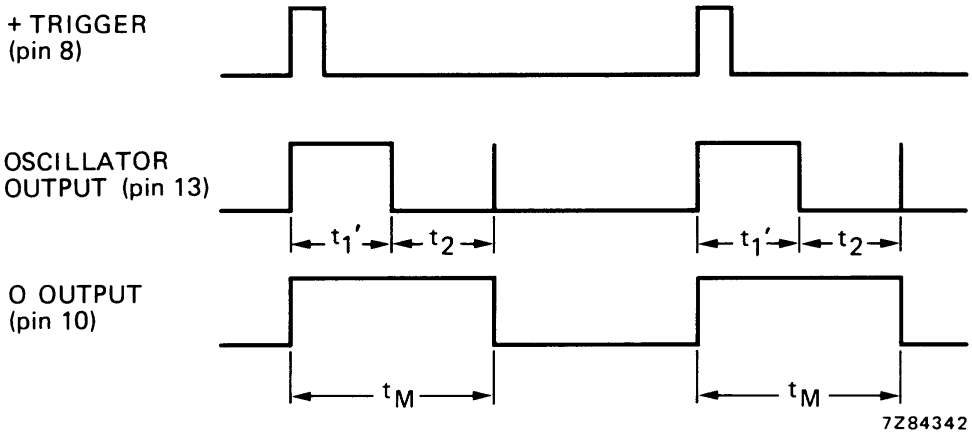


Fig.7 Monostable waveforms.

$$t_1' = -R_tC_t \ln\frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -R_tC_t \ln\frac{(V_{TR})\ (V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})\ (2V_{DD})}$$, where t_M = Monostable mode pulse width.

Values for t_M are:

	typ. :	$V_{TR} = 0,5\ V_{DD}$;	$t_M = 2,48\ R_tC_t$
V_{DD} = 5 to10 V	min. :	$V_{TR} = 0,3\ V_{DD}$;	$t_M = 2,78\ R_tC_t$
	max.:	$V_{TR} = 0,7\ V_{DD}$;	$t_M = 2,52\ R_tC_t$
V_{DD} = 15 V	min. :	V_{TR} = 4 V;	$t_M = 2,88\ R_tC_t$
	max.:	V_{TR} = 11 V;	$t_M = 2,56\ R_tC_t$

Note

1. In the astable mode, the first positive half cycle has a duration of t_M; succeeding durations are ½ t_A.

thus if $\mathbf{t_M = 2,48\ R_tC_t}$ is used, the maximum variation will be (+ 12%; –0,0%) at 10 V.

3. Retrigger mode operation

The HEF4047B can be used in the retrigger mode to extend the output pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (Fig.8). Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (output O), terminates at some variable time, t_D, after the termination of the last retrigger pulse; t_D is variable because t_{RE} (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

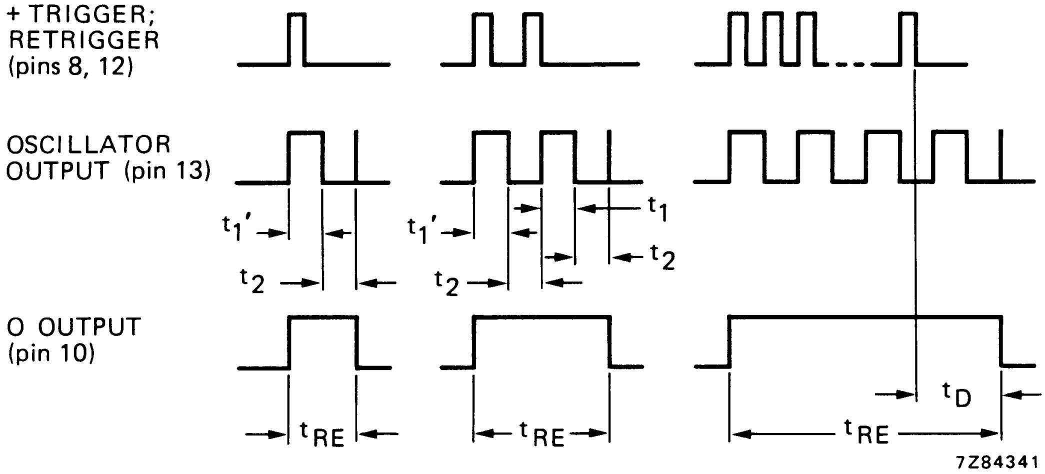


Fig.8 Retrigger mode waveforms.

4. External counter option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig.9.

The pulse duration at the output is: $t_{ext} = (N-1)(t_A) + (t_M + 1/2\, t_A)$

Where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

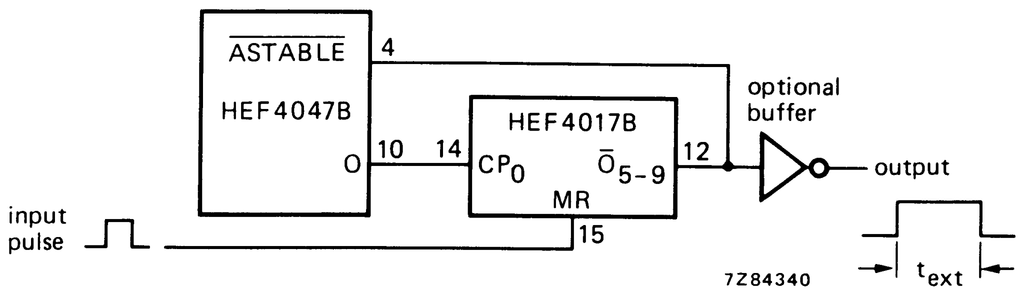


Fig.9 Implementation of external counter option.

5. Timing component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used).
There is no upper or lower limit for either R_t or C_t value to maintain oscillation.
However, in consideration of accuracy, C_t must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account).
R_t must be much larger than the LOCMOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for R_t and C_t to maintain agreement with previously calculated formulae without trimming should be:

$C_t \geq 100$ pF, up to any practical value,
$10\ k\Omega \leq R_t \leq 1\ M\Omega$.

6. Power consumption

In the standby mode (monostable or astable), power dissipation will be a function of leakage current in the circuit.
For dynamic operation, the power needed to charge the external timing capacitor C_t is given by the following formulae:

Astable mode:	$P = 2\ C_t V^2 f$ (f at output pin 13) $P = 4\ C_t V^2 f$ (f at output pins 10 and 11)
Monostable mode:	$P = \frac{(2,9\ C_t V^2)(\text{duty cycle})}{T}$ (f at output pins 10 and 11)

Because the power dissipation does not depend on R_t, a design for minimum power dissipation would be a small value of C_t. The value of R would depend on the desired period (within the limitations discussed previously).
Typical power consumption in astable mode is shown in Figs 10, 11 and 12.

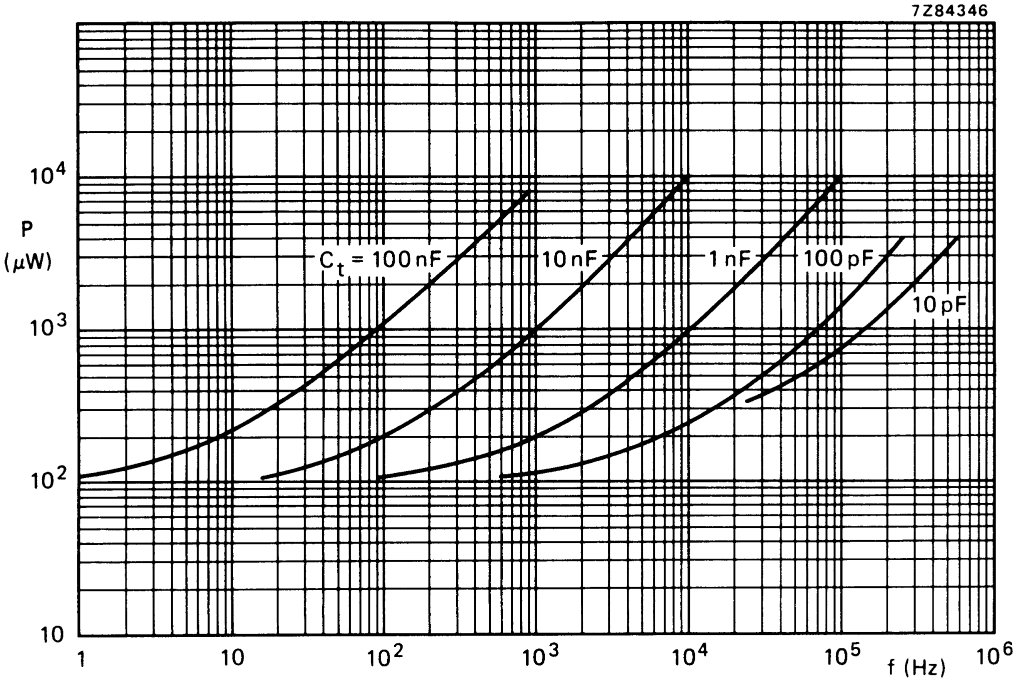


Fig.10 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 5 V; astable mode.

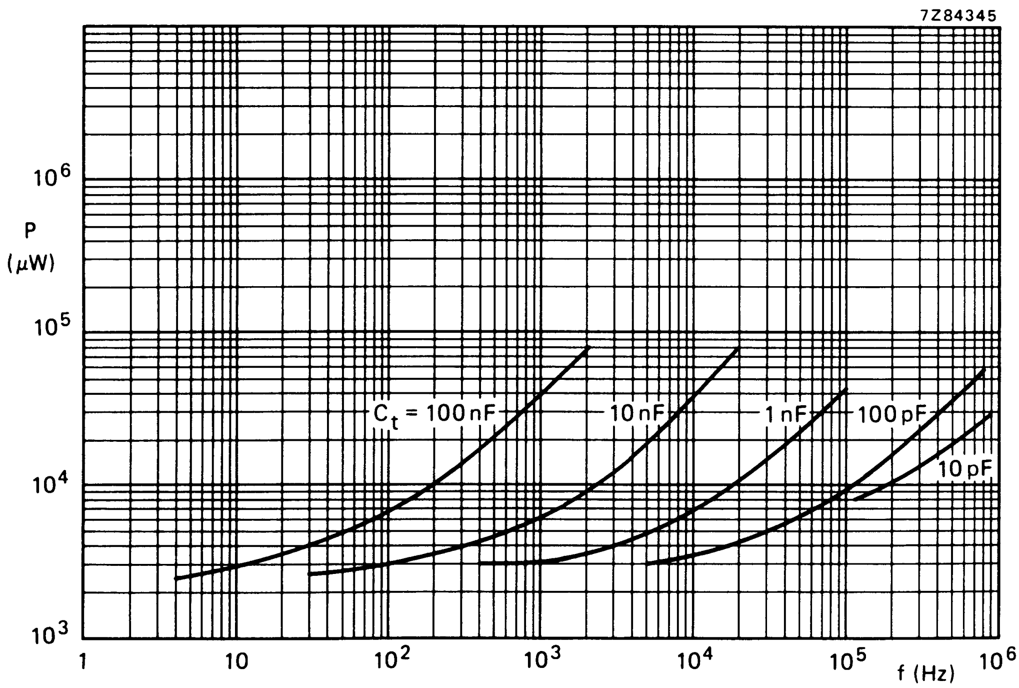


Fig.11 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 10 V; astable mode.

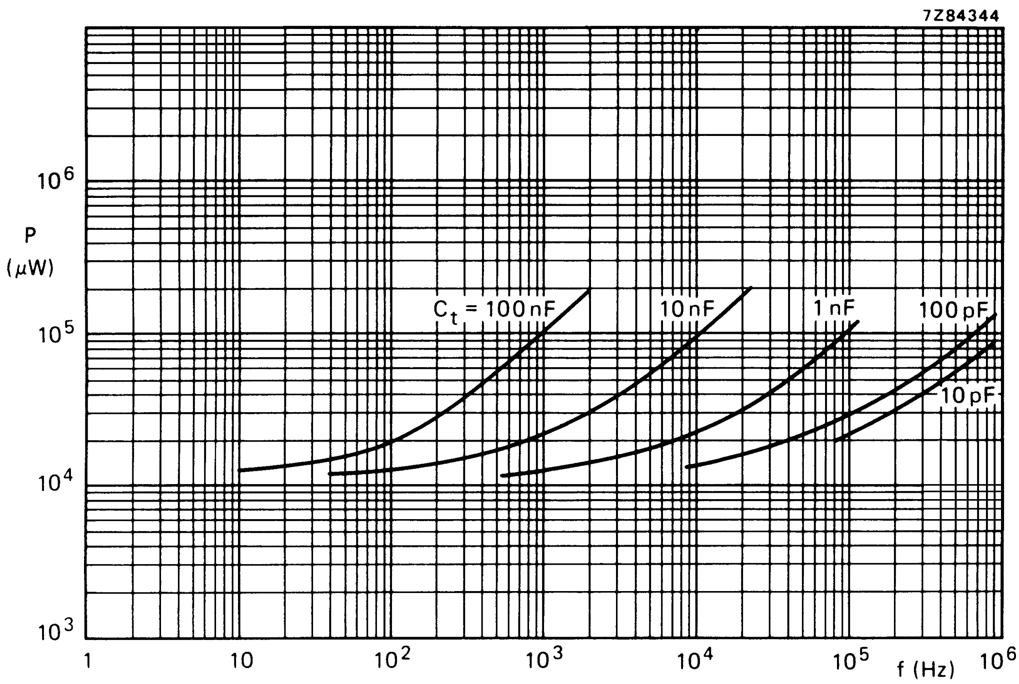


Fig.12 Power consumption as a function of the output frequency at O or $\overline{O}$; V_{DD} = 15 V; astable mode.