

# DATA SHEET

**74F540**

Octal inverter buffer (3- State)

**74F541**

Octal buffer (3- State)

Product specification

1990 Jan 08

IC15 Data Handbook

# Buffers

# 74F540, 74F541

74F540 Octal Inverter Buffer (3-State)  
 74F541 Octal Buffer (3-State)

### FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Low power, light bus loading
- Functionally similar to the 74F240 and 74F241
- Provides ideal interface and increases fan-out of MOS microprocessors
- Efficient pinout to facilitate PC board layout
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

### DESCRIPTION

The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

### ORDERING INFORMATION

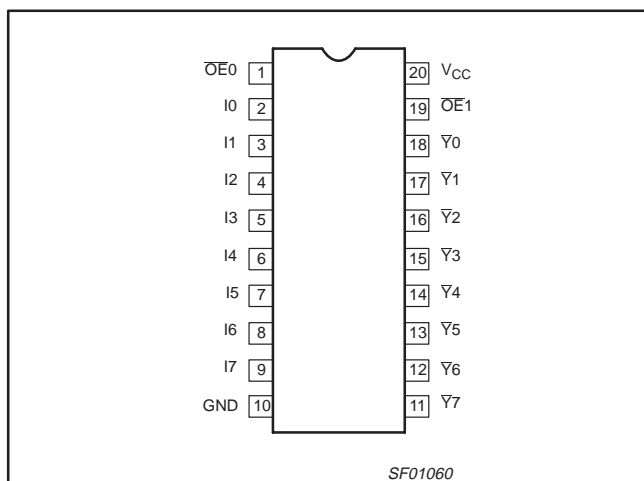
DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F540, N74F541N	SOT146-1
20-Pin Plastic SOL	N74F540D, N74F541D	SOT163-1

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

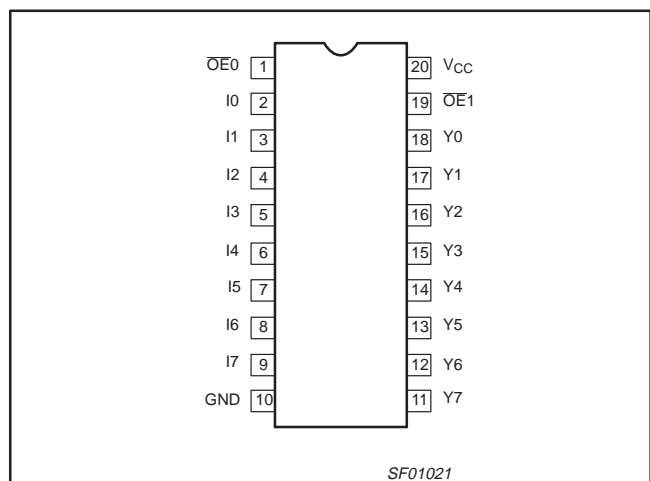
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0–I7	Data inputs	1.0/0.033	20µA/20µA
OE0, OE1	3-State output enable inputs (active Low)	1.0/0.033	20µA/20µA
Y0 - Y7	Data outputs (74F541)	750/106.7	15mA/64mA
Y0 - Y7	Data outputs (74F540)	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

### PIN CONFIGURATION – 74F540



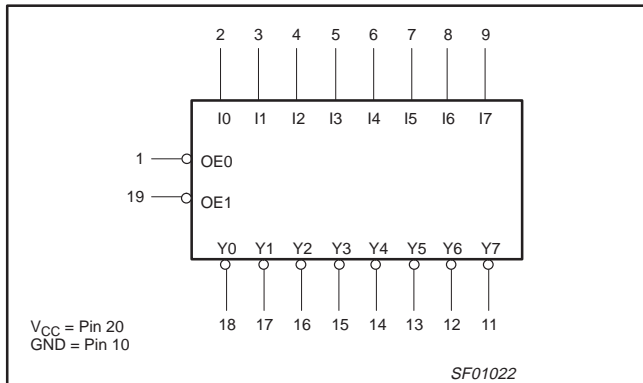
### PIN CONFIGURATION – 74F541



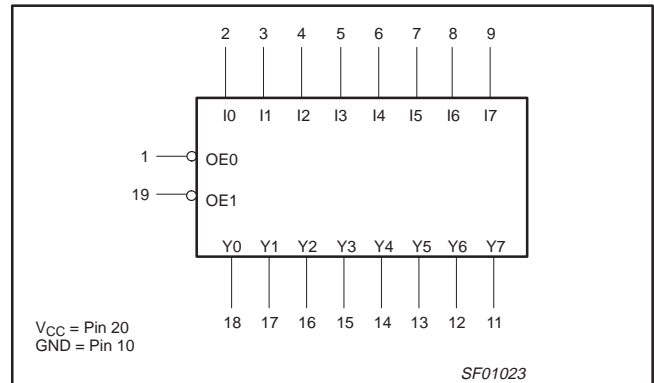
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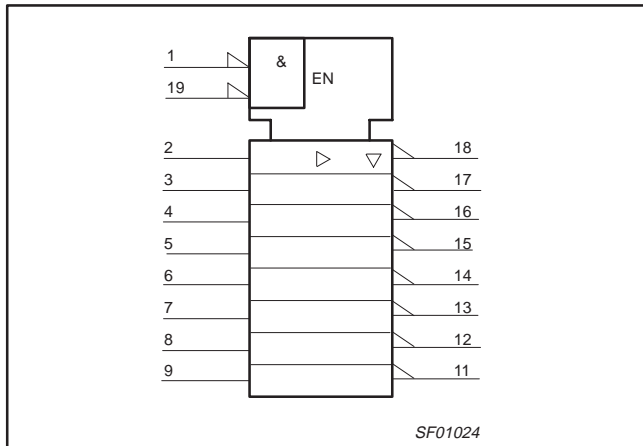
**LOGIC SYMBOL – 74F540**



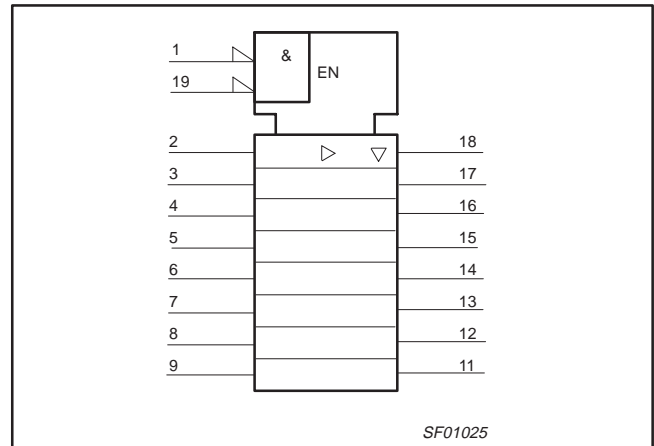
**LOGIC SYMBOL – 74F541**



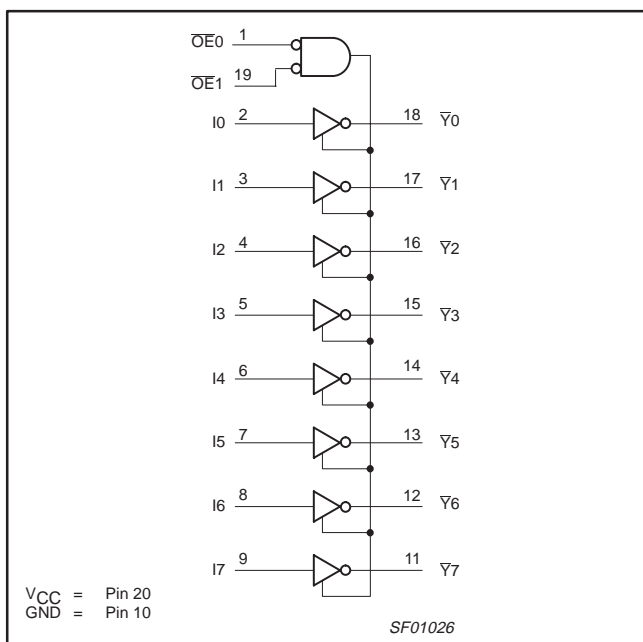
**LOGIC SYMBOL (IEEE/IEC) – 74F540**



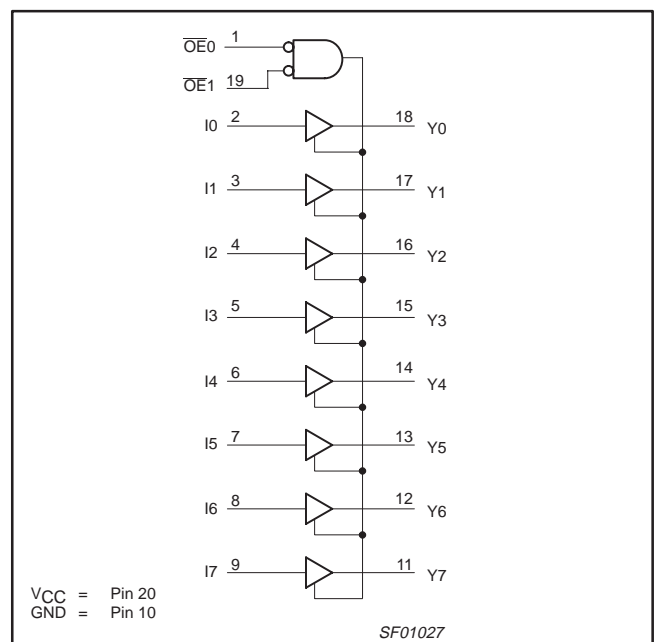
**LOGIC SYMBOL (IEEE/IEC) – 74F541**



**LOGIC DIAGRAM – 74F540**



**LOGIC DIAGRAM – 74F541**



## Buffers

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## FUNCTION TABLE

INPUTS			OUTPUTS	
			74F541	74F540
OE0	OE1	In	Yn	Yn
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level

L = Low voltage level

X = Don't care

Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5.0	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

# Buffers

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>			LIMITS			UNIT
					MIN	TYP NO TAG	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V
				±5%V <sub>CC</sub>	2.7	3.4		V
			I <sub>OH</sub> = -15mA	±10%V <sub>CC</sub>	2.0			V
				±5%V <sub>CC</sub>	2.0			V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.55	V	
				±5%V <sub>CC</sub>		0.42	0.55	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V				100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-20	μA	
I <sub>OZH</sub>	Off-state output current High-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V				50	μA	
I <sub>OZL</sub>	Off-state output current Low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V				-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>	V <sub>CC</sub> = MAX			-100	-225	mA	
I <sub>CC</sub>	Supply current (total)	74F540	V <sub>CC</sub> = MAX	In=0E̅n=GND	22	30	mA	
				In=4.5V, 0E̅n=GND	58	75	mA	
				In=GND, 0E̅n=4.5V	40	55	mA	
		74F541		In=4.5V, 0E̅n=GND	30	40	mA	
				In=0E̅n=GND	55	72	mA	
				In=GND, 0E̅n=4.5V	45	58	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> should be performed last.

# Buffers

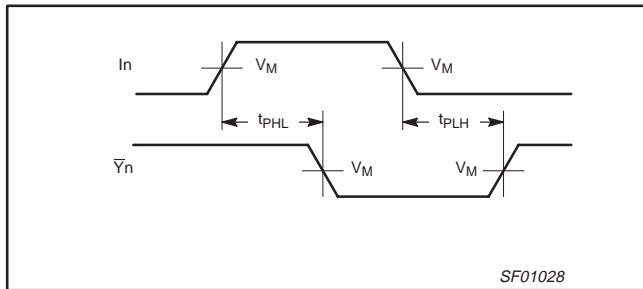
# 74F540, 74F541

## AC ELECTRICAL CHARACTERISTICS

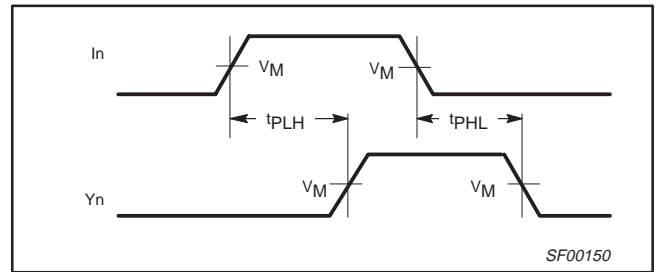
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT		
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω				
			MIN	TYP	MAX	MIN	MAX			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to $\bar{Y}_n$	74F540	Waveform 1		3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4		2.0 4.0	3.5 7.5	6.5 9.5	2.0 4.0	7.0 10.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Disable time from High or Low level		Waveform 3 Waveform 4		2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to $\bar{Y}_n$	74F541	Waveform 2		2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4		3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Disable time from High or Low level		Waveform 3 Waveform 4		2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns ns

## AC WAVEFORMS

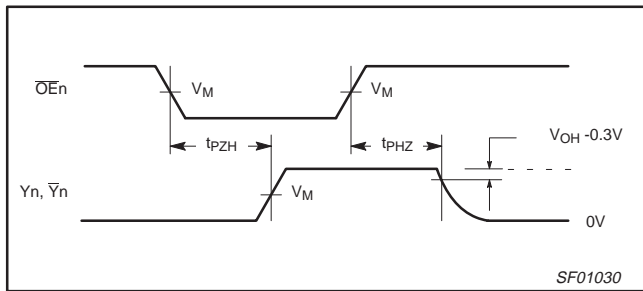
For all waveforms, V<sub>M</sub> = 1.5V.



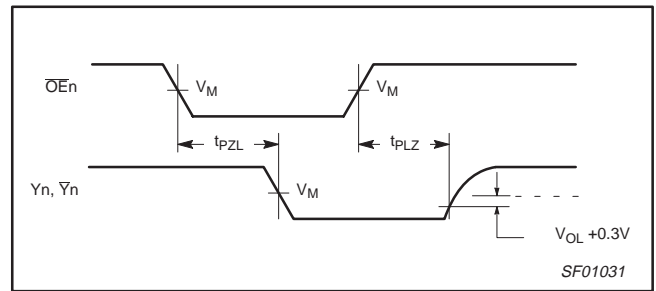
Waveform 1. Propagation Delay Data to Outputs for 74F540



Waveform 2. Propagation Delay Data to Outputs for 74F541



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

# Buffers

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## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

The diagram shows a pulse generator connected to the input  $V_{IN}$  of a D.U.T. (Device Under Test) through a termination resistor  $R_T$ . The output  $V_{OUT}$  is connected to a load resistor  $R_L$  and a load capacitor  $C_L$ . A switch is connected to the output, controlled by a 7.0V signal. The supply voltage  $V_{CC}$  is also indicated.

**Input Pulse Definition**

The waveforms show the timing parameters for negative and positive pulses. The pulse amplitude is  $V_M$ . The pulse width is  $t_w$ . The rise time is  $t_{TLH}(t_r)$  and the fall time is  $t_{THL}(t_f)$ . The signal levels are marked at 90% and 10% of the pulse amplitude.

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

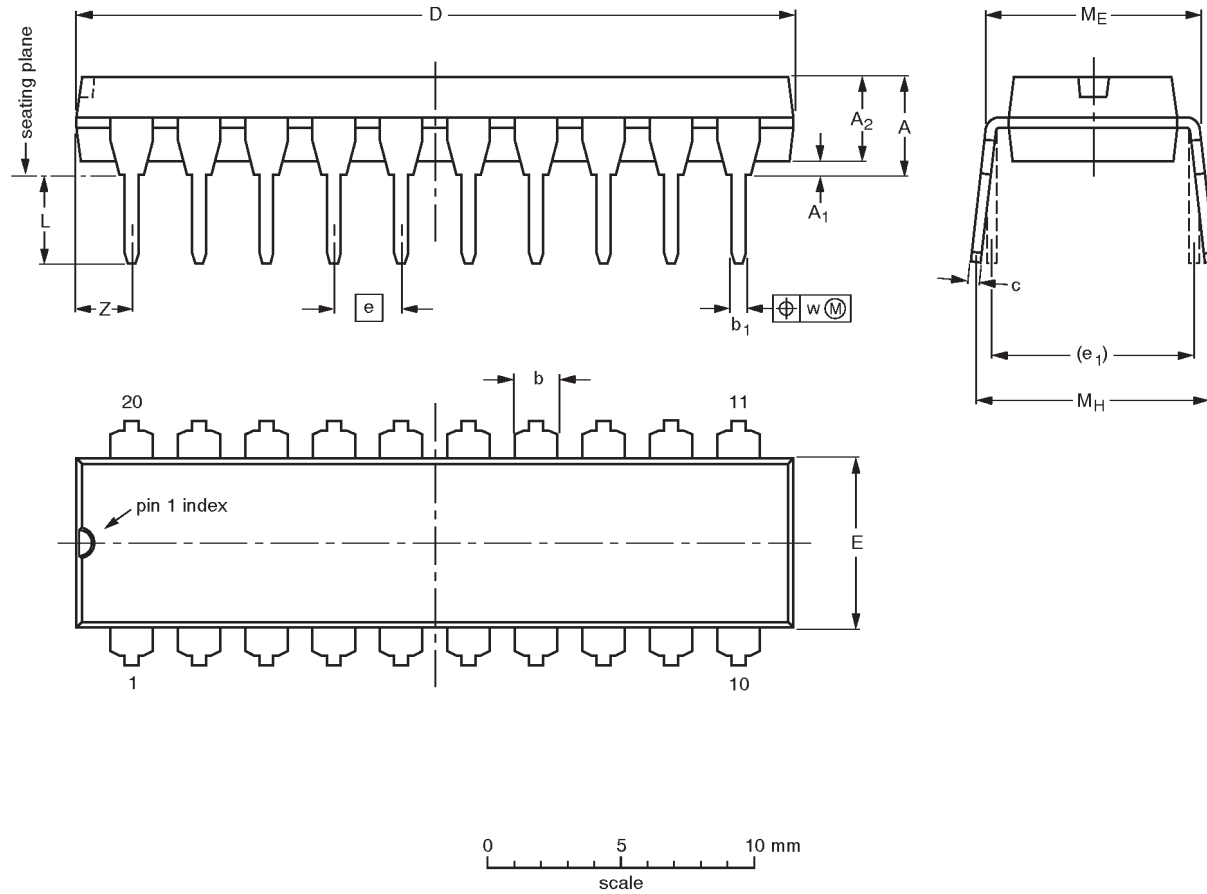
SF00777

# Buffers

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

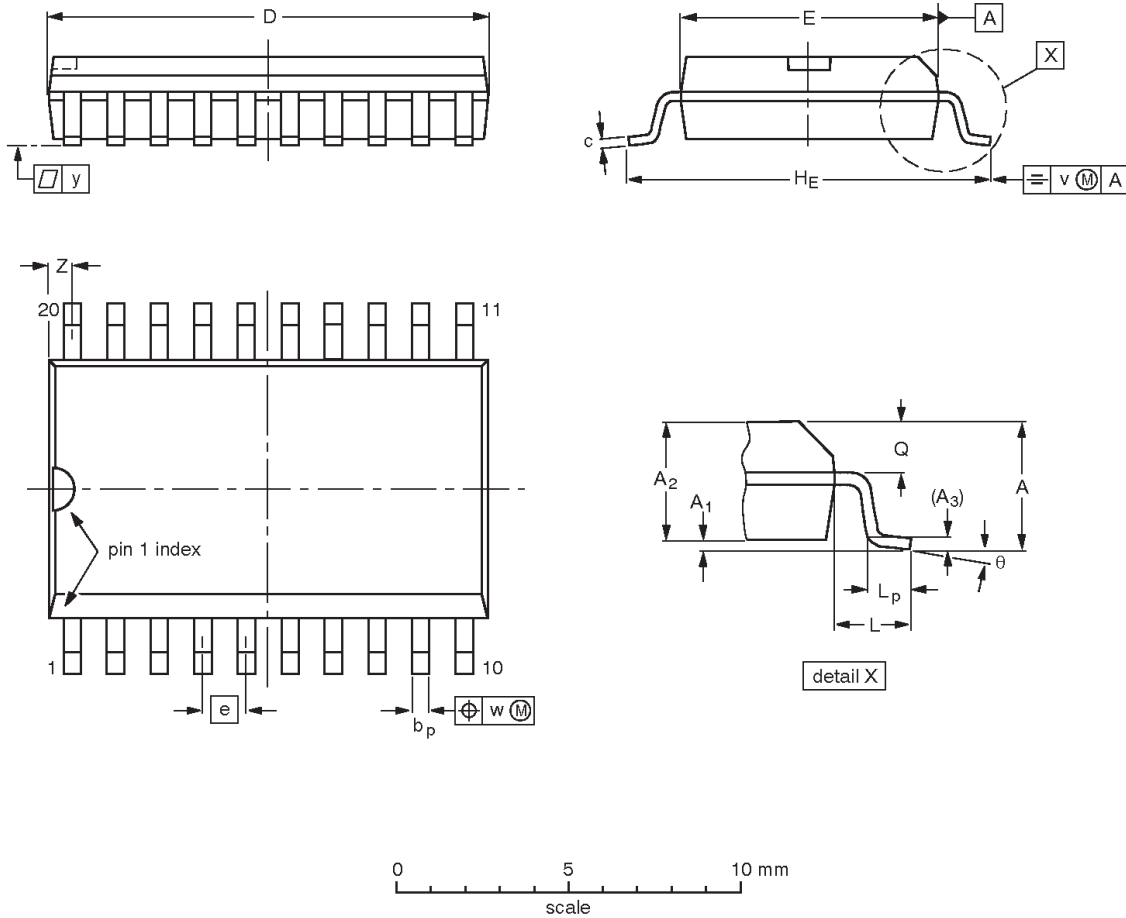


Buffers

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

## Buffers

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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