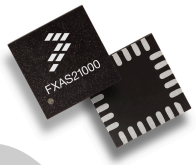
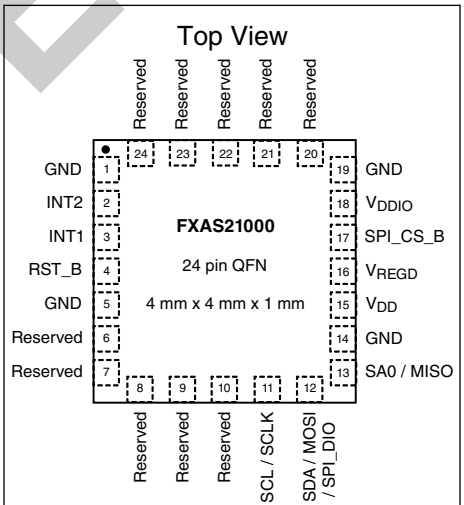
3-Axis Digital Angular Rate Gyroscope

FXAS21000



24 QFN
4 mm x 4 mm x 1 mm
Case 2209-01



Pin Connections

FXAS21000 is a small, low-power, 3-axis yaw, pitch, and roll angular rate gyroscope. The full-scale range is adjustable from ±200°/s to ±1600°/s, with Output Data Rates (ODR) from 1.5625 to 200 Hz. It features both I^2C and SPI interfaces. The device may be configured to generate an interrupt when a user-programmable angular rate threshold is crossed on any one of the enabled axes.

FXAS21000 is available in a plastic QFN package; the device is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.

Features

- Supply voltage (V_{DD}) from 1.95 V to 3.6 V
- Interface supply voltage (V_{DDIO}) from 1.62 V to 3.6 V
- I^2C interfaces
  - Normal mode (100 kHz)
  - Fast mode (400 kHz)
- SPI interface
  - Up to 2 MHz (3- and 4-wire modes)
- FIFO buffer is 192 bytes (32 X/Y/Z samples) with stop and circular operating modes
- Output Data Rates (ODR) from 1.5625 to 200 Hz; integrated antialiasing filter ensures that output signal bandwidth is limited to ODR/2
- Angular rate sensitivity of 0.2°/s in ±1600°/s FSR mode
- Low power standby mode
- Rate threshold interrupt
- Integrated self-test function
- No external charge-pump capacitor required

Typical Applications

- Game controller
- Gyro stabilized electronic compass
- Orientation determination
- Gesture-based user interfaces and Human Machine Interface (HMI)
- Indoor navigation
- Mobile phones
- Hobby and toy grade RC vehicles and UAVs
- Virtual and augmented reality devices (including glasses)

Ordering Information

Part Number	Temperature Range	Package Description	Shipping
FXAS21000CQR1	–40 °C to +85 °C	QFN	Tape and reel (1 k)

Related Documentation

The FXAS21000CFXAS21000C device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to freescale.com/FXAS21000CFXAS21000C.
2. Click on the **Documentation** tab.

Table of Contents

1 General Description

1.1 Block Diagram

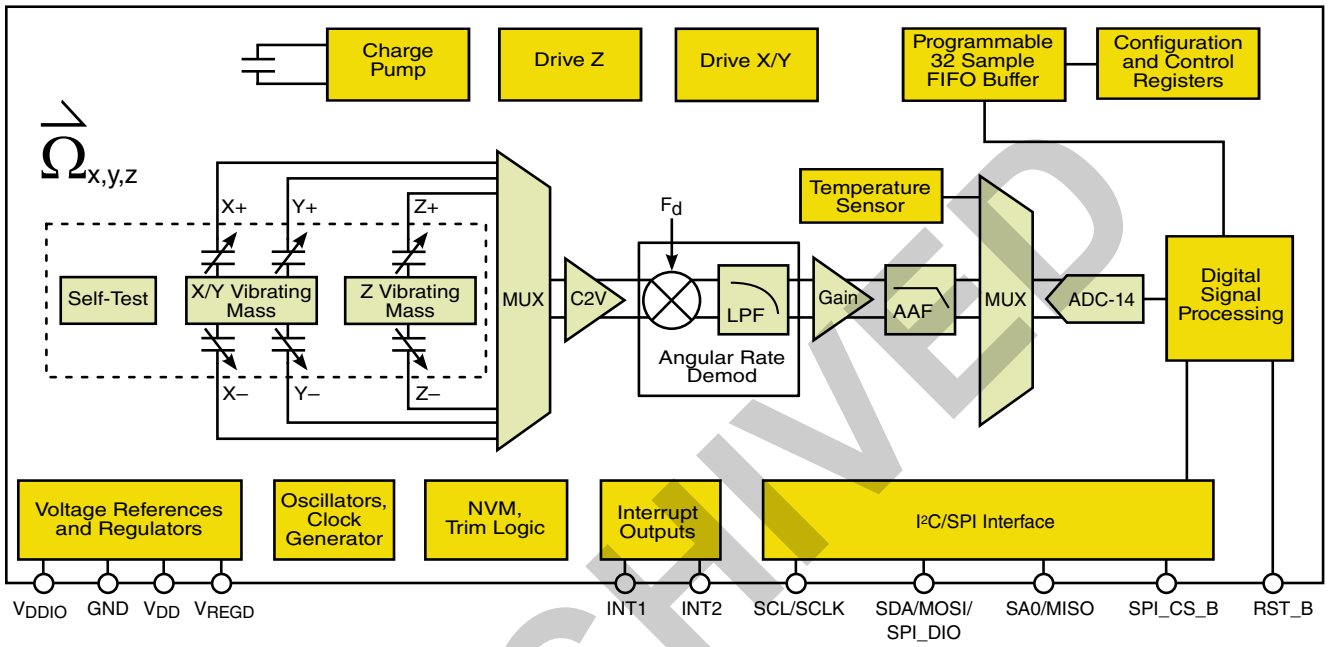


Figure 1. Block Diagram

1.2 Pinout

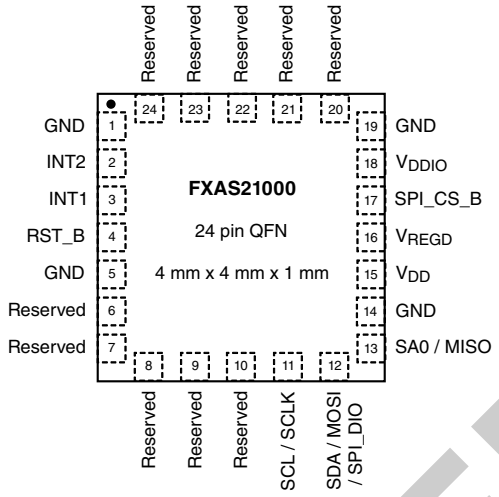


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	GND	Ground
2	INT2	Interrupt Output 2
3	INT1	Interrupt Output 1
4	RST_B	Reset input (active low, connect to V_{DDIO} if unused)
5	GND	Ground
6	Reserved	Reserved - Must be tied to ground
7	Reserved	Reserved - Must be tied to ground
8	Reserved	Reserved - Must be tied to ground
9	Reserved	Reserved - Must be tied to ground
10	Reserved	Reserved - Must be tied to ground
11	SCL/SCLK	I^2C / SPI clock
12	SDA/MOSI/SPI_DIO	I^2C data / SPI 4-wire Master Out Slave In / SPI 3-wire data In/Out [1]
13	SA0/MISO	I^2C address bit0 / SPI 4-wire Master In Slave Out
14	GND	Ground
15	V_{DD}	Supply voltage
16	V_{REGD}	Digital regulator output. Please connect a 0.1 µF capacitor between this pin and GND
17	SPI_CS_B	SPI chip select input, active low. This pin must be held logic high when operating in I^2C interface mode (I^2C/SPI_CS_B set high) to ensure correct operation.
18	V_{DDIO}	Interface supply voltage
19	GND	Ground
20	Reserved	Reserved - Must be tied to ground
21	Reserved	Reserved - Must be tied to ground

Table continues on the next page...

Table 1. Pin functions (continued)

Pin	Name	Function
22	Reserved	Reserved - Must be tied to ground
23	Reserved	Reserved - Must be tied to ground
24	Reserved	Reserved - Must be tied to ground

1. MOSI becomes a bidirectional data pin when FXAS21000C is operated in 3-wire SPI mode with **CTRL_REG0[**SPIW**]** = 1.

1.3 System Connections

The FXAS21000 offers the choice of connecting to a host processor through either I^2C or SPI interfaces. Figure 3 and Figure 4 show the recommended circuit connections for implementing both options.

1.3.1 Typical Application Circuit—I^2C Mode

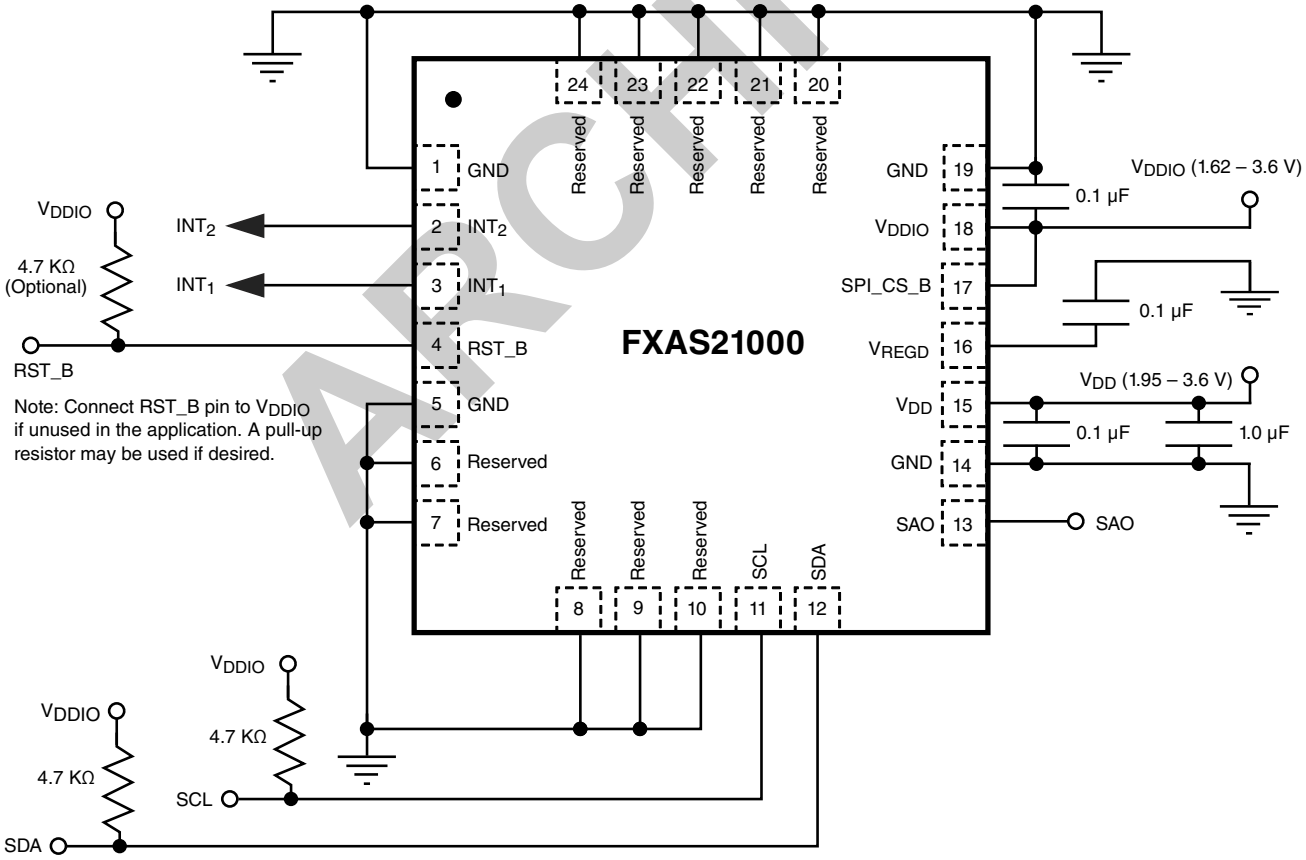


Figure 3. I^2C mode electrical connections

1.3.2 Typical Application Circuit—SPI Mode

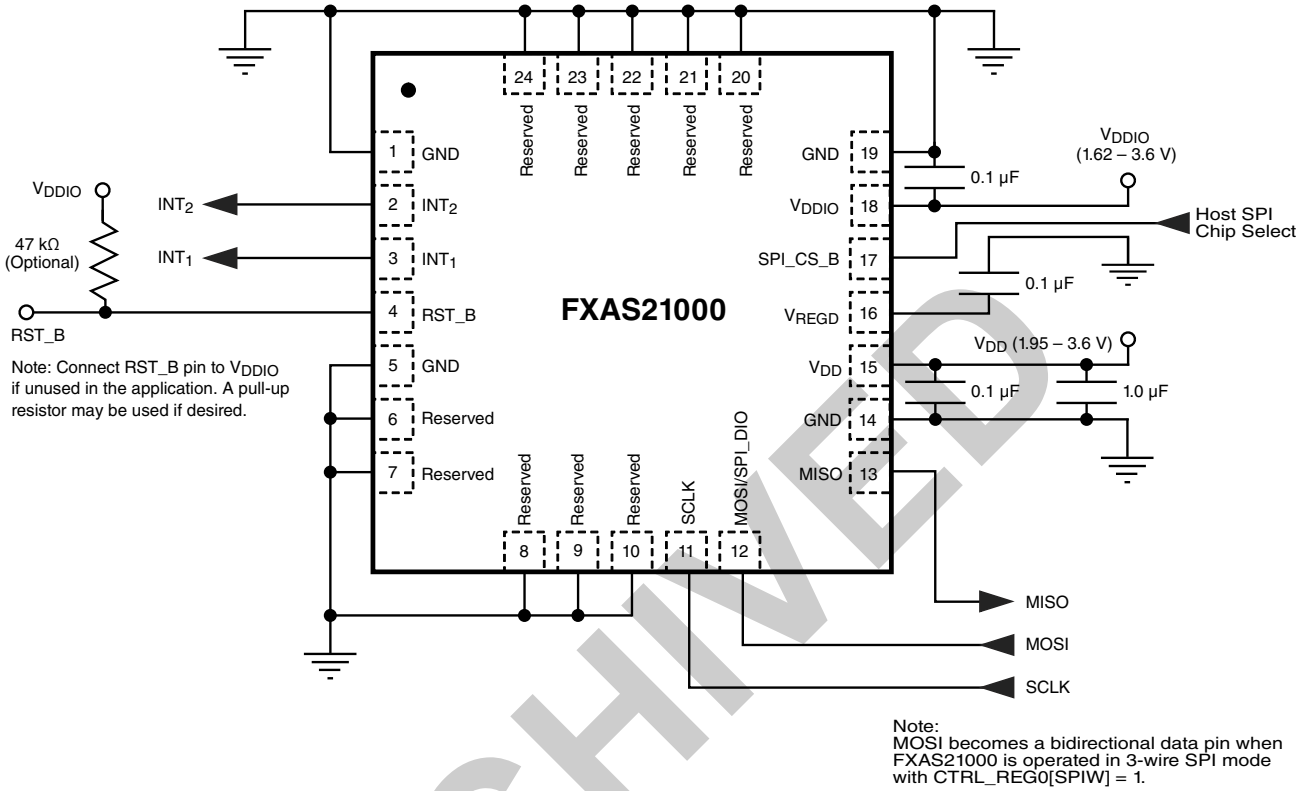


Figure 4. SPI mode electrical connections

1.4 Sensitive Axes Orientations and Polarities

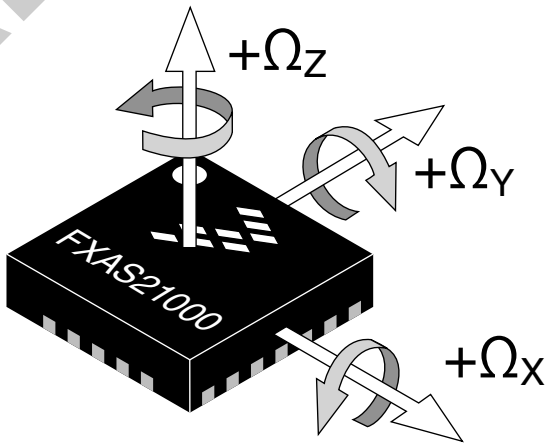


Figure 5. Reference frame for rotational measurement

2 Mechanical and Electrical Specifications

2.1 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either GND or V_{DD}).

Table 2. Absolute maximum ratings

Rating	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.6	V
Interface supply voltage	V_{DDIO}	–0.3	V_{DD} +0.3	V
Input voltage on any control pin (SA0, SCL, SDA)	V_{IN}	–0.3	V_{DDIO} +0.3	V
Maximum Acceleration (all axes, 100 µs)	g_{max}	—	5000	*g*
Operating temperature	T_{OP}	–40	+85	°C
Storage temperature	T_{STG}	–40	+125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model (HBM)	V_{HBM}	±2000	V
Machine model (MM)	V_{MM}	±200	V
Charge device model (CDM)	V_{CDM}	±500	V
Latch-up current at T = 85 °C	I_{LU}	±100	mA

Caution
This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

	Caution
	This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.2 Operating Conditions

Table 4. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.95	—	3.6	V
Digital supply voltage	V_{DDIO}	1.62	—	V_{DD} + 0.3	V
Digital high-level input voltage on SCL, SDA, SA0, I^2C, RST_B	VIH	0.7 * V_{DDIO}	—	—	V
Digital low-level input voltage on SCL, SDA, SA0, I^2C, RST_B	VIL	—	—	0.3 * V_{DDIO}	V
Operating temperature	T_{OP}	–40	+25	+85	°C

2.3 Mechanical Characteristics

Table 5. Mechanical characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Full-scale range	FS	FS = 00 FS = 01 FS = 10 FS = 11	—	±1600 ±800 ±400 ±200	—	dps
Sensitivity[1]	So	FS = 00 FS = 01 FS = 10 FS = 11	—	0.2 0.1 0.05 0.025	—	dps/LSB
Sensitivity change vs. temperature	TCS	–40 °C ≤ T ≤ 85 °C	—	±0.1	—	%/°C
Initial zero-rate offset	ZRO	Factory calibrated, before board mount	—	±100	—	dps
Zero-rate offset change vs. temperature	TCO	—	—	±0.3	—	dps/°C
Cross axis sensitivity	CAS	—	—	±1.5	—	%
Nonlinearity	NL	—	—	±1	—	%FS
Self-test output change	STOC	—	50	—	—	LSB

Table continues on the next page...

Table 5. Mechanical characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output data bandwidth	BW	—	—	ODR/2	—	Hz
Noise density	ND	ODR = 100 Hz	—	0.055	—	dps/√Hz
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V • T = 25 °C						

1. Sensitivity based on XYZ output data registers that are 14-bit left justified data

2.4 Electrical Characteristics

Table 6. Electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Current consumption	Idd_{Act}	Active Mode; Probe data on a trimmed oscillator and iref	—	5.8	—	mA
Supply current drain in Standby mode	Idd_{Stby}	Standby mode	—	2	—	µA
Supply current drain in Ready mode	Idd_{Rdy}	Ready mode	—	4.8	—	mA
High-level output voltage INT1, INT2	VOH	IO = 500 µA	0.9 * V_{DDIO}	—	—	V
Low-level output voltage INT1, INT2	VOL	IO = 500 µA	—	—	0.1 * V_{DDIO}	V
Low-level output voltage SDA	VOL_{SDA}	IO = 500 µA	—	—	0.1 * V_{DDIO}	V
Output data rate frequency tolerance	ODR_{TOL}	—	—	±2.5	—	% ODR
Signal bandwidth	BW	—	—	ODR/2	—	Hz
Boot time from POR/Reset to Standby mode	T_{boot}	—	—	16	—	µs
Turn-on time 1, Standby to Active mode transition	Ton1	—	—	2/ODR + 250	—	ms
Turn-on time 2, Ready to Active mode transition	Ton2	—	—	2/ODR + 10	—	ms
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V • T = 25°C						

2.5 Temperature Sensor Characteristics

Table 7. Temperature sensor characteristics

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full scale range	T_{FSR}	—	–40	—	+85	°C
Temperature Accuracy	—	25 °C	—	±1	—	°C
		Over Temperature Range	—	±3	—	
Operating Temperature	T_{OP}	—	–40	+25	+85	°C
Temperature sensor sensitivity	T_{SENS}	—	—	1	—	°C/LSB
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V						

3 Digital Interfaces

The registers embedded inside the FXAS21000 are accessed through either an I^2C or an SPI serial interface. To enable either interface, the V_{DDIO} line must be connected to the interface supply voltage. If V_{DD} is not present and V_{DDIO} is present, FXAS21000 is in shutdown mode and communications on the interface are ignored. If V_{DDIO} is maintained, V_{DD} can be powered off and the communications pins will be placed in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 8. Serial interface pin descriptions

Pin name	Pin description
V_{DDIO}	Digital interface power
I^2C/SPI_CS_B	I^2C/SPI interface mode selection and SPI chip select pin
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI/SPI_DIO	I^2C serial data/SPI master serial data out slave serial data in, SPI 3-wire data In/Out (in 3-wire SPI mode with **CTRL_REG0[**SPIW**]**=1)
SA0/MISO	I^2C least significant slave device address bit/SPI master serial data in slave serial data out

3.1 I^2C Interface

To use the I^2C interface, the I^2C/SPI_CS_B pin should be connected to V_{DDIO}. The implemented I^2C interface is compliant with the NXP I^2C-bus specification for Normal and Fast modes. The 7-bit slave addresses that may be assigned to the device

are 0x20 (with SA0 = 0) and 0x21 (with SA0 = 1). When I^2C/SPI_CS_B is high, the SA0/MISO pin is used to define the LSB of this I^2C address. The key timing constraints are shown in Table 9.

Table 9. Slave timing values

Parameter	Symbol	I^2C Standard Mode[1, 2]		I^2C Fast Mode[1, 2]		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	µs
Hold time (repeated) START condition	$t_{HD;STA}$	4	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	µs
Set-up time for a STOP condition	$t_{SU;STO}$	4	—	0.6	—	µs
SDA data-hold time[2]	$t_{HD;DAT}$	—	—	0.05	0.9[3]	µs
SDA valid time	$t_{VD;DAT}$	—	3.45	—	0.9[3]	µs
SDA valid acknowledge time[4]	$t_{VD;ACK}$	—	3.45	—	0.9[3]	µs
SDA setup time	$t_{SU;DAT}$	250	—	100[5]	—	ns
SCL clock low time	t_{LOW}	4.7	—	1.3	—	µs
SCL clock high time	t_{HIGH}	—	—	0.6	—	µs
SDA and SCL rise time	t_r	—	1000	$20+0.1C_b$[6]	300	ns
SDA and SCL fall time	t_f	—	300	$20+0.1C_b$[6]	300	ns
Pulse width of spikes on SDA and SCL that must be suppressed by the internal input filter	t_{SP}	—	50	—	50	ns

1. All values refer to VIH (min) and VIL (max) levels.
2. $t_{HD;DAT}$ is the data-hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
4. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. $t_{SU;DAT}$ = maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
6. C_b = total capacitance of one bus line in pF.

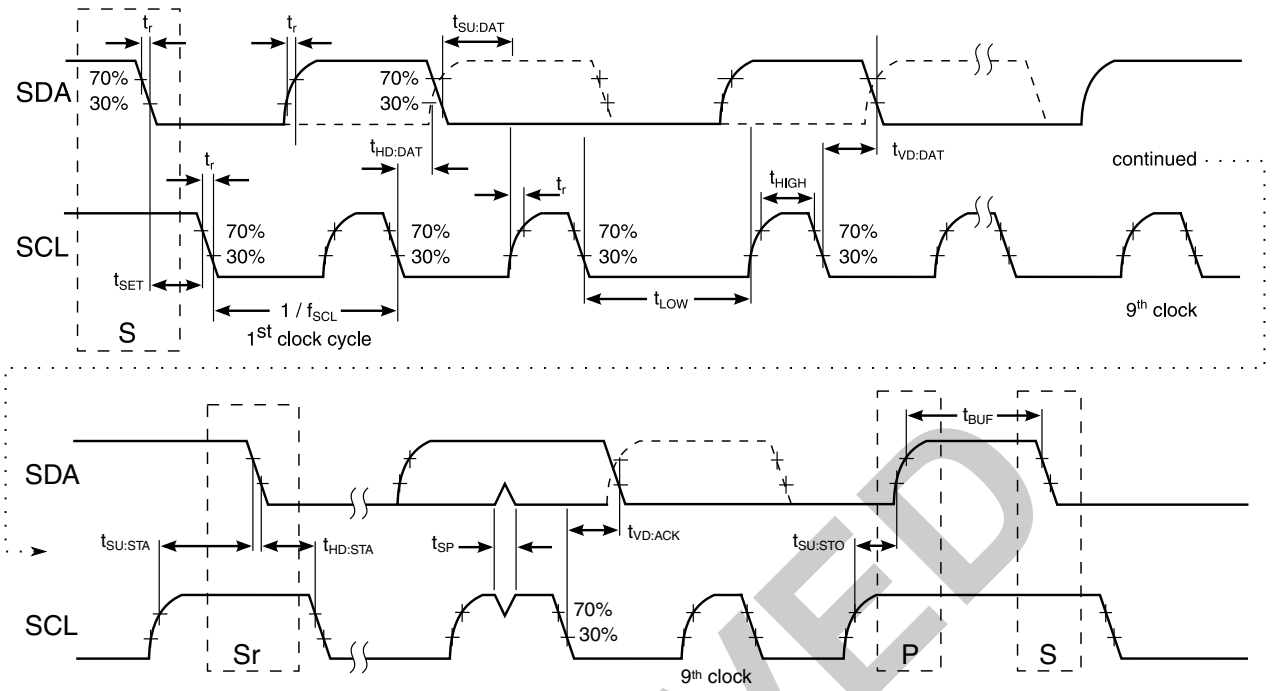


Figure 6. I²C timing diagram

3.1.1 I²C Operation

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The SDA is a bidirectional line used for sending and receiving the data to/from the interface. External pull-up resistors connected to V_{DDIO} are required for SDA and SCL. When the bus is free, both the lines are high. The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pull-up resistor values, and total bus capacitance (trace + device capacitance). For more information, see Table 10.

A transaction on the bus is started through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. Each device in the system compares the first seven bits after the ST condition with its own address. If the two addresses match, the device considers itself addressed by the master. The ninth clock pulse following the slave address byte (and each subsequent byte) is the acknowledge

(ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer continues only when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching, and not all master devices recognize clock stretching. The FXAS21000 does not support clock stretching.

A LOW-to-HIGH transition on the SDA line while SCL is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer.

Table 10. I²C Address Selection

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0100000 (0x20)	0100001 (0x21)	Factory Default

3.1.2 I²C Read Operations

3.1.2.1 Single-Byte Read

The master (or MCU) transmits an ST to the FXAS21000, followed by the slave address, with the R/W bit set to “0” for a write, and the FXAS21000 sends an acknowledgement. Then, the MCU transmits the address of the register to read and the FXAS21000 sends an acknowledgement. The MCU transmits an SR, followed by the byte containing the slave address and the R/W bit set to “1” for a read from the previously selected register. The FXAS21000 then acknowledges and transmits the data from the requested register. The master does not transmit a no acknowledge (NACK), but transmits an SP to end the data transfer.

3.1.2.2 Multiple-Byte Read

When performing a multiple-byte or burst read, the FXAS21000 increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXAS21000 ACK is received. This continues until a NACK occurs followed by an SP signaling an end of transmission.

3.1.3 I²C Write Operations

3.1.3.1 Single-Byte Write

To start a write command, the MCU transmits an ST to the FXAS21000, followed by the slave address with the R/W bit set to “0” for a write, and the FXAS21000 sends an ACK. Then, the MCU transmits the address of the register to write to, and the FXAS21000 sends an ACK. Then, the MCU transmits the 8-bit data to write to the designated register and the FXAS21000 sends an ACK that it has received the data. Since this transmission is complete, the master transmits an SP to end the data transfer. The data sent to the FXAS21000 is now stored in the appropriate register.

3.1.3.2 Multiple-Byte Write

The FXAS21000 automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXAS21000 ACK is received.

Command	Device Address Bit[6:1]	Device Address Bit[0] (SA0 pin state)	Device Address Bit[6:0]	R/W Bit	Address Byte Transmitted by Master
Read	6'b010000	0	0x20	1	0x41
Write	6'b010000	0	0x20	0	0x40
Read	6'b010000	1	0x21	1	0x43
Write	6'b010000	1	0x21	0	0x42

3.1.3.3 I²C Data Sequence Diagrams

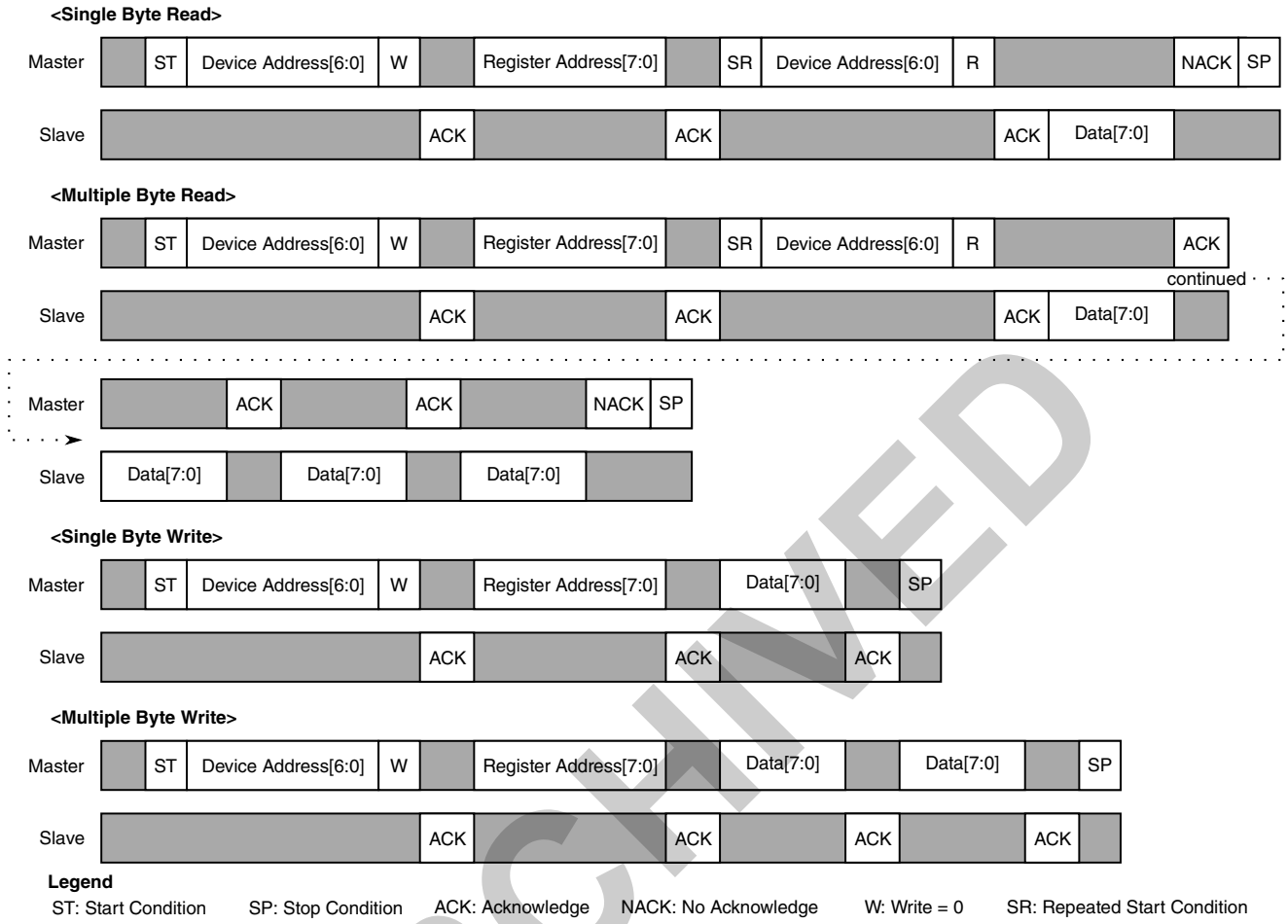


Figure 7. I²C data sequence diagram

3.2 General SPI Operation (4-Wire Mode)

The SPI_CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction, the master toggles the SPI clock (SCLK). The SCLK polarity is defined as having an idle value that is low and phase where data is captured on the clock's rising edge and propagated on the falling edge. [1] Single read and write operations are completed in 16 SCLK cycles or multiples of 8 cycles for multiple read/write operations. The first SCLK cycle uses the first bit on MOSI to determine whether the operation is a read (R/W = 1) or a write, such as R/W = 0. The following seven SCLK cycles are the slave register addresses. SCLK cycles and are present on the MOSI line. SCLK cycles nine through 16 are the data that is either read (present on MISO) or to be written (present on MOSI).

3.2.1 SPI Write (4-Wire Mode)

A write operation is initiated by transmitting a 0 for the R/W bit. Then, the 7-bit register address, ADDR[6:0](MSB first) is encoded in the first byte. Data to be written starts in the second serialized byte (MSB first). Figure 8 shows the bus protocol for the single write operation.

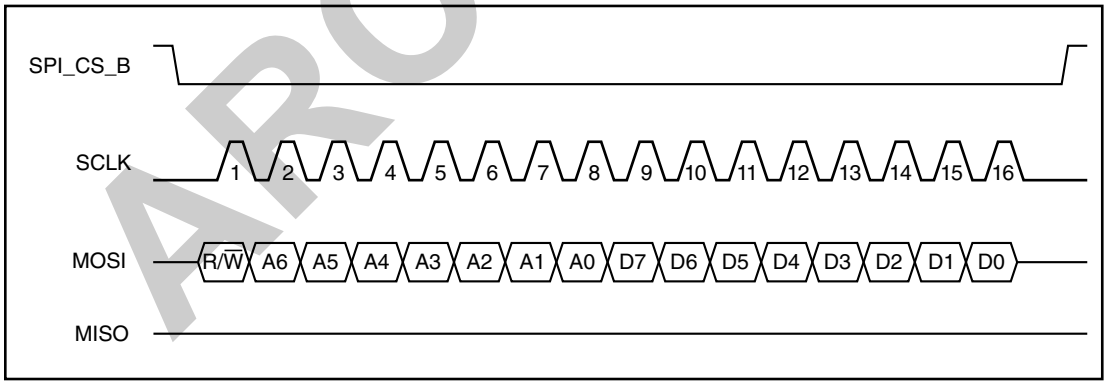


Figure 8. SPI single write operation. R/W = 1

Multiple write operations performed similar to the single write except bytes are written in multiples of eight SCLK cycles. The register address is auto incremented so that every eighth next clock edges will latch the MSB of the next register. When desired, the rising edge on SPI_CS_B stops the SPI communication.

1. From the Freescale SPI protocol definition, the polarity and phase settings are CPOL=0 and CPHA=0.

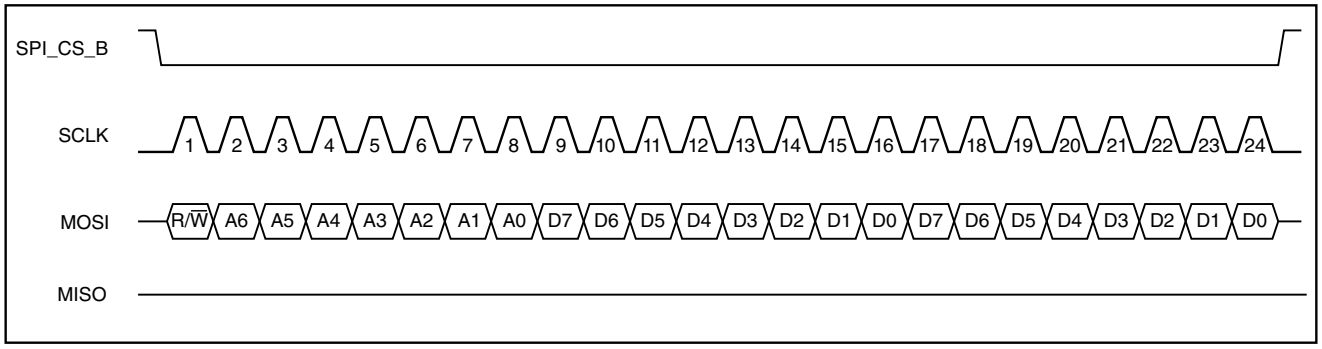


Figure 9. SPI multiple write operation showing 2 bytes written

3.2.2 SPI Single Read (4-Wire Mode)

NOTE

this description pertains only to the default SPI 4-wire interface mode (with CTRL_REG0[SPIW] = 0). This mode is the default out of POR, or after a hard/soft reset.

A register read operation is initiated by transmitting a 1 for the R/W bit. Then the 7-bit register read address, A[6:0] is encoded in the first byte. The data is read from the MISO pin (MSb first). Figure 10 shows the bus protocol for a single byte read operation.

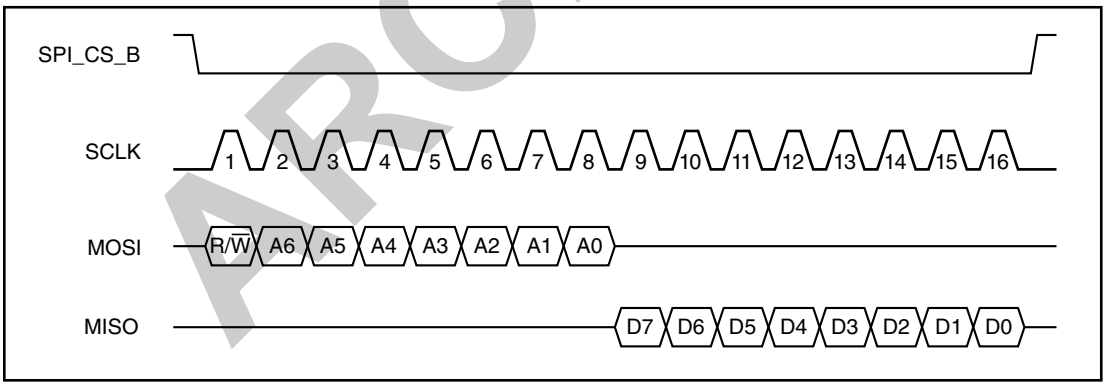


Figure 10. SPI single read operation. R/W = 1

Multi-byte read operations are performed similarly to single byte reads; additional bytes are read in multiples of eight SCLK cycles. The register read address is auto incremented by FXAS21002C so that every eighth clock edge will latch the address of the next register read address. When the desired number of bytes has been read, the rising edge on the SPI_CS_B terminates the transaction.

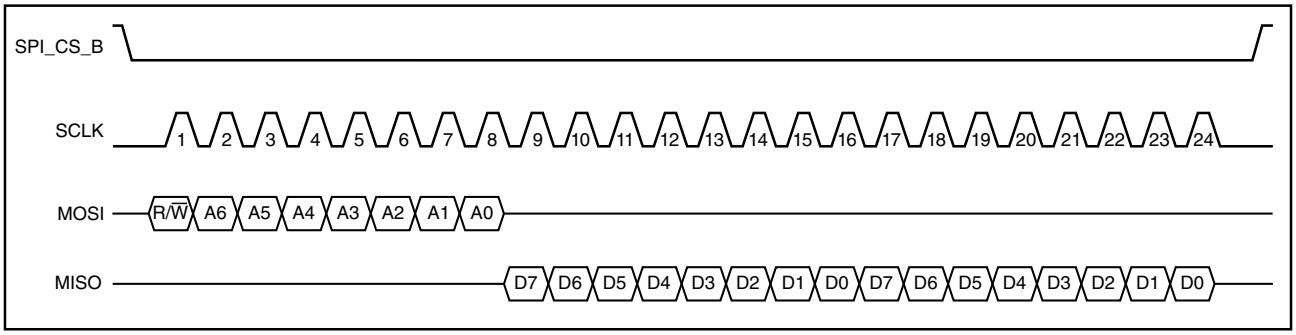


Figure 11. SPI multiple read operation showing 2 bytes written

3.2.3 SPI 3-Wire Mode

The FXAS21000CFXAS21000C can be configured to operate in 3-wire mode. In this mode the only signal pins used are SPI_CS_B, SCLK, and SPI_DIO; the MISO pin is not used. 3- wire mode is selected by setting the SPIW bit in CTRL_REG0.

Read operations in 3-Wire mode are different from read operations in 4-Wire mode.

- At the end of the address cycle of read operations in 3-Wire mode, the MOSI pin switches from SI to SO
- Multiple read operations in 3-wire mode use auto-increment
- Multiple read operations in 3-wire mode return data on the MOSI pin

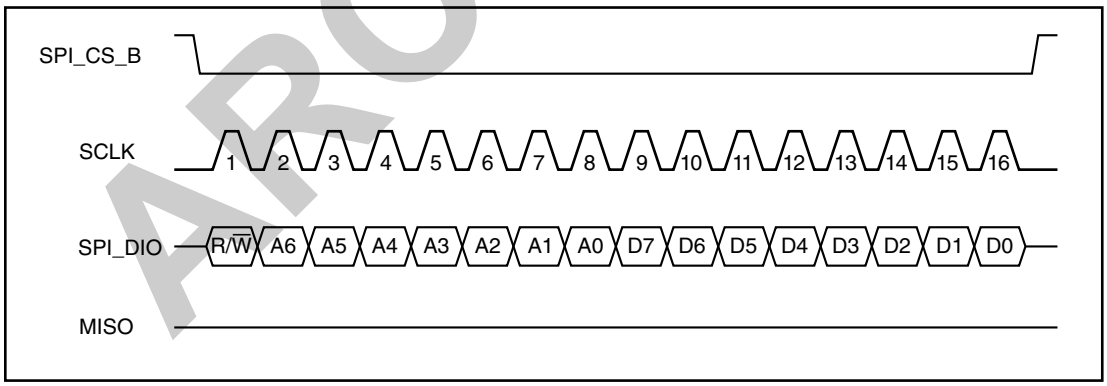


Figure 12. SPI 3-Wire single read operation

Write operations in 3-wire mode are identical to write operation in 4-wire mode since the MISO pin is not used in either mode of operation.

4 Modes of Operation

The device may be placed into one of three functional modes:

- **Standby:** Some digital blocks are enabled; I²C/SPI communication with FXAS21000CFXAS21000C is possible.
- **Active:** All blocks are enabled (digital and analog), the device is actively measuring the angular rate at the ODR specified in 0x13: CTRL_REG1.
- **Ready:** The drive circuits are running, but no measurements are being made.

The functional mode is selected using 0x13: CTRL_REG1. After a power-on-reset (POR) or triggered reset event (software or hardware pin), the device performs a boot sequence and loads the registers with their preset values, which are stored within the non-volatile memory (NVM).

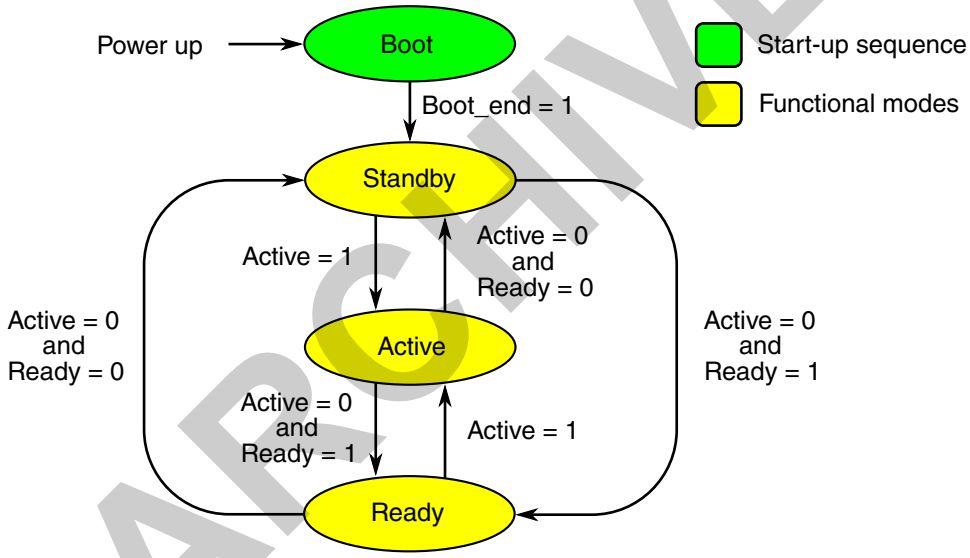


Figure 13. Functional mode diagram

5 Functionality

The FXAS21000 is a low-power, digital-output, 3-axis gyroscope with both I²C and SPI interfaces. The functionality includes the following:

- 14-bit output data is left justified in 2's complement format (big endian format)
- Configurable full scale ranges of ±200, ±400, ±800 and ±1600 dps
- Configurable output data rates from 1.5625 to 200 Hz

- Configurable high-pass filter cutoff frequency; Integrated Anti-Aliasing Filter (AAF) limits output data bandwidth to ODR/2
- Embedded rate threshold detection with programmable debounce timer
- 32-sample (X/Y/Z data at 14-bit) FIFO, configurable operating mode (Circular, Stop, Triggered)
- 2 external interrupt pins that are configurable to trigger on data-ready, rate threshold, or FIFO events
- Self-test function for indication of device health
- Single control bit for zero-rate offset compensation

Data for each axis must be read from the respective data registers two bytes at a time; for example, one byte for most significant byte and one byte for least significant. Combining these two bytes results in a 16-bit 2's complement signed integer with the sign bit in bit location #15 and the least significant bit in bit location #2. See the tables below.

Bit	**15**	14	13	12	11	10	9	8
Data bit	**D13**	D12	D11	D10	D9	D8	D7	D6
	Sign bit							

Bit	7	6	5	4	3	**2**	1	0
Data bit	D5	D4	D3	D2	D1	**D0**	X	X
						LSB		

The conversion from counts to a dps is done by first converting the 16-bit signed integer to 14-bit left-justified signed integer. This can be done by dividing the counts by four, or right shifting by two, then multiplying by the appropriate sensitivity value for the currently selected full-scale range. See Table 33 for nominal sensitivity values.

5.1 FIFO Data Buffer

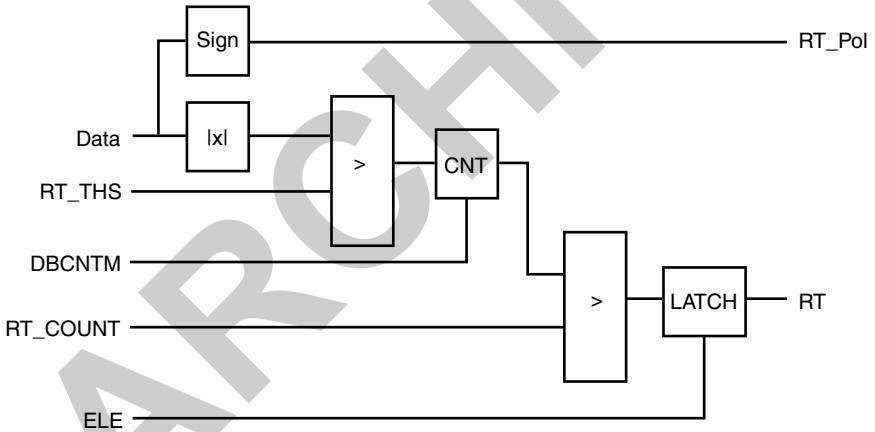
FXAS21000 contains a 32-sample FIFO data buffer that is useful for reducing the frequency of transactions on the I^2C/SPI bus. The FIFO can also provide system level power savings by allowing the host processor/MCU to go into a sleep/low-power mode while the FXAS21000 collects up to 32 samples of 3-axis angular rate data.

The FIFO can be configured to operate in Circular Buffer mode or Stop mode, depending on the settings made in the 0x09: F_SETUP register. The Circular Buffer mode allows the FIFO to be filled with a new sample replacing the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This is useful in situations where the processor is waiting for a specific interrupt to indicate that the data must be flushed to analyze the event.

The FXAS21000 FIFO Buffer has a configurable watermark, allowing an interrupt to be signaled to the processor after a configurable number of samples are stored in the buffer (from 1 to 32).

5.2 Rate Threshold Detection Function

The embedded rate detection function can be used to detect an angular rate event that exceeds a programmed threshold on any one of the enabled axes for longer than the programmed debounce time and to trigger an interrupt signal. The function is fully programmable, offering flexibility for the various potential use cases.



Output data rate (Hz)	Counter clock period (ms)	Event duration range
200	5	0 – 1.275
100	10	0 – 2.55
50	20	0 – 5.1
25	40	0 – 10.2
12.5	80	0 – 20.4

Table continues on the next page...

Output data rate (Hz)	Counter clock period (ms)	Event duration range
6.25	160	0 – 40.8
3.125	320	0 – 81
1.5625	640	0 – 163

The rate threshold (RT) event flag is set in the 0x0B: INT_SOURCE_FLAG register. It is cleared by reading the RT_SRC register. Using 0x14: CTRL_REG2, the device can be configured to generate an external interrupt on either the INT1 or INT2 pin when a rate threshold event condition occurs.

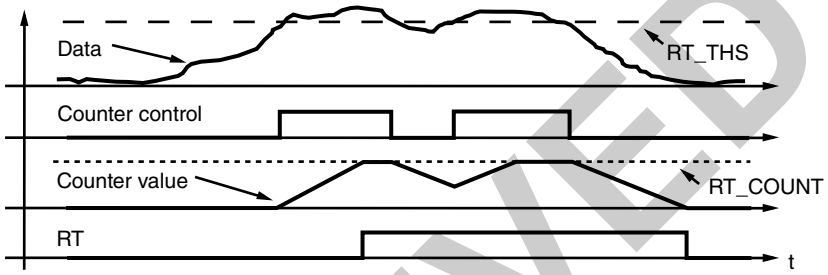


Figure 14. RT example 1

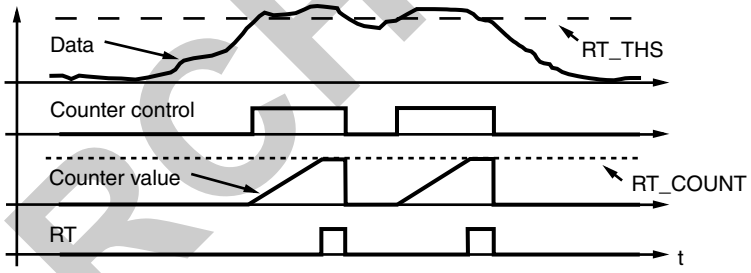


Figure 15. RT example 2

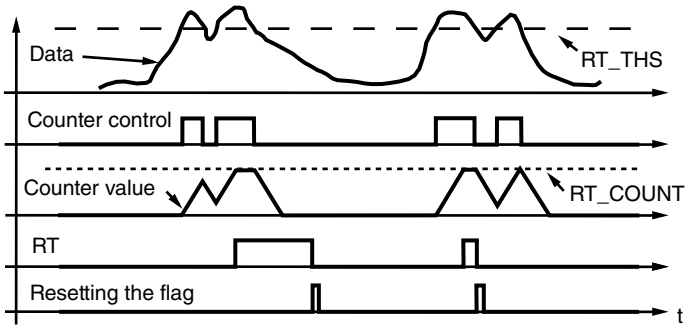


Figure 16. RT example 3

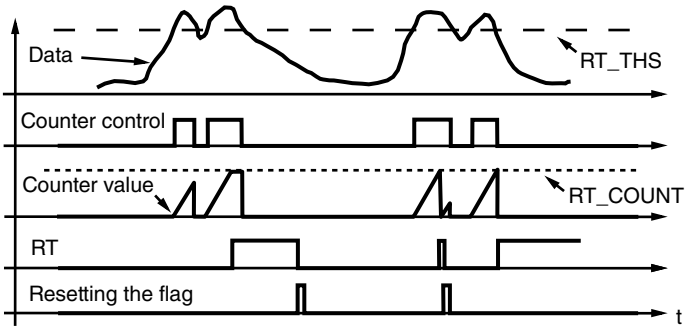


Figure 17. RT example 4

6 Register Descriptions

Table 12. Register address map

Name	Type	Register address	Default value	Comment
STATUS	R	0x00	0x00	Alias for DR_STATUS or F_STATUS
OUT_X_MSB	R	0x01	0x00	14-bit X-axis measurement data bits 13:6
OUT_X_LSB	R	0x02	0x00	14-bit X-axis measurement data bits 5:0
OUT_Y _MSB	R	0x03	0x00	14-bit Y-axis measurement data bits 13:6
OUT_Y_LSB	R	0x04	0x00	14-bit Y-axis measurement data bits 5:0
OUT_Z_MSB	R	0x05	0x00	14-bit Z-axis measurement data bits 13:6
OUT_Z_LSB	R	0x06	0x00	14-bit Z-axis measurement data bits 5:0
DR_STATUS	R	0x07	0x00	Data-ready status information
F_STATUS	R	0x08	0x00	FIFO Status
F_SETUP	R/W	0x09	0x00	FIFO setup
F_EVENT	R	0x0A	—	FIFO event
INT_SRC_FLAG	R	0x0B	—	Interrupt event source status flags
WHO_AM_I	R	0x0C	0xD1	Device ID
CTRL_REG0	R/W	0x0D	0x00	Control register 0: Full-scale range selection, high-pass filter setting, SPI mode selection
RT_CFG	R/W	0x0E	0x00	Rate threshold function configuration
RT_SRC	R	0x0F	0x00	Rate threshold event flags status register
RT_THS	R/W	0x10	0x00	Rate threshold function threshold register
RT_COUNT	R/W	0x11	0x01	Rate threshold function debounce counter
TEMP	R	0x12	0x00	Device temperature in °C
CTRL_REG1	R/W	0x13	0x00	Control register 1: Operating mode, ODR selection, self-test and soft reset
CTRL_REG2	R/W	0x14	0x00	Control register 2: Interrupt configuration settings

6.1 0x00: STATUS

The STATUS register content depends on the FIFO mode setting. It is a copy of either 0x07: DR_STATUS or 0x08: F_STATUS. This allows for easy reading of the relevant status register before reading the current sample output data, or the first sample stored in the FIFO.

6.2 0x01–0x06: OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB

X-, Y-, and Z-axis sample data are represented in 14-bit, 2's complement format. The output data registers are either updated at the output data rate (F_MODE = 00) or alternately point to the first sample stored in the FIFO buffer (F_MODE > 00). The FIFO read pointer is incremented whenever the Z-axis data is read. Using the burst-read mode, the data is read in the following order: OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB and then OUT_Z_LSB.

NOTE

To avoid the loss of data, the user must burst-read all six bytes of sample data (three axes) in a single I2C or SPI transaction.

NOTE

Data output LSB registers only contain valid data after a read of the corresponding axis MSB data register. When F_SETUP[F_MODE] > 0b00, a data read operation must start by reading the OUT_X_MSB register in order for the contents of the other output data registers to be updated for the currently indexed buffered sample. With F_SETUP[F_MODE] > 0b00, the OUT_Z_MSB register must also be read in order to advance the internal buffer read pointer to index the next sample stored in the FIFO.

NOTE

The two least significant bits of each axis's data LSB are not used. Data must be right shifted by two bits (or divided by 4) in the user application to obtain a properly scaled 16-bit 2's complement rate value.

NOTE

After OUT_Z_LSB is read, the next read register by the auto-increment process is STATUS at 0x00.

Table 13. OUT_X_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	XD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 14. OUT_X_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	XD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

Table 15. OUT_Y_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	YD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 16. OUT_Y_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	YD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

Table 17. OUT_Z_MSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	ZD[13:6]							
Write								
Reset	0	0	0	0	0	0	0	0

Table 18. OUT_Z_LSB register (default value 0x00)

Bit	7	6	5	4	3	2	1	0
Read	ZD[5:0]						0	0
Write								
Reset	0	0	0	0	0	0	0	0

6.3 0x07: DR_STATUS

The DR_STATUS register provides the sample data acquisition status and reflects the real-time updates to the OUT_X, OUT_Y, and OUT_Z registers. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 19. DR_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
Write								
Reset	0	0	0	0	0	0	0	0

Table 20. DR_STATUS field descriptions

Field	Description
7 ZYXOW	X-, Y-, Z-axis data overwrite • Asserted whenever new X-, Y-, and Z-axis data is acquired before completing the retrieval of the previous set. • Cleared after the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read. 0: No data overwrite has occurred 1: X, Y, and Z data overwrite occurred before the previous data was read
6 ZOW	Z-axis data overwrite • Asserted whenever a new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: Z-axis data overwrite occurred before the previous data was read

Table continues on the next page...

Table 20. DR_STATUS field descriptions (continued)

Field	Description
5 YOW	Y-axis data overwrite • Asserted whenever a new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: Y-axis data overwrite occurred before the previous data was read
4 XOW	X-axis data overwrite • Asserted whenever a new X-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: X-axis data overwrite occurred before the previous data was read
3 ZYXDR	X-, Y-, and Z-axis data available • Signals that a new acquisition for any of the channels is available. • Cleared when the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read. 0: No new data is ready 1: New data is ready
2 ZDR	Z-axis new data available • Asserted whenever a new Z-axis data acquisition is completed. • Cleared anytime the OUT_Z_MSB register is read. 0: No new Z-axis data is ready 1: New Z-axis data is ready
1 YDR	Y-axis new data available • Asserted whenever a new Y-axis data acquisition is completed. • Cleared anytime the OUT_Y_MSB register is read. 0: No new Y-axis data is ready 1: New Y-axis data is ready
0 XDR	X-axis new data available • Asserted whenever a new X-axis data acquisition is completed. • Cleared anytime the OUT_X_MSB register is read. 0: No new X-axis data is ready 1: New X-axis data is ready

6.4 0x08: F_STATUS

Indicates the current status of the FIFO, when the FIFO is enabled.

When the FIFO is enabled, the STATUS register (address 0x00) also contains the same content as this register to facilitate the emptying of the FIFO by the host processor. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes. The SRC_FIFO bit in the 0x0B: INT_SOURCE_FLAG register is cleared when F_STATUS is read.

Table 21. F_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	F_OVF	F_WMKF	F_CNT[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 22. F_Status field descriptions

Field	Description
7 F_OVF	FIFO overflow flag • A FIFO overflow event, such as when F_CNT = 32 and a new sample arrives, asserts the F_OVF flag. • Cleared when this register is read. 0: No overflow detected 1: Overflow detected
6 F_WMKF	FIFO watermark flag • A FIFO sample count greater than or equal to the sample count watermark (determined by the F_WMRK field in register 0x09: F_SETUP) asserts the F_WMKF event flag. • Disabling the FIFO clears the F_WMKF • Cleared when this register is read. 0: No watermark detected 1: Watermark detected
5:0 F_CNT	FIFO sample counter • Indicates the number of samples currently stored in the FIFO. • A count value of 0b000000 indicates that the FIFO is empty.

6.5 0x09: F_SETUP

The F_SETUP register is used to configure the FIFO. The FIFO update rate is set by the selected system ODR (DR bits in 0x13: CTRL_REG1).

Table 23. F_Setup register

Bit	7	6	5	4	3	2	1	0
Read	F_MODE[1:0]		F_WMRK[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 24. F_SETUP field descriptions

Field	Description
7:6 F_MODE	Selects the FIFO operating mode • In the Circular Buffer mode, the oldest sample is discarded and replaced by the newest sample when the buffer is full (**F_STATUS[**F_CNT**]** = 32). • In the Stop mode, the FIFO will stop accepting new samples when the buffer is full (**F_STATUS[**F_CNT**]** = 32). • The FIFO operating mode cannot be switched between Circular and Stop modes while the FIFO is enabled. • To change the FIFO operating mode, the FIFO function must first be disabled by setting F_MODE[1:0] = 00. • Disabling the FIFO clears the FIFO. 00: FIFO is disabled 01: Circular Buffer mode 1x: Stop mode
5:0 F_WMRK	FIFO sample count watermark setting • Used to set the watermark level. • A FIFO sample count exceeding the watermark level does not stop the FIFO from accepting new data. • To suppress FIFO watermark event flag generation, F_WMRK[5:0] can be set to 0x00. Default value is 0b000000.

6.6 0x0A: F_EVENT

The F_EVENT register is used to monitor the system state and FIFO event status. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 25. F_Event register

Bit	7	6	5	4	3	2	1	0
Read	0	0	F_EVENT	FE_TIME[4:0]				
Write								
Reset	0	0	0	0	0	0	0	0

Table 26. F_EVENT field descriptions

Field	Description
5 F_EVENT	FIFO Event • Indicates if either F_WMKF or F_OVF flags are set (logical OR). • The F_STATUS register must be read to determine which event(s) occurred. 0: FIFO Event not detected 1: FIFO Event was detected
4:0 FE_TIME	Number of ODR periods elapsed since F_EVENT was set • indicates the number of samples acquired since a FIFO event flag (overflow or watermark) was asserted. • Reset when 0x08: F_STATUS is read.

6.7 0x0B: INT_SOURCE_FLAG

The INT_SOURCE_FLAG register provides the event-flag status for the functions within the device. Reading the INT_SRC_FLAG register does not reset any event-flag source bits; they are reset by reading the appropriate event source register. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 27. INT_SRC register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	BOOTEND	SRC_FIFO	SRC_RT	SRC_DRDY
Write								
Reset	0	0	0	0	0	0	0	0

Table 28. INT_SRC_FLAG field descriptions

Field	Description
3 BOOTEND	Boot sequence complete event flag • Asserted as soon as the device boot sequence has completed. 1: Boot sequence is complete 0: Boot sequence is not complete
2 SRC_FIFO	FIFO event source flag • Indicates that the FIFO triggered the interrupt • Cleared by reading the register 1: F_OVF or F_WMKF are set, provided the FIFO interrupt is enabled (**CTRL_REG2[**INT_EN_FIFO=1**]**) 0: Cleared by reading the register
1 SRC_RT	Rate threshold event source flag • Indicates that the rate threshold event flag triggered the interrupt • Cleared by reading RT_SRC register
0 SRC_DRDY	Data ready event source flag • Asserted whenever a data-ready event triggers the interrupt • Cleared whenever the MSB's of the X, Y, and Z axes sample data are read • Cleared by reading the MSB's of the X, Y, and Z axes sample data

6.8 0x0C: WHO_AM_I

The WHO_AM_I register contains the device identifier which is factory programmed to 0xD1.

Table 29. WHO_AM_I

Bit	7	6	5	4	3	2	1	0
Read	1	1	0	1	0	0	0	1
Write								
Reset	1	1	0	1	0	0	0	1

6.9 0x0D: CTRL_REG0

CTRL_REG0 is used for general control and configuration of the device. The bit fields in CTRL_REG0 should be changed only in Standby or Ready modes. Accuracy of the output data is not guaranteed if these bits are changed when the device is in Active mode.

Table 30. CTRL_REG0

Bit	7	6	5	4	3	2	1	0
Read Write	0	0	SPIW	SEL[1:0]		HPF_EN	FS[1:0]	
Reset	0	0	0	0	0	0	0	0

Table 31. CTRL_REG0 field descriptions

Field	Description
5 SPIW	SPI interface mode selection • The contents should only be modified when the device is in Standby mode 0: SPI 4-wire mode (default) 1: SPI 3-wire mode (MOSI is used for IN/OUT signals)
4:3 SEL	High-pass filter cutoff frequency selection • Details of the high-pass filter settings are shown in Table 32.
2 HPF_EN	High-pass filter enable • The high-pass filter is initialized on mode change, ODR change, and assertion of the ZR_COND bit. • When enabled, the HPF is applied to the angular rate data supplied to the output registers/FIFO and the embedded rate threshold algorithm. 0: High-pass filter disabled (default) 1: High-pass filter enabled
1:0 FS	Full-scale range selection • See Table 33

Table 32. High-pass filter cutoff frequency selection

SEL1	SEL0	Cutoff Frequency in Hz versus ODR							
		200 Hz	100 Hz	50 Hz	25 Hz	12.5 Hz	6.25 Hz	3.15 Hz	1.5625 Hz
0	0	3.75	1.875	0.937	0.468	0234	0.12	0.06	0.03
0	1	1.925	0.963	0.481	0.241	0.120	0.06	0.03	0.015
1	0	0.975	0.488	0.244	0.122	0.061	0.03	0.015	0.008
1	1	0.495	0.248	0.124	0.062	0.031	0.015	0.008	0.004

Table 33. Selectable Full Scale Ranges

FS1	FS0	Range (dps)	Nominal Sensitivity (dps/LSB)
0	0	±1600	0.2
0	1	±800	0.1

Table continues on the next page...

Table 33. Selectable Full Scale Ranges (continued)

FS1	FS0	Range (dps)	Nominal Sensitivity (dps/LSB)
1	0	±400	0.05
1	1	±200	0.025

6.10 0x0E: RT_CFG

The RT_CFG register is used to enable the Rate Threshold interrupt generation.

Table 34. RT_ CFG Register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	ELE	ZTEFE	YTEFE	XTEFE
Write								
Reset	0	0	0	0	0	0	0	0

Table 35. RT_CFG field descriptions

Field	Description
3 ELE	Event latch enable Enables a latch event • See Modes of Operation for more details. • The internal state of the Rate Threshold function is reset when a transition from Standby to Active or Ready to Active modes occurs. • The contents should only be modified when the device is in Standby mode 0: Event flag latch disabled 1: Event flag latch enabled
2 ZTEFE	Event flag enable on Z axis • Enable bits for rate threshold event detection on the Z axis 0: Z event detection disabled 1: Z event detection enabled
1 YTEFE	Event flag enable on Y axis • Enable bits for rate threshold event detection on the Y axis 0: Y event detection disabled 1: Y event detection enabled
0 XTEFE	Event flag enable on X axis • Enable bits for rate threshold event detection on the X axis 0: X event detection disabled 1: X event detection enabled

6.11 0x0F: RT_SRC

This register indicates the source of the Rate Threshold event. It also clears the RT_SRC flag in the 0x0B: INT_SOURCE_FLAG register.

Table 36. RT_ SRC Register

Bit	7	6	5	4	3	2	1	0
Read	0	EA	ZRT	Z_RT_Pol	YRT	Y_RT_Pol	XRT	X_RT_Pol
Write								
Reset	0	0	0	0	0	0	0	0

Table 37. RT_SRC field descriptions

Field	Description
6 EA	Event active flag • Asserted whenever a rate threshold event has been detected on one or more of the enabled axes. • The contents should only be modified when the device is in Standby mode • The internal state of the Rate Threshold function is reset when a transition from Standby to Active or Ready to Active modes occurs. • It is upon reading this register when **RT_CFG[**ELE**]** = 1, or self-cleared by the function when the condition is no longer true with RT_CFG[ELE] = 0. 0: No event flags have been asserted 1: One or more event flags have been asserted
5 ZRT	Z rate event • Indicates that a rate threshold event (as defined in Modes of Operation) has been detected on the Z axis • Cleared when read if it has been latched (ELE = 1). 0: Z rate lower than RT_THS value 1: Z rate greater than RT_THS event has occurred
4 Z_RT_Pol	Polarity of Z event • Indicates the rate polarity for the event detected on the Z axis 0: Z rate event was Positive 1: Z rate event was Negative
3 YRT	Y rate event • Indicates that a rate threshold event (as defined in Modes of Operation) has been detected on the Y axis • Cleared when read if it has been latched (ELE = 1). 0: Y rate lower than RT_THS value 1: Y rate greater than RT_THS value event has occurred

Table continues on the next page...

Table 37. RT_SRC field descriptions (continued)

Field	Description
2 Y_RT_Pol	Polarity of Y event • Indicates the rate polarity for the event detected on the Y axis 0: Y rate event was Positive 1: Y rate event was Negative
1 XRT	X rate Event • Indicates that a rate threshold event (as defined in Modes of Operation) has been detected on the X axis • Cleared when read if it has been latched (ELE = 1). 0: X rate lower than RT_THS value 1: X rate greater than RT_THS value event has occurred
0 X_RT_Pol	Polarity of X event • Indicates the rate polarity for the event detected on the X axis 0: X rate event was positive 1: X rate event was negative

6.12 0x10: RT_THS

The RT_THS register sets the threshold limit for the detection of the rate and the debounce counter mode. See Modes of Operation for more details.

Table 38. RT_THS register

Bit	7	6	5	4	3	2	1	0
Read Write	DBCNTM	THS[6:0]						
Reset	0	0	0	0	0	0	0	0

Table 39. RT_THS field descriptions

Field	Description
7 DBCNTM	Debounce counter mode selection • The contents should only be modified when the device is in Standby mode 1: Clear counter when angular rate is below threshold value 0: Decrement counter when angular rate is below threshold value

Table continues on the next page...

Table 39. RT_THS field descriptions (continued)

Field	Description
6:0 THS	Unsigned 7-bit rate threshold value • The contents should only be modified when the device is in Standby mode • The internal state of the Rate Threshold function is reset when a transition from Standby to Active or Ready to Active modes occurs. • The rate threshold in dps is given by the following formula: $Rate\_threshold = THS * \frac{Full\_scale}{128}$

6.13 0x11: RT_COUNT

RT_COUNT sets the number of debounce counts. See Modes of Operation for more details.

Table 40. RT_COUNT register

Bit	7	6	5	4	3	2	1	0
Read	D[7:0]							
Write								
Reset	0	0	0	0	0	0	0	1

Table 41. RT_COUNT field descriptions

Field	Description
7:0 D	Debounce counter value • The contents should only be modified when the device is in Standby mode • A transition from Standby to Active or Ready to Active modes resets the internal state of the Rate Threshold function. • Stores the number of counts with the angular rate above the threshold needed before asserting the rate threshold event flag • The counter period is the same as the selected ODR period, allowing for a debounce time to be calculated. For example, an RT_COUNT value of 10 (decimal) and an ODR of 100 Hz would result in a debounce time of 100 ms.

6.14 0x12: TEMP

The TEMP register contains an 8-bit 2's complement temperature value with a range of –128 °C to +127 °C, with a scaling of 1 °C/LSB. This register is reset only by a hard reset event (POR/RST_B pin assertion); a soft reset, such as setting **CTRL_REG1**[RST] = 1, will not reset the contents of this register. The temperature data is only compensated when the device is operating in the Active mode.

Table 42. TEMP register

Bit	7	6	5	4	3	2	1	0
Read	Temp[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

6.15 0x13: CTRL_REG1

The CTRL_REG1 register is used to configure the device ODR, set the operating mode, and exercise the self-test and zero-rate offset adjustment functions.

NOTE

Control bits in CTRL_REG1 should be changed only in Standby or Ready mode. Accuracy of the data is not guaranteed if these bits are changed when the device is in Active mode.

Table 43. CTRL_REG1 register

Bit	7	6	5	4	3	2	1	0
Read	ZR_cond	RST	ST	DR[2:0]			Active	Ready
Write								
Reset	0	0	0	0	0	0	0	0

Table 44. CTRL_REG1 field descriptions

Field	Description
7 ZR_cond[1]	Zero-rate condition • Used to trigger the offset compensation. For this reason, it is meant to be used only when the device is in zero rate condition on all axes. • Writing a *1* to this bit initiates the internal zero-rate offset calibration. • Self-clears after the zero-rate offset calculation, and it can only be used once after a hard or soft reset has occurred. In order to use the ZR_cond a second time, the device has to be reset either with a hard or soft reset.
6 RST	Software Reset • Causes a synchronous reset of the device. • On reset, all registers revert to their default values. • Self cleared after assertion. 0: Device reset not triggered/completed 1: Device reset triggered

Table continues on the next page...

Table 44. CTRL_REG1 field descriptions (continued)

Field	Description
5 ST	Self-test enable • Activates the self-test function. • When ST is set, a data output change will occur even if no angular rate is applied. This allows the host application to check the functionality of the sensor and the entire measurement signal chain. 0: self test disabled 1: self test enabled
4:2 DR	Output Data Rate selection • Selects the output data rate as per Table 45
1 Active	Standby/Active mode selection
0 Ready	Standby/Ready mode selection

1. ZR_cond may be written only after the first rate sample is available, as it uses the current sample for calibration. ZR_cond should not be used when the HPF is enabled.

Table 45. Output data rate selection

DR2	DR1	DR0	ODR (Hz)	Period (ms)
0	0	0	200.0	5
0	0	1	100.0	10
0	1	0	50.0	20
0	1	1	25	40
1	0	0	12.5	80
1	0	1	6.25	160
1	1	0	3.125	320
1	1	1	1.5625	640

The Active and Ready bits are used to set the device operating mode. In Standby mode, the device is only capable of digital communication over the I^2C or SPI interfaces. In Ready mode, the device is ready to measure but no sample acquisition is performed. This state is useful for reducing the power consumption of the device while also allowing for a fast transition to the Active mode. In Active mode, the device is fully functional. The Active bit has higher priority than the Ready bit as per Table 46.

Table 46. Device mode

Active	Ready	Device mode
0	0	Standby
0	1	Ready
1	x	Active

6.16 0x14: CTRL_REG2

This register enables and assigns the output pin(s) and logic polarities for the various interrupt sources available on the device.

Table 47. CTRL_REG2 register

Bit	7	6	5	4	3	2	1	0
Read Write	INT_CFG_FIFO	INT_EN_FIFO	INT_CFG_RT	INT_EN _RT	INT_CFG_DRDY	INT_EN_DRDY	IPOL	PP_OD
Reset	0	0	0	0	0	0	0	0

Table 48. Interrupt Enable register descriptions

Register	Description
7 INT_CFG_FIFO	FIFO interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
6 INT_EN_FIFO	FIFO Interrupt Enable 0: FIFO interrupt disabled 1: FIFO interrupt enabled
5 INT_CFG_RT	Rate threshold interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
4 INT_EN_RT	Rate threshold interrupt enable 0: Rate threshold interrupt disabled 1: Rate threshold interrupt enabled
3 INT_CFG_DRDY	Data-ready interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin

Table continues on the next page...

Table 48. Interrupt Enable register descriptions (continued)

Register	Description
2 INT_EN_DRDY	Data ready interrupt enable 0: Data-ready interrupt disabled 1: Data-ready interrupt enabled
1 IPOL	Interrupt logic polarity 0: Active low 1: Active high
0 PP_OD	INT1 and INT2 pin output driver configuration 0: Push-pull output driver 1: Open-drain output driver

Table 49. INT pin behavior as a function of PP_OD and IPOL bit settings

INT pin configuration	PP_OD	IPOL	INT asserted value	INT deasserted value
CMOS output	0	0	0	1
CMOS output	0	1	1	0
External pull-up resistor added	1	0	0	high-z[1]
External pull-down resistor added	1	1	1	high-z[1]

1. High-z = tri-state (high impedance) condition; the state of the INT pin will be defined by the external pull-up or pull-down resistor.

7 Printed Circuit Board Layout and Device Mounting

Printed Circuit Board (PCB) layout and device mounting are critical to the overall performance of the design. The footprint for the surface mount packages must be the correct size as a base for a proper solder connection between the PCB and the package. This, along with the recommended soldering materials and techniques, will optimize assembly and minimize the stress on the package after board mounting.

Freescale application note AN1902, "Assembly Guidelines for QFN and DFN Packages" discusses the QFN package used by the FXAS21000CFXAS21000C.

7.1 Printed Circuit Board Layout

The following recommendations are meant to serve as general guidelines for realizing an effective PCB layout. See Figure 18 for component PCB footprint dimensions.

- The PCB land pattern should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 18.
- On the layer that the device is soldered, there should be no trace routing or vias underneath the device's component package.
- No components or vias should be placed at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on the NC pads in order to have same length of exposed trace for all pads.
- No copper traces should be on the top layer of the PCB under the package. This will cause planarity issues with board mount. Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

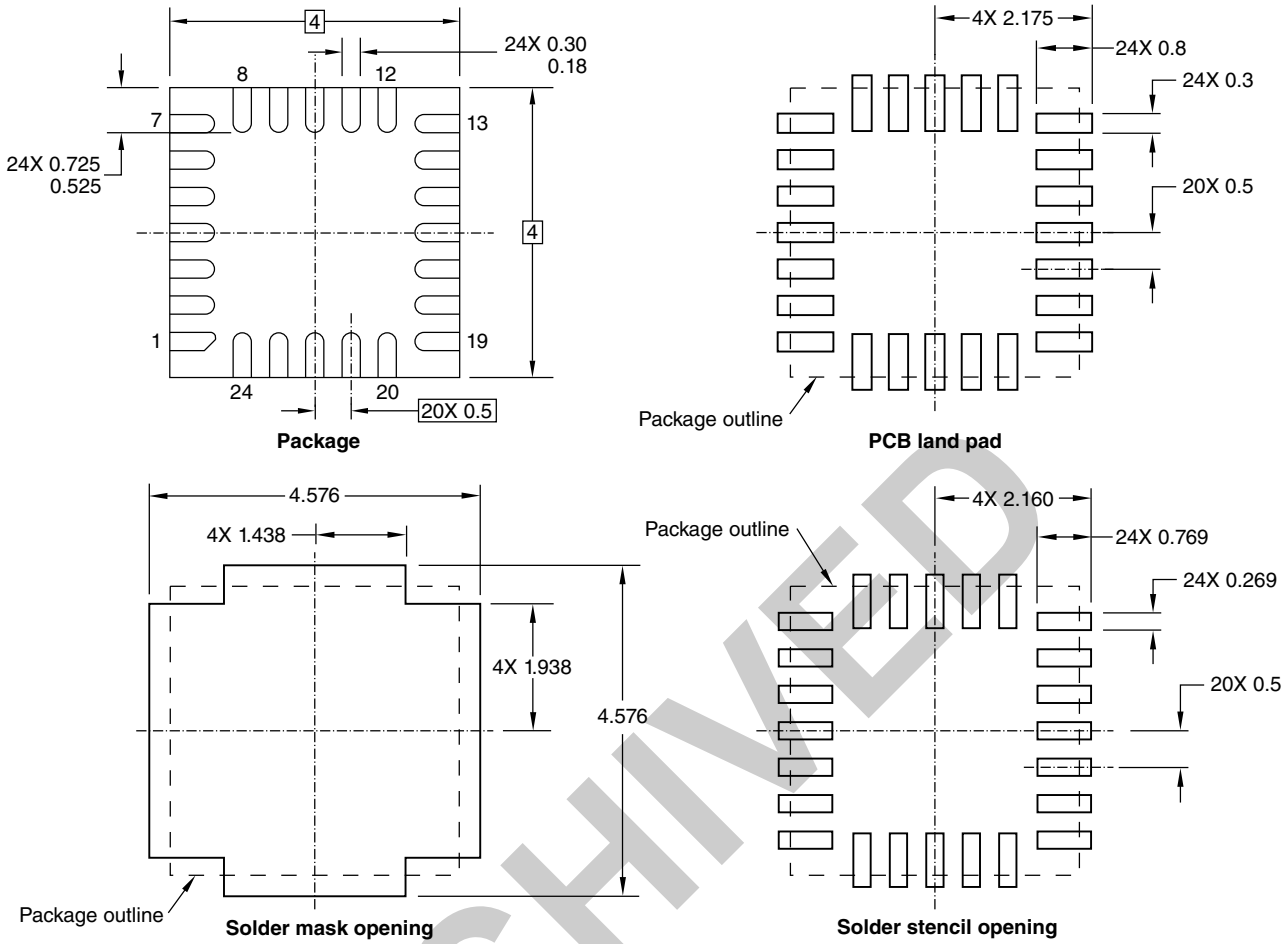


Figure 18. Footprint

7.2 Overview of Soldering Considerations

The information provided here is based on experiments executed on QFN devices. These experiments cannot represent exact conditions present at a customer site. Therefore, information herein should be used for guidance purposes only. Process and design optimizations are recommended to develop an application-specific solution. With the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

- Stencil thickness should be 100 or 125 µm.
- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.

- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Do not use a screw-down or stacking to mount the PCB into an enclosure. These methods could bend the PCB, which would put stress on the package.

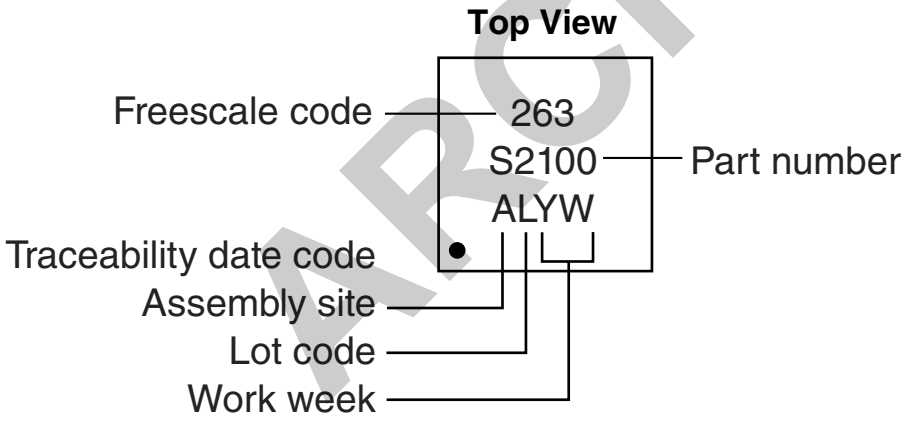
7.3 Halogen Content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembled package will contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

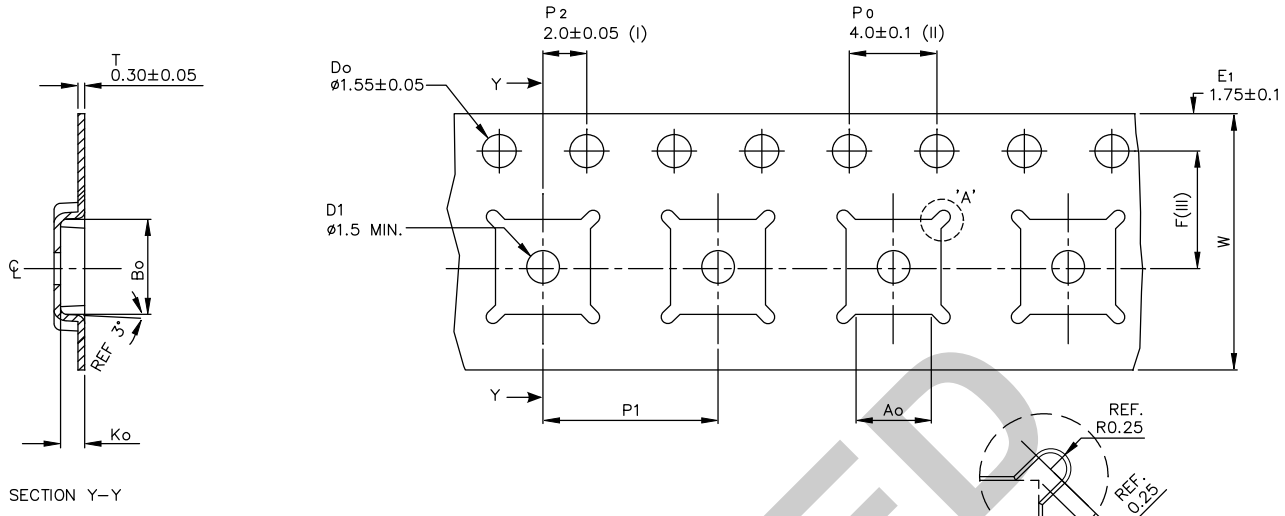
8 Package Information

The FXAS21000 platform uses a 24-lead QFN package, case number 2209-01.

8.1 Product Identification Markings



8.2 Tape and Reel Information



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.05
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
(V) Typical SR value Max 10^9 OHM/SQ
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Figure 19. Tape dimensions

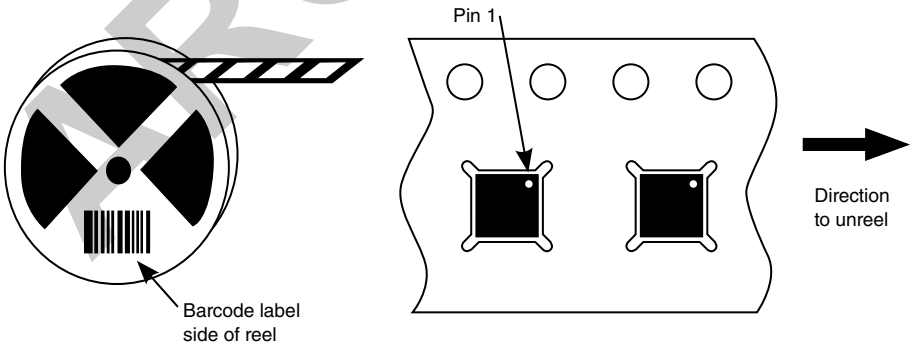
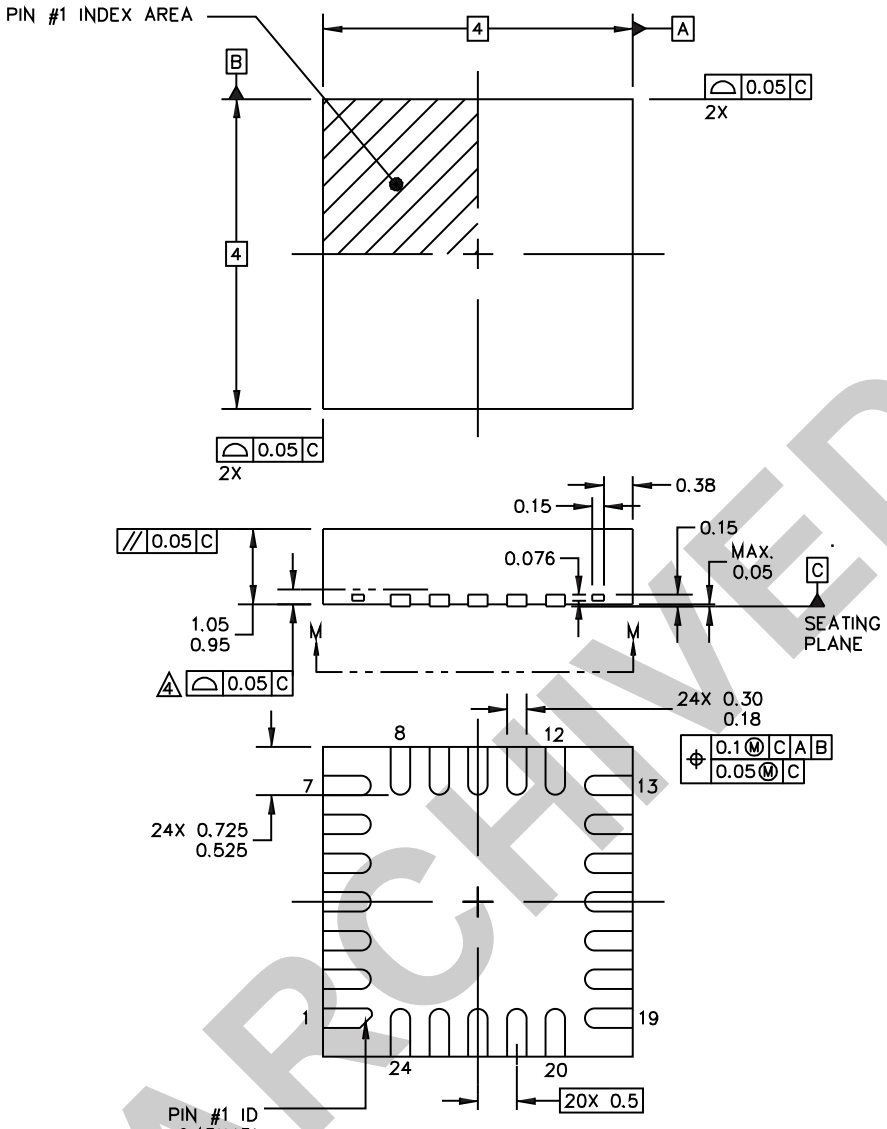


Figure 20. Tape and reel orientation

8.3 Package Description



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

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TITLE: QFN, CHIP ON LEAD (COL), 4 X 4 X 1, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00356D	REV: O
	CASE NUMBER: 2209-01	15 DEC 2011
	STANDARD: NON-JEDEC	

This drawing is located at www.freescale.com/files/shared/doc/package_info/98ASA00356D.pdf.

9 Revision History

Revision number	Revision date	Description
1.0	09/2013	Initial release of document
1.1	10/2013	Register address map, Comments column, 5:0 was 7:2 (3 plcs) RT_THS register table, THS[6:0] was THS[6:3] Electrical Characteristics, Idd_{Rdy}, Typ, 4.8 was 3.8
1.2	7/2014	Figures 3 and 4, changed value of capacitor on pins 18/19 and 14/15 from 1.0 to 0.1 and added a 0.1 µF capacitor to pins 14/15 Added Table 2, Temperature sensor characteristics Table 3, added Maximum Acceleration (all axes, 100 µs) Table 3, deleted Drop-test height Table 9, SDA setup time unit changed from µs to ns Table 32, changed all cutoff frequency values
1.3	11/2014	Moved Table 2, Temperature sensor characteristics, to Table 5 Added Appendix A and A.1

Appendix A: Errata

A.1 I²C Communications

Description

PFXAS21000C erroneously processes I²C read commands addressed to other devices on the I²C bus. This can have unintended effects including the clearing of status flags such as data ready, decrementing the FIFO counter, and de-asserting interrupt pins cleared by the action of an I²C read on flags. PFXAS21000C does not respond on the I²C bus to these erroneously processed read commands and it does not respond to I²C write commands addressed to other devices on the bus. As such, I²C bus communications are never corrupted and the performance of other devices on the bus will not be impacted.

Affected device registers

The PFXAS21000C registers and bit fields within these registers which may be erroneously read when the device is not actively addressed are shaded in the table below. Reading of these registers and their related bit fields may cause interrupt flags to be deasserted (for example, data ready, rate threshold, and FIFO status flags), or output data stored within the FIFO to be lost in applications where **F_SETUP[**F_MODE] > 0b00 (reading OUT_Z_MSB causes the next stored sample to be latched in the output registers, thereby discarding the previously stored set).

Register Name	Address	Type	B7	B6	B5	B4	B3	B2	B1	B0
STATUS	0x00	R	Alias for DR_STATUS or F_STATUS depending on F_MODE setting							
OUT_X_MSB	0x01	R	XD[15:8]							
OUT_X_LSB	0x02	R	XD[7:0]							
OUT_Y _MSB	0x03	R	YD[15:8]							
OUT_Y_LSB	0x04	R	YD[7:0]							
OUT_Z _MSB	0x05	R	ZD[15:8]							
OUT_Z_LSB	0x06	R	ZD[7:0]							
DR_STATUS	0x07	R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
F_STATUS	0x08	R	F_OVF	F_WMKF	F_CNT[5:0]					
F_SETUP	0x09	R/W	F_MODE[1:0]		F_WMRK[5:0]					
F_EVENT	0x0A	R	—	—	FEVENT	FE_TIME[4:0]				
INT_SRC_FLAG	0x0B	R	—	—	—	—	BOOT_END	SRC_FIFO	SRC_RT	SRC_DRDY
WHO_AM_I	0x0C	R	WHO_AM_I[7:0]							
CTRL_REG0	0x0D	R/W	BW[1:0]		SPIW	SEL[1:0]	HPF_EN	FS[1:0]		
RT_CFG	0x0E	R/W	—	—	—	—	ELE	ZTEFE	YTEFE	XTEFE
RT_SRC	0x0F	R	—	EA	ZRT	Z_RT_POL	YRT	Y_RT_POL	XRT	X_RT_POL
RT_THS	0x10	R/W	DBCNTM	THS[6:0]						
RT_CNT	0x11	R/W	RT_CNT[7:0]							
TEMP	0x12	R	TEMP[7:0]							
CTRL_REG1	0x13	R/W	—	RST	ST	DR[2:0]			ACTIVE	READY
CTRL_REG2	0x14	R/W	INT_CFG_FIFO	INT_EN_FIFO	INT_CFG_RT	INT_EN_RT	INT_CFG_DRDY	INT_EN_DRDY	IPOL	PP_OD

Workarounds

Three workarounds are associated with this erratum.

- Operate PFXAS21000C on a dedicated I²C bus. The part will behave as expected provided no I²C commands are sent which specify a different device address.
- Operate PFXAS21000C in SPI mode. This erratum has no impact on SPI operation.
- When operating PFXAS21000C on a shared I²C bus, poll the output registers asynchronously under timing from the host microcontroller rather than checking data ready bits or interrupts.

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