

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT7731**

### **Quad 64-bit static shift register**

Product specification  
File under Integrated Circuits, IC06

September 1993

## Quad 64-bit static shift register

## 74HC/HCT7731

## FEATURES

- Frequency range DC to 100 MHz.
- Separate serial data inputs
- Cascadable
- Functionally compatible with HEF 4731
- Includes recycling mode
- Direct shift out
- Output capability: Standard
- I<sub>CC</sub> category: LSI.

## APPLICATIONS

- Data storage
- Delay line.

## GENERAL DESCRIPTION

The HC/HCT7731 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT7731 are quad 64-bit static shift registers with a recycling mode. Each register has separate data inputs D<sub>a</sub> to D<sub>d</sub>, clock inputs CP<sub>a</sub> to CP<sub>d</sub> and data outputs Q<sub>a</sub> to Q<sub>d</sub>. Data shifts one place towards the output, each LOW to HIGH transition of the clock pulse. Each recycling mode input controls two registers REC<sub>ab</sub> for registers A and B and REC<sub>cd</sub> for registers C and D. When the REC input is HIGH, the device is in the recycling mode and data at the output is shifted back into the input of the register, so after 64 clock pulses the contents of a register is again in its original position. This enables the user to tap off data from any position. When the REC input is LOW external data can be shifted in.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP <sub>a-d</sub> to Q <sub>a-d</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	15	20	ns
f <sub>max</sub>	maximum clock frequency		100	100	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per register	notes 1, 2 and 3	58	61	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull-up} \times V_{CC})$$

where:

f<sub>i</sub> = input frequency in MHz.

f<sub>o</sub> = output frequency in MHz.

V<sub>CC</sub> = supply voltage in V.

C<sub>L</sub> = output load capacitance in pF.

I<sub>pull-up</sub> = pull-up currents in μA.

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V.
3. See also power dissipation information.

## ORDERING INFORMATION

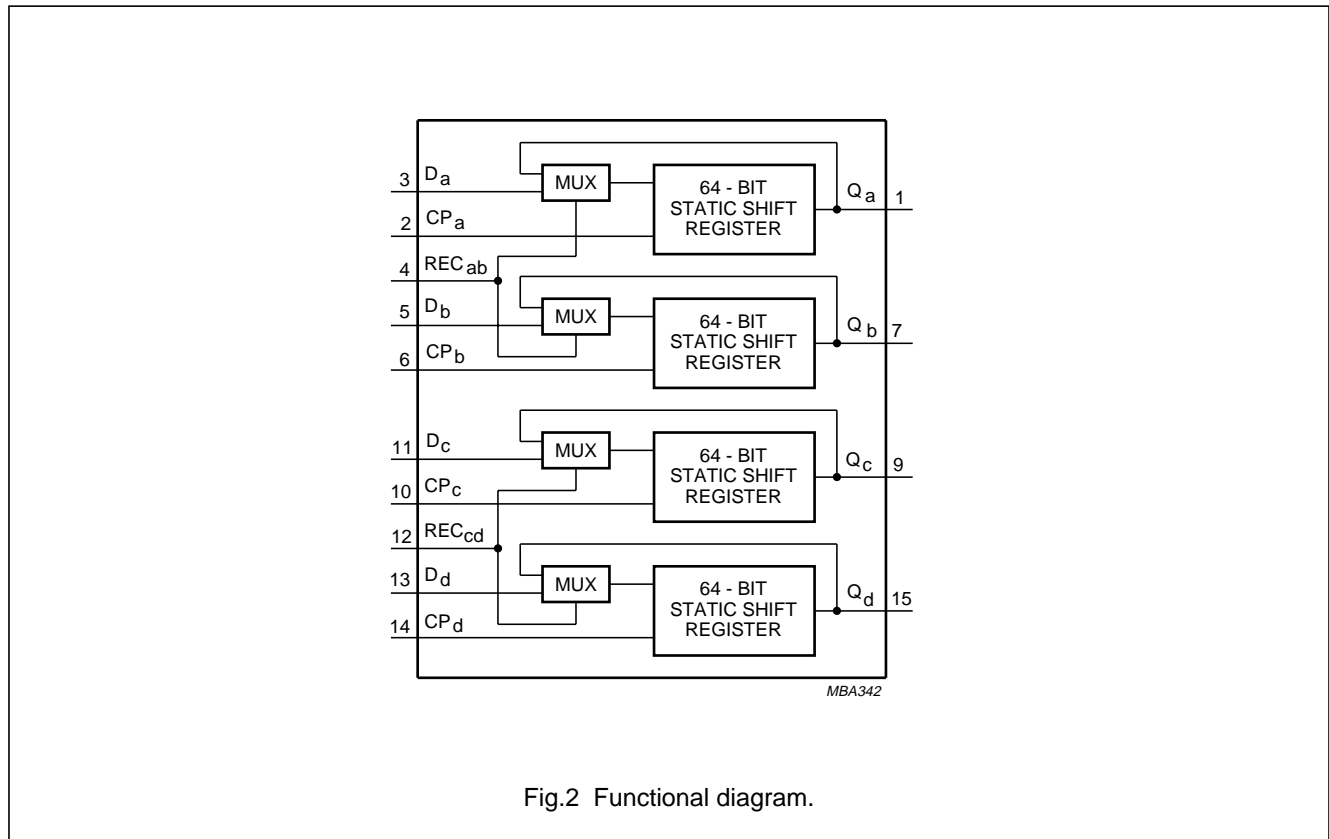
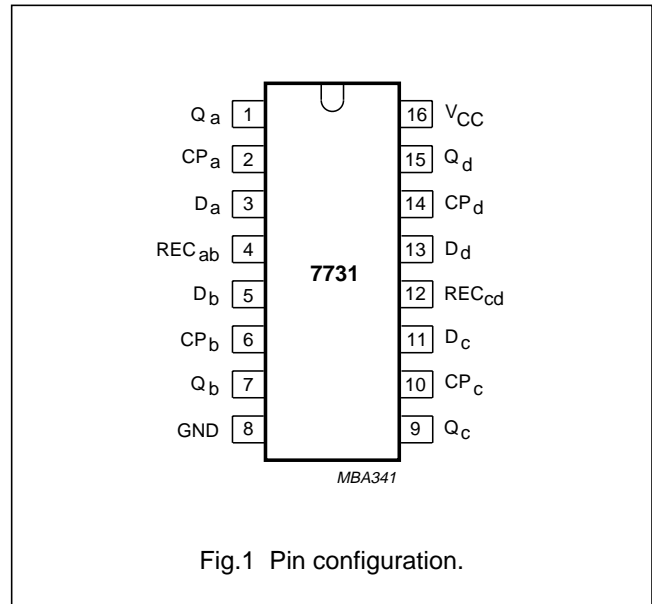
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7731N	16	DIL	plastic	SOT38Z
74HC/HCT7731D	16	SO16	plastic	SOT109A

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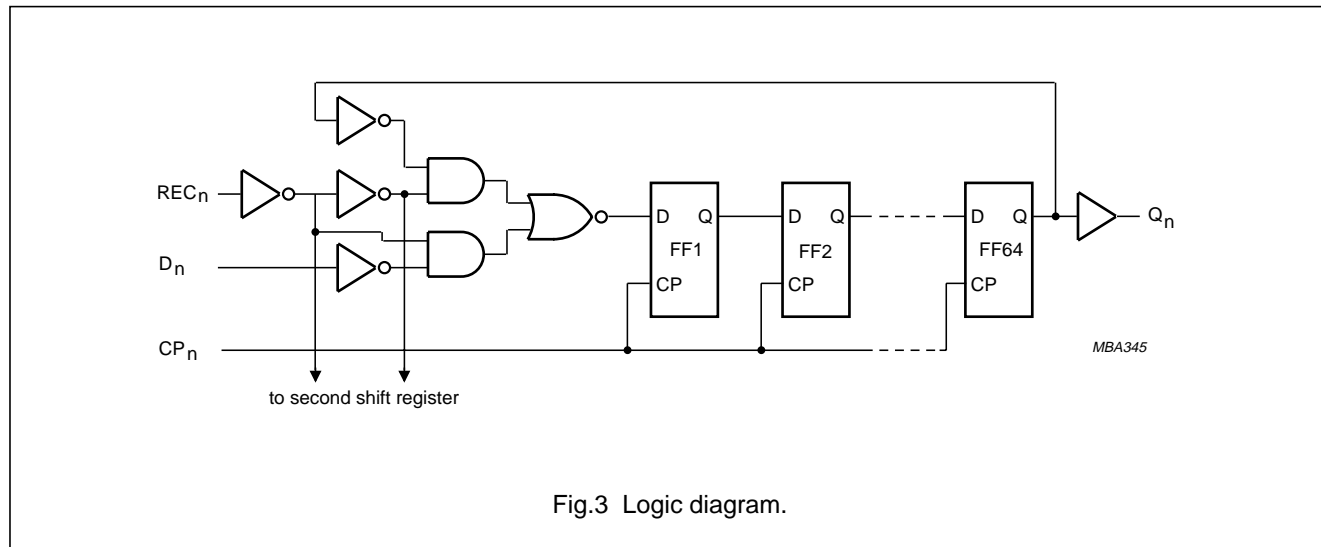
### PINNING

SYMBOL	PIN	DESCRIPTION
Q <sub>a</sub> to Q <sub>d</sub>	1, 7, 9, 15	data outputs
CP <sub>a</sub> to CP <sub>d</sub>	2, 6, 10, 14	clock inputs
D <sub>a</sub> to D <sub>d</sub>	3, 5, 11, 13	data inputs
REC <sub>ab</sub> , REC <sub>cd</sub>	4, 12	recycled enable input
GND	8	ground (0 V)
V <sub>CC</sub>	16	positive supply



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**FUNCTION TABLE**

INPUT		OUTPUT
REC	CP	MODE
L	↑	shift
H	↑	recycle

**Notes**

1. L = LOW voltage level  
 H = HIGH voltage Level  
 ↑ = LOW-to-HIGH CP transition

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: LSI.

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF.

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			V <sub>CC</sub> (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay time CP to Q <sub>n</sub>	–	50	155	–	190	–	230	ns	2.0	Fig.4
		–	18	31	–	38	–	46	ns	4.5	
		–	15	26	–	32	–	39	ns	6.0	
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	–	19	75	–	90	–	110	ns	2.0	Fig.4
		–	7	15	–	18	–	22	ns	4.5	
		–	6	13	–	15	–	19	ns	6.0	
t <sub>W</sub>	clock pulse width HIGH or LOW	80	19	–	100	–	120	–	ns	2.0	Fig.4
		16	7	–	20	–	24	–	ns	4.5	
		14	6	–	17	–	20	–	ns	6.0	
t <sub>su</sub>	set-up time D <sub>n</sub> to CP <sub>n</sub>	60	8	–	75	–	90	–	ns	2.0	Fig.4
		12	3	–	15	–	18	–	ns	4.5	
		10	3	–	13	–	15	–	ns	6.0	
t <sub>su</sub>	set-up time REC <sub>n</sub> to CP <sub>n</sub>	75	22	–	90	–	110	–	ns	2.0	Fig.5
		15	8	–	18	–	22	–	ns	4.5	
		13	7	–	15	–	19	–	ns	6.0	
t <sub>h</sub>	hold time D <sub>n</sub> to CP <sub>n</sub>	25	–3	–	30	–	35	–	ns	2.0	Fig.4
		5	–1	–	6	–	7	–	ns	4.5	
		4	–1	–	5	–	6	–	ns	6.0	
t <sub>h</sub>	hold time REC <sub>n</sub> to CP <sub>n</sub>	10	–8	–	10	–	15	–	ns	2.0	Fig.5
		2	–3	–	2	–	3	–	ns	4.5	
		2	–3	–	2	–	3	–	ns	6.0	
f <sub>max</sub>	maximum clock pulse frequency	6	26	–	4.8	–	4	–	MHz	2.0	Fig.4 (note 1)
		30	78	–	24	–	20	–	MHz	4.5	
		35	93	–	28	–	23	–	MHz	6.0	

**Note**

1. The maximum power dissipation has to be observed. See power dissipation information.

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## UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
CP <sub>n</sub>	0.7
REC <sub>n</sub>	0.4
D <sub>n</sub>	0.5

## Notes

1. The RS input has CMOS input switching levels.
2. The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in Table 1.

## AC CHARACTERISTICS FOR 74HCT

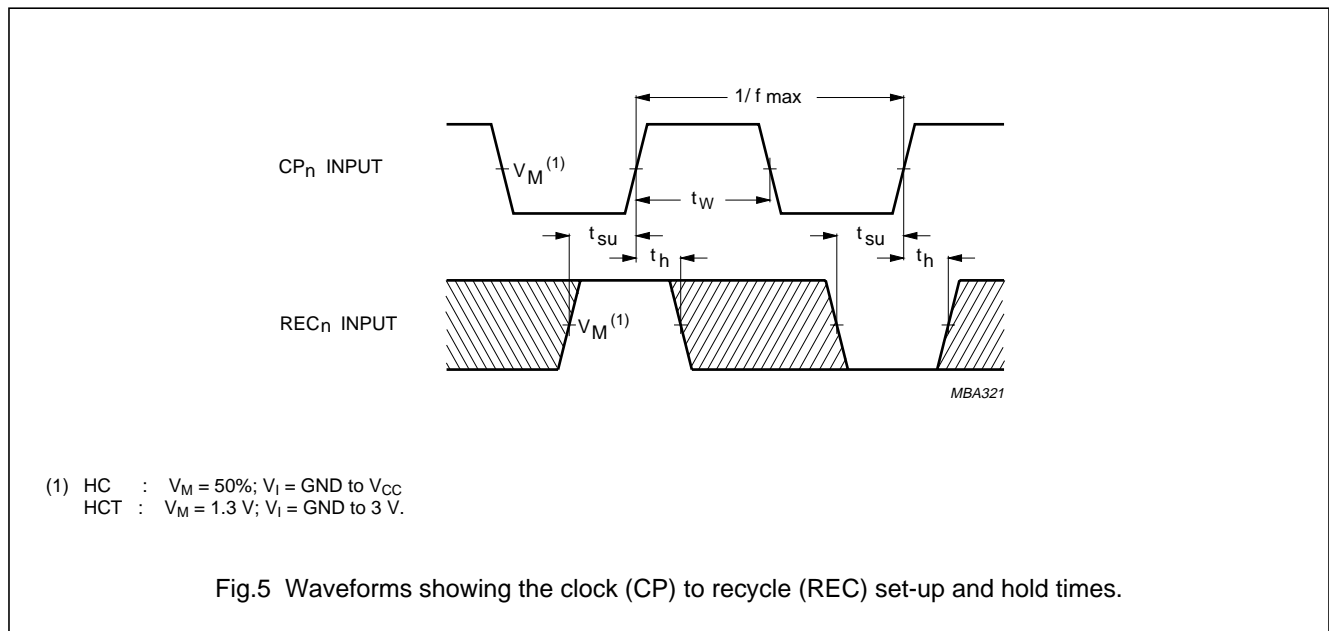
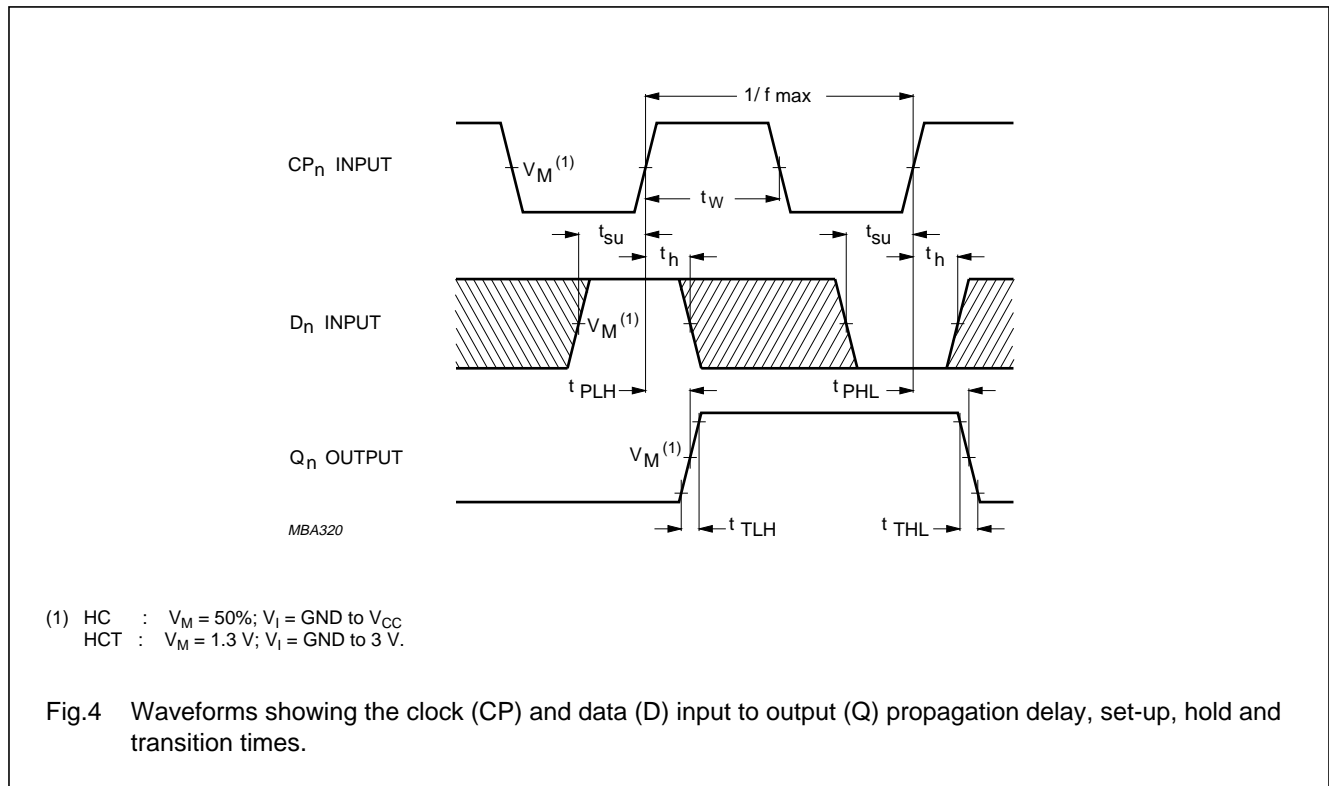
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			V <sub>CC</sub> (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay time CP to Q <sub>n</sub>	–	24	42	–	52	–	63	ns	4.5	Fig.4
t <sub>THL</sub> /t <sub>TLH</sub>	output transmission time	–	7	15	–	18	–	22	ns	4.5	Fig.4
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7	–	20	–	24	–	ns	4.5	Fig.4
t <sub>su</sub>	set-up time D <sub>n</sub> to CP <sub>n</sub>	12	3	–	15	–	18	–	ns	4.5	Fig.4
t <sub>su</sub>	set-up time REC <sub>n</sub> to CP <sub>n</sub>	15	6	–	18	–	22	–	ns	2	Fig.5
t <sub>h</sub>	hold time D <sub>n</sub> to CP <sub>n</sub>	5	0	–	6	–	7	–	ns	2	Fig.4
t <sub>h</sub>	hold time REC <sub>n</sub> to CP <sub>n</sub>	2	–3	–	2	–	3	–	ns	4.5	Fig.5
f <sub>max</sub>	maximum clock pulse frequency	30	80	–	24	–	20	–	MHz	4.5	Fig.4 (note 1)

Quad 64-bit static shift register

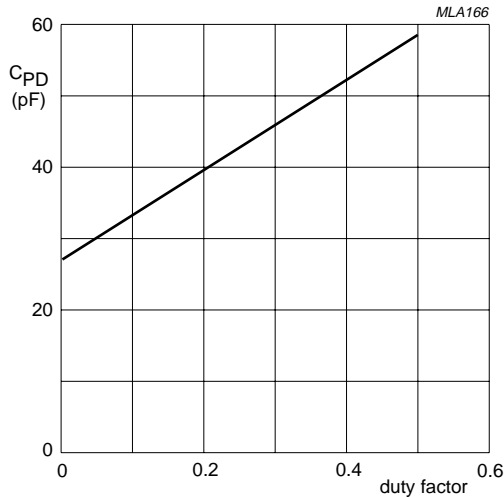
74HC/HCT7731

AC WAVEFORMS



## Quad 64-bit static shift register

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Fig.6 C<sub>PD</sub> as a function of the duty factor.**POWER DISSIPATION INFORMATION**

The power dissipation per register operating at the same frequency is given by:

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull-up} \times V_{CC})$$

- $f_i$  = clock input frequency  
 $f_o$  = data output frequency  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = power supply voltage in V.

As  $P_D$  also depends on the frequency at which the contents of the internal bits are changing, the value of  $C_{PD}$  is a function of the duty factor ( $d_f$ ) being the ratio between data and clock frequency, see Fig.6.

Example:

$$\begin{aligned}
 f_i &= 12 \text{ MHz} \\
 f_o &= 3 \text{ MHz} \\
 C_L &= 25 \text{ pF} \\
 V_{CC} &= 5 \text{ V} \\
 d_f &= 3/12 = 0.25 \\
 C_{PD} &= 42.5 \text{ pF} \\
 P_D &= (42.5 \times 5^2 \times 12) + (25 \times 5^2 \times 3) = 14625 \text{ } \mu\text{W}
 \end{aligned}$$

As the maximum allowable power dissipation in an SO package at  $T_{amb} = 125 \text{ }^\circ\text{C}$  is 60 mW, it is allowed to apply 4 registers at the same time under these conditions.

**PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".