# DATA SHEET

# OM4068
## LCD driver for low multiplex rates

Product specification
File under Integrated Circuits, IC12

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PHILIPS

# LCD driver for low multiplex rates OM4068

## FEATURES

- Single-chip LCD controller/driver
- Static/duplex/triplex drive modes with up to 32/64/96 LCD segments drive capability per device
- Selectable backplane drive configuration: static or 2 or 3 backplane multiplexing
- Selectable display bias configuration drive: static, $\frac{1}{2}$ or $\frac{1}{3}$
- 32 segment drivers
- Serial data input (word length 32 to 96 bits)
- On-chip generation of intermediate LCD bias voltages
- 2 MHz fast serial bus interface
- CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications
- Logic supply voltage range ($V_{DD} - V_{SS}$) of 2.5 to 5.5 V
- Display supply voltage range ($V_{LCD} - V_{SS}$) of 3.5 to 6.5 V
- Low power consumption, suitable for battery operated systems
- No external components needed by the oscillator
- Manufactured in silicon gate CMOS process.

## APPLICATIONS

- Telecom equipment
- Portable instruments
- Alarm systems
- Automotive equipment.

## GENERAL DESCRIPTION

The OM4068 is a low-power CMOS LCD driver, designed to drive Liquid Crystal Displays (LCDs) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to three backplanes and up to 32 segment lines and can be easily cascaded for larger LCD applications. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption. A 3-line bus structure enables serial data transfer with most microprocessors/microcontrollers. All inputs are CMOS compatible.

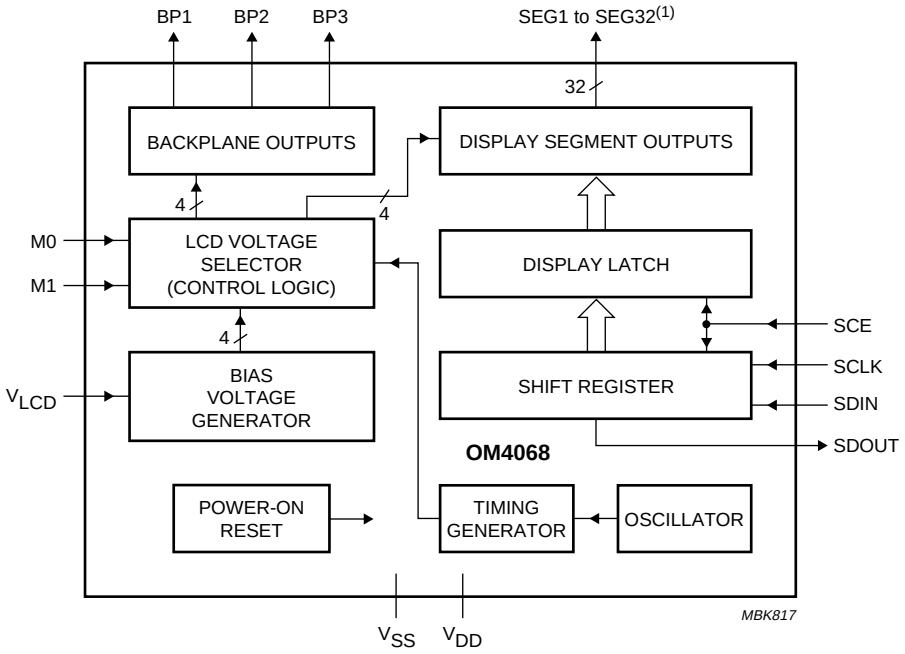
## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| OM4068H[1] | QFP44 | plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm | SOT307-2 |
| OM4068P | DIP40 | plastic dual in-line package; 40 leads (600 mil) | SOT129-1 |
| OM4068U/5[2] | die | unsawn wafer | – |
| OM4068U | tray | chip in tray | – |

**Notes**

1. Gull Wing package.
2. For details see Chapter “Bonding pad locations”.

## BLOCK DIAGRAM




(1) SEG1, SEG6, SEG15 and SEG25 are not available in DIP40 package.

Fig.1 Block diagram.

## PINNING

See notes 1 to 8.

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | QFP44 | DIP40 | |
| $V_{LCD}$ | 4 | 19 | LCD supply voltage |
| $V_{DD}$ | 5 | 20 | positive supply voltage |
| $V_{SS}$ | 6 | 21 | ground |
| M0 | 7 | 22 | drive mode select input 0 |
| M1 | 8 | 23 | drive mode select input 1 |
| SDIN | 9 | 24 | serial bus data input |
| SCLK | 10 | 25 | serial bus clock input |
| SCE | 11 | 26 | serial bus clock enable |
| SDOUT | 12 | 27 | serial bus data output |
| BP1 | 13 | 28 | LCD backplane driver output 1 |
| BP2 | 14 | 29 | LCD backplane driver output 2 |
| BP3 | 15 | 30 | LCD backplane driver output 3 |
| SEG1 | 16 | – | LCD segment driver output 1 |
| SEG2 | 17 | 31 | LCD segment driver output 2 |
| SEG3 | 18 | 32 | LCD segment driver output 3 |
| SEG4 | 19 | 33 | LCD segment driver output 4 |
| SEG5 | 20 | 34 | LCD segment driver output 5 |
| SEG6 | 21 | – | LCD segment driver output 6 |
| SEG7 | 22 | 35 | LCD segment driver output 7 |
| SEG8 | 23 | 36 | LCD segment driver output 8 |
| SEG9 | 24 | 37 | LCD segment driver output 9 |
| SEG10 | 25 | 38 | LCD segment driver output 10 |
| SEG11 | 26 | 39 | LCD segment driver output 11 |
| SEG12 | 27 | 40 | LCD segment driver output 12 |
| SEG13 | 28 | 1 | LCD segment driver output 13 |
| SEG14 | 29 | 2 | LCD segment driver output 14 |
| SEG15 | 30 | – | LCD segment driver output 15 |
| SEG16 | 31 | 3 | LCD segment driver output 16 |
| SEG17 | 32 | 4 | LCD segment driver output 17 |
| SEG18 | 33 | 5 | LCD segment driver output 18 |
| SEG19 | 34 | 6 | LCD segment driver output 19 |
| SEG20 | 35 | 7 | LCD segment driver output 20 |
| SEG21 | 36 | 8 | LCD segment driver output 21 |
| SEG22 | 37 | 9 | LCD segment driver output 22 |
| SEG23 | 38 | 10 | LCD segment driver output 23 |
| SEG24 | 39 | 11 | LCD segment driver output 24 |
| SEG25 | 40 | – | LCD segment driver output 25 |
| SEG26 | 41 | 12 | LCD segment driver output 26 |

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | QFP44 | DIP40 | |
| SEG27 | 42 | 13 | LCD segment driver output 27 |
| SEG28 | 43 | 14 | LCD segment driver output 28 |
| SEG29 | 44 | 15 | LCD segment driver output 29 |
| SEG30 | 1 | 16 | LCD segment driver output 30 |
| SEG31 | 2 | 17 | LCD segment driver output 31 |
| SEG32 | 3 | 18 | LCD segment driver output 32 |

**Notes**

1. SEG1 to SEG32 (LCD segment driver outputs) output the multi-level signals for the LCD segments.
2. BP0, BP1 and BP2 (LCD backplane driver outputs) output the multi-level signals for the LCD backplanes.
3. $V_{LCD}$ (LCD power supply): power supply for the LCD.
4. SDIN (serial data line): input for the bus data line.
5. SCL (serial clock line): input for the bus clock line.
6. SDOUT (serial data output): output of the shift register to allow serial cascading of the OM4068 with other devices.
7. SCE (serial clock enable): input for enable/disable acquisition on the data input line. If disabled, data on the serial bus are not accepted by the device.
8. M0 and M1 (display mode select inputs): inputs to select the LCD drive configurations; static, duplex or triplex.

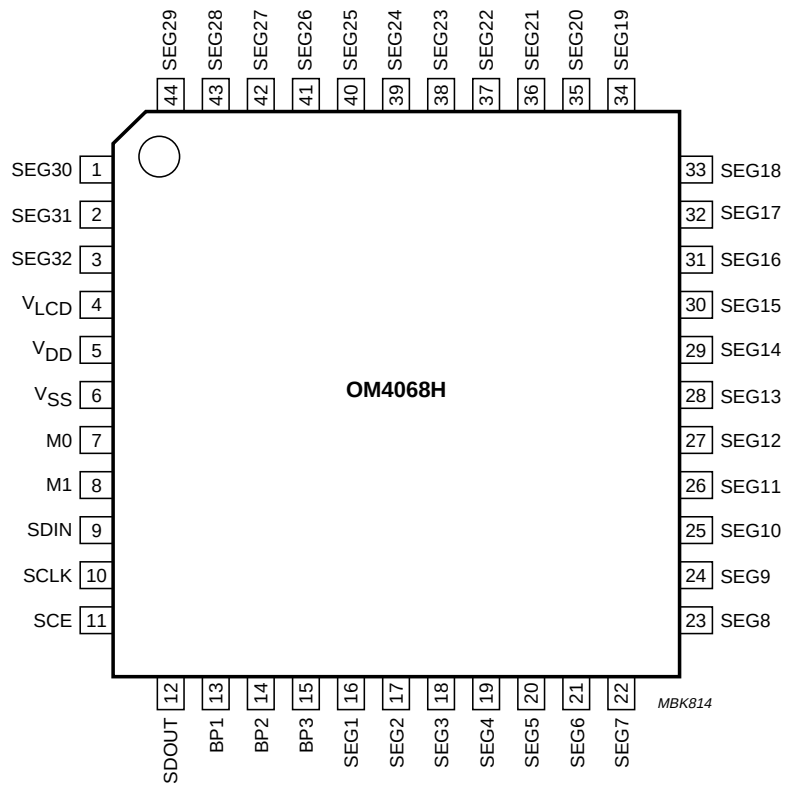



Fig.2 Pin configuration (QFP44).

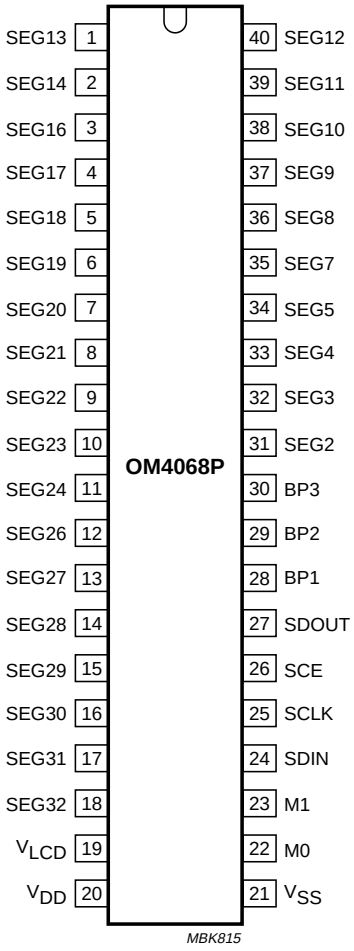



Fig.3 Pin configuration (DIP40).

## FUNCTIONAL DESCRIPTION

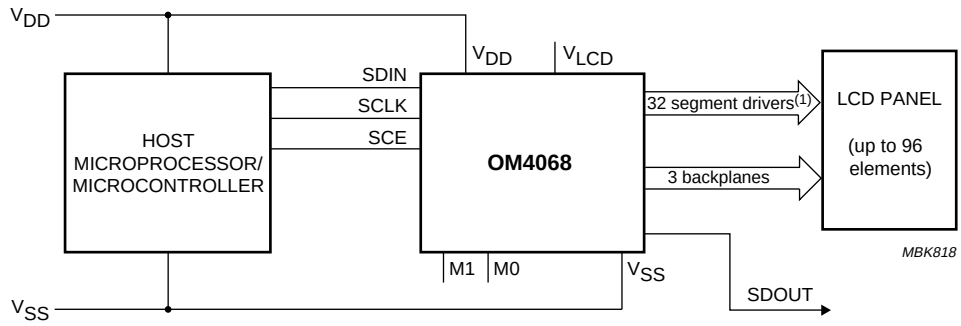
The OM4068 is a low-power LCD driver designed to interface with any microprocessor/microcontroller and a wide variety of LCDs. It can drive any static or multiplexed LCD containing up to three backplanes and up to 96 segments.

The display configurations possible with the OM4068 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

A typical system (MUX 1 : 3) is shown in Fig.4.

**Table 1** Selection of display configurations

| NUMBER OF | | 7-SEGMENTS NUMERIC | | DOT MATRIX |
|---|---|---|---|---|
| BACKPLANES | DISPLAY SEGMENTS | DIGITS | INDICATOR SYMBOLS | |
| 3 | 96 | 12 | 12 | 96 dots ($3 \times 32$) |
| 2 | 64 | 8 | 8 | 64 dots ($2 \times 32$) |
| 1 | 32 | 4 | 4 | 32 dots ($1 \times 32$) |




(1) 28 segment drivers for DIP40 package.

Fig.4 Typical system configuration.

The host microprocessor/microcontroller maintains the 3-line bus communication channel with OM4068. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip.

The only other connections required to complete the system are to the power supplies ($V_{SS}$, $V_{DD}$ and $V_{LCD}$) and suitable capacitors to decouple the $V_{LCD}$ and $V_{DD}$ pins to $V_{SS}$.

### Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failures. The OM4068 resets to a starting condition as follows:

- All backplane and segment outputs are set to $V_{SS}$ (display off)
- All shift registers and latches are set in 3-state
- SDOUT (allowing serial cascading) is set to logic 0 (with SCE LOW)
- Power-down mode.

Data transfers on the serial bus should be avoided for 0.5 ms following power-on to allow completion of the reset action.

### Power-down

After power-on the chip is in power-down mode as long as the serial clock is not active. During power-down all static currents are switched off (no internal oscillator, no timing and no bias level generation) and all LCD-outputs are 3-stated. The power-on reset functions remain enabled.

The power-down mode is disabled at the first rising edge of the serial clock SCLK.

### LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The full-scale LCD voltage $V_{OP}$ equals $V_{LCD} - V_{SS}$. The optimum value of $V_{OP}$ depends on the LCD threshold voltage ($V_{th}$) and the number of bias levels.

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors ($\frac{1}{3}$bias) connected between $V_{LCD}$ and $V_{SS}$. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

The bias levels depend on the multiplex rate and are selected automatically when the display configuration is selected using M1 and M0.

### LCD voltage selector

The LCD voltage selector (control logic) coordinates the multiplexing of the LCD in accordance with the selected drive or display configuration. The operation of the voltage selector is controlled by the input pins M0 and M1 (see Table 2).

**Table 2** Drive mode selection

| M1 | M0 | DRIVE MODE |
|---|---|---|
| 0 | 0 | test mode (not user accessible) |
| 0 | 1 | static drive (1 : 1) |
| 1 | 0 | duplex drive (1 : 2) |
| 1 | 1 | triplex drive (1 : 3) |

For multiplex rates of 1 : 2 three bias levels are used including $V_{LCD}$ and $V_{SS}$. Four bias level are used for the 1 : 3 multiplex rate. The various biasing configurations together with the biasing characteristics as functions of $V_{OP} = V_{LCD} - V_{SS}$ and the resulting discrimination ratios (D), are given in Table 3.

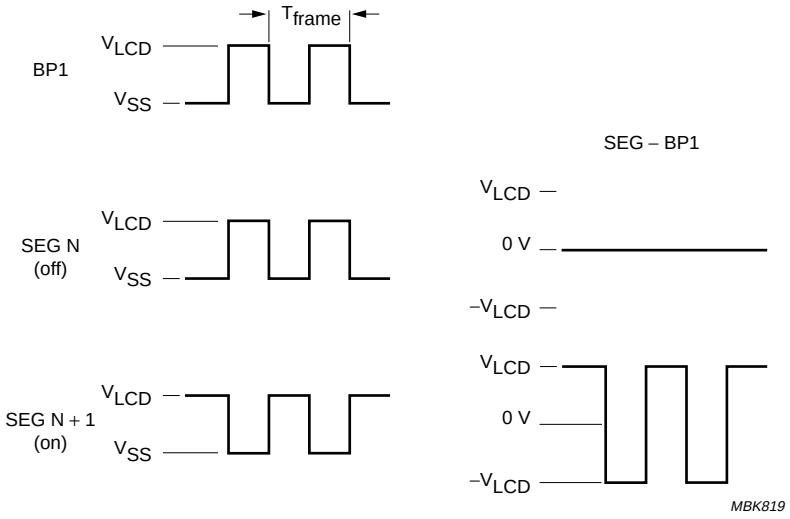
A practical value for $V_{OP}$ is determinated by equating $V_{off(rms)}$ with a defined LCD threshold voltage ($V_{th}$), typically when the LCD exhibits approximately 10% contrast. In static mode a suitable choice is $V_{OP} > 3V_{th}$.

**Table 3** LCD drive modes: summary of characteristics

| LCD DRIVE MODE | NUMBER OF | | LCD BIAS CONFIGURATION | $\frac{V_{off(rms)}}{V_{OP}}$ | $\frac{V_{on(rms)}}{V_{OP}}$ | $D = \frac{V_{on(rms)}}{V_{off(rms)}}$ |
|---|---|---|---|---|---|---|
| | BACKPLANES | LEVELS | | | | |
| Static | 1 | 2 | static | 0 | 1 | – |
| 1 : 2 | 2 | 3 | ½ | 0.354 | 0.791 | 2.2236 |
| 1 : 3 | 3 | 4 | ⅓ | 0.333 | 0.638 | 1.915 |

### LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.

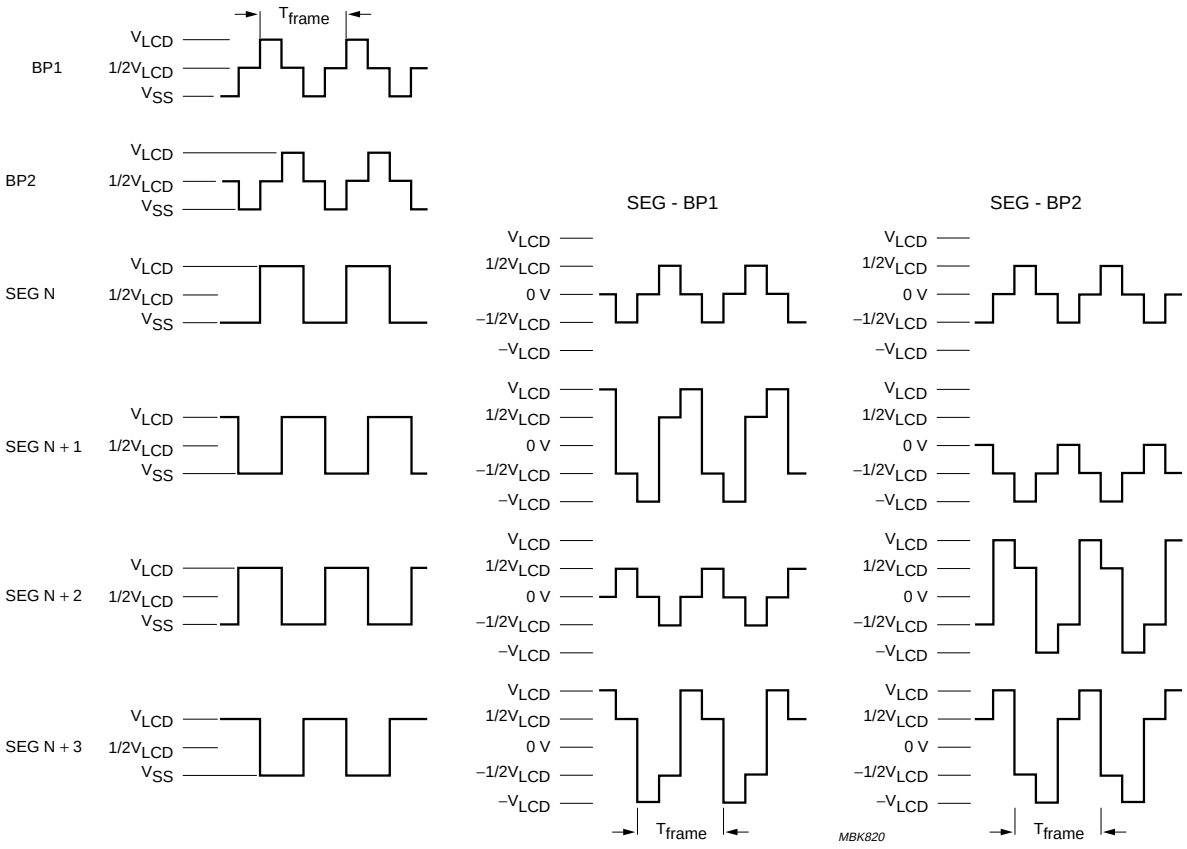



| BACKPLANE DRIVER OUTPUT | SEGMENTS | |
|---|---|---|
| | SEG N | SEG N + 1 |
| BP1 | off | on |

Fig.5 Static drive mode waveforms ($V_{OP} = V_{LCD} - V_{SS}$).

### 1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies, as shown in Fig.6.

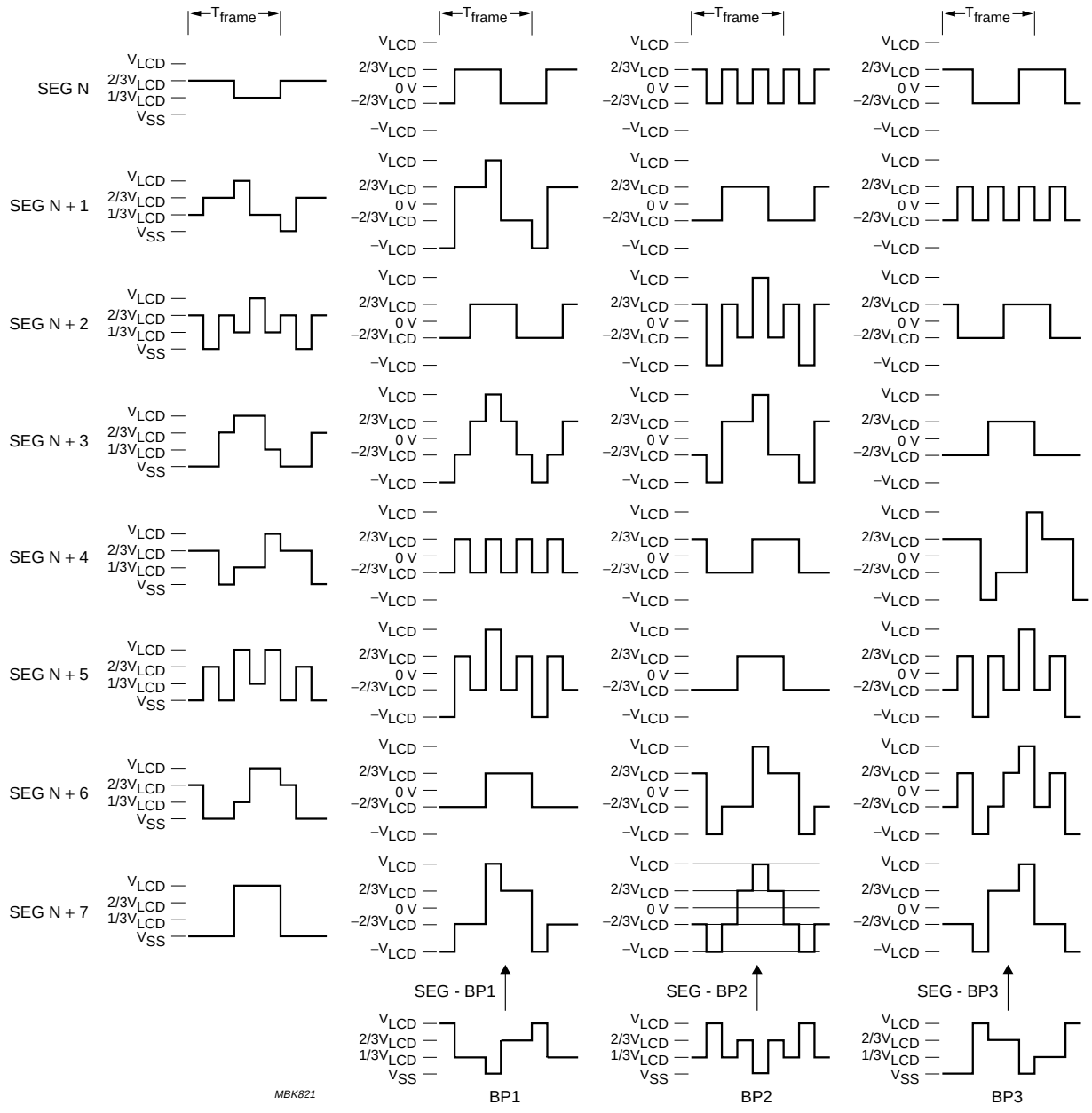



| BACKPLANE DRIVER OUTPUTS | SEGMENTS | | | |
|---|---|---|---|---|
| | SEG N | SEG N + 1 | SEG N + 2 | SEG N + 3 |
| BP1 | off | on | off | on |
| BP2 | off | off | on | on |

Fig.6 Waveforms for 1 : 2 multiplex drive mode ($V_{OP} = V_{LCD} - V_{SS}$).

### 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex mode applies, as shown in Fig.7.




| BACKPLANE DRIVER OUTPUTS | SEGMENTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | N | N + 1 | N + 2 | N + 3 | N + 4 | N + 5 | N + 6 | N + 7 |
| BP1 | off | on | off | on | off | on | off | on |
| BP2 | off | off | on | on | off | off | on | on |
| BP3 | off | off | off | off | on | on | on | on |

Fig.7 Waveforms for 1 : 3 multiplex drive motive ($V_{OP} = V_{LCD} - V_{SS}$).

### Oscillator

The internal logic and the multi-level LCD drive signals of the OM4068 are generated by the built-in RC oscillator. No external components are required.

In order to minimize radio frequency interference, the oscillator operates with symmetrical and slew-rate limited capacitor charge/discharge.

The oscillator runs continuously once the power down state after power-on has been left.

### Interface to microprocessor unit: serial interface

A three-line bus structure enables serial unidirectional data transfer with microprocessors/microcontrollers. The three lines are a serial data input line (SDIN), a serial clock line (SCLK) and a data line enable (SCE). All inputs are CMOS compatible. These lines must always be in a defined state $V_{SS}$ or $V_{DD}$. Floating inputs could damage the chip.

On the bus, one data bit is transferred during each clock pulse. The data on the SDIN line remains stable during the whole clock period. Data changes arrive with the falling edge of the serial clock SCLK (see Fig.8).

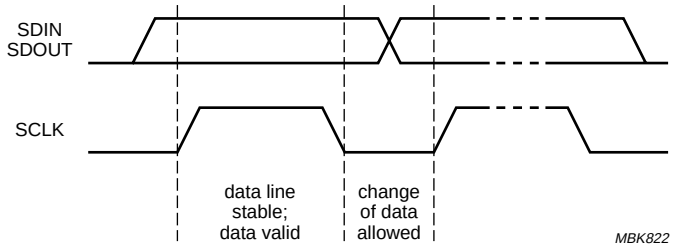



Fig.8 Bit transfer on bus.

### Shift register

Data present on the SDIN pin is shifted into a shift register with the rising edge of the serial clock SCLK in a synchronous manner. The shift register serves to transfer display information from the serial bus to the (display) latch while previous data is displayed.

The shift register is organized as three 32-bit shift registers. Depending on the display driving mode selected (see Table 3), one, two or three registers are used and cascaded resulting in a shift register length of 32, 64 or 96 bits. Figure 9 shows the shift register organization with the display data bits after a shift operation is completed. The shift sequence begins with data bit D32 and finishes with data bit D1. The correspondence between the data bit numbers and the LCD display segments is shown in Table 4.

Data from the last stage of the register is supplied to the SDOUT pin to allow serial cascading of the OM4068 with other peripheral devices. Depending on the display driving mode selected, SDOUT corresponds to bit 32, 64 or 96 of the register (see Fig.10). Data on the SDOUT pin is shifted out with the falling edge of the SCLK clock. SDOUT is therefore delayed by $\frac{1}{2}$SCLK cycle before it is applied to the SDIN pin of the next IC in the serial chain (see Fig.8).

The clock enable SCE signal must be HIGH in order to enable the shift operation. SDOUT output is latched with the last data after SCE returned to HIGH (shift operation terminated).

SDOUT is in 3-state mode when SCE is LOW.

### Display latch

The 96-bit display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch and the LCD segment outputs. An LCD segment is activated when the corresponding data bit in the display latch is HIGH.

Display latches are in HOLD mode (SCE HIGH) during the shift operation to maintain the display data constant.

Data are latched into the display latch with the internal frame clock. Thus there is a delay of up to one half frame before new data are latched after signal SCE returns to zero.

### Timing

The timing of the OM4068 organizes the internal data flow of the device. This includes the transfer of display data from the shift register to the display segments outputs. The timing also generates the LCD frame frequency which is derived from the clock frequency generated in the internal clock generator:

$$f_{fr(LCD)} = \frac{f_{osc}}{2400}$$

### Shift register configuration

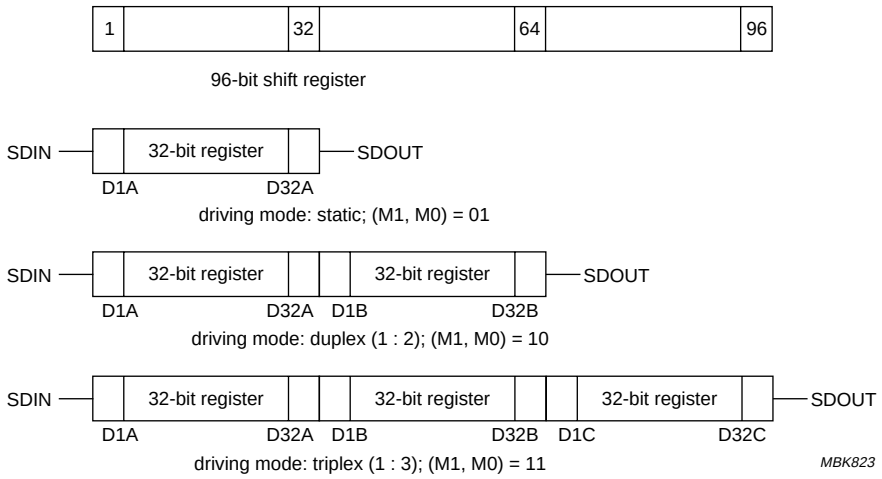



Fig.9 Display data bit position in shift register.

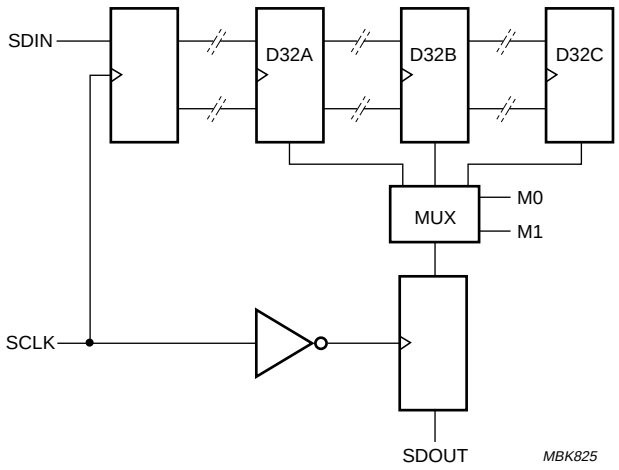



Fig.10 Shift register structure.

**Table 4** Relationships between data bit numbers and the LCD segment outputs

| SEGMENT NUMBER | DRIVING MODE | | | | | |
|---|---|---|---|---|---|---|
| | STATIC | DUPLEX | | TRIPLEX | | |
| SEG1 | D1A | D1A | D1B | D1A | D1B | D1C |
| SEG2 | D2A | D2A | D2B | D2A | D2B | D2C |
| SEG3 | D3A | D3A | D3B | D3A | D3B | D3C |
| SEG4 | D4A | D4A | D4B | D4A | D4B | D4C |
| SEG5 | D5A | D5A | D5B | D5A | D5B | D5C |
| SEG6 | D6A | D6A | D6B | D6A | D6B | D6C |
| SEG7 | D7A | D7A | D7B | D7A | D7B | D7C |
| SEG8 | D8A | D8A | D8B | D8A | D8B | D8C |
| SEG9 | D9A | D9A | D9B | D9A | D9B | D9C |
| SEG10 | D10A | D10A | D10B | D10A | D10B | D10C |
| SEG11 | D11A | D11A | D11B | D11A | D11B | D11C |
| SEG12 | D12A | D12A | D12B | D12A | D12B | D12C |
| SEG13 | D13A | D13A | D13B | D13A | D13B | D13C |
| SEG14 | D14A | D14A | D14B | D14A | D14B | D14C |
| SEG15 | D15A | D15A | D15B | D15A | D15B | D15C |
| SEG16 | D16A | D16A | D16B | D16A | D16B | D16C |
| SEG17 | D17A | D17A | D17B | D17A | D17B | D17C |
| SEG18 | D18A | D18A | D18B | D18A | D18B | D18C |
| SEG19 | D19A | D19A | D19B | D19A | D19B | D19C |
| SEG20 | D20A | D20A | D20B | D20A | D20B | D20C |
| SEG21 | D21A | D21A | D21B | D21A | D21B | D21C |
| SEG22 | D22A | D22A | D22B | D22A | D22B | D22C |
| SEG23 | D23A | D23A | D23B | D23A | D23B | D23C |
| SEG24 | D24A | D24A | D24B | D24A | D24B | D24C |
| SEG25 | D25A | D25A | D25B | D25A | D25B | D25C |
| SEG26 | D26A | D26A | D26B | D26A | D26B | D26C |
| SEG27 | D27A | D27A | D27B | D27A | D27B | D27C |
| SEG28 | D28A | D28A | D28B | D28A | D28B | D28C |
| SEG29 | D29A | D29A | D29B | D29A | D29B | D29C |
| SEG30 | D30A | D30A | D30B | D30A | D30B | D30C |
| SEG31 | D31A | D31A | D31B | D31A | D31B | D31C |
| SEG32 | D32A | D32A | D32B | D32A | D32B | D32C |

### Segment outputs

The LCD drive section includes 32 segment outputs SEG1 to SEG32 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplex backplane signals and with data in the display latch. When less than 32 segments are required the unused segment outputs should be left open-circuit.

### Backplane outputs

The LCD drive section includes three backplane outputs (BP1 to BP3) which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than three backplane outputs are required the unused outputs should be left open-circuit. In 1 : 2 multiplex drive mode, BP3 is set to $\frac{1}{2}V_{LCD}$. In static drive mode BP3 and BP2 are set to $V_{SS}$.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +6.5 | V |
| $V_{LCD}$ | LCD supply voltage | | –0.5 | +7.5 | V |
| $V_I$ | input voltage (any input) | | –0.5 | $V_{DD}$ + 0.5 | V |
| $V_O$ | output voltage (BP1, BP2, BP3, S1 to S32 and $V_{LCD}$) | | –0.5 | $V_{LCD}$ + 0.5 | V |
| $I_I$ | DC input current | | –10 | +10 | mA |
| $I_O$ | DC output current | | –10 | +10 | mA |
| $I_{DD}$, $I_{SS}$, $I_{LCD}$ | $V_{DD}$, $V_{SS}$ or $V_{LCD}$ current | | –50 | +50 | mA |
| $P_{tot(pack)}$ | total power dissipation per package | | – | 500 | mW |
| P/out | power dissipation per output | | – | 10 | mW |
| $T_{amb}$ | operating ambient temperature | | –40 | +105 | °C |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | | – | 150 | °C |
| $V_{es}$ | electrostatic handling | note 1 | –2000 | +2000 | V |
| | | note 2 | –150 | +150 | V |

**Notes**

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor (human body model).
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor (machine model).

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

## DC CHARACTERISTICS

$V_{DD}$ = 2.5 to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 3.5 to 6.5 V; $T_{amb}$ = –40 to +105 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage | | $V_{SS}$ + 2.5 | – | 5.5 | V |
| $V_{LCD}$ | LCD supply voltage | | $V_{SS}$ + 3.5 | – | 6.5 | V |
| $I_{DD}$ | supply current | power-down state; note 1 | – | 4 | 10 | µA |
| | | normal mode; $f_{osc}$ = intern; notes 2 and 3 | – | 12 | 25 | µA |
| $I_{LCD}$ | $V_{LCD}$ current | power-down state; note 1 | – | – | 1.5 | µA |
| | | normal mode; $f_{osc}$ = intern; notes 3 and 4 | – | – | 40 | µA |
| $V_{POR}$ | power-on reset voltage level | note 5 | 0.8 | 1.25 | 1.6 | V |
| **Logic** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | $V_{SS}$ | – | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD}$ | – | $V_{DD}$ | V |
| $I_{OL}$ | LOW-level output current (SDOUT) | $V_{OL}$ = 0.5 V; $V_{DD}$ = 5 V | 1.0 | – | – | mA |
| $I_{OH}$ | HIGH-level output current (SDOUT) | $V_{OH} = V_{DD} – 0.5$ V; $V_{DD}$ = 5 V | – | – | –1 | mA |
| $I_{pu}$ | pull-up current M1 and M0 | $V_I = V_{SS}$ | 0.04 | 0.15 | 1 | µA |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | –1 | – | +1 | µA |
| **Segment and backplane outputs** | | | | | | |
| $R_{(o)seg}$ | segment output resistance SEG1 to SEG32 | note 6 | – | 15 | 40 | kΩ |
| $R_{(o)back}$ | backplane output resistance BP1 to BP3 | note 6 | – | 15 | 40 | kΩ |
| $V_{seg(bias)(tol)}$ | bias tolerance SEG1 to SEG32 | note 7 | –100 | 0 | +100 | mV |
| $V_{back(bias)(tol)}$ | bias tolerance BP1, BP2 and BP3 | note 7 | –100 | 0 | +100 | mV |

### Notes

1. Power-down state. After power-on the chip is in power-down state as long as the serial clock is not activated. During power-down all static currents are switched off except the power-on reset block.
2. Output SDOUT is open-circuit; inputs at $V_{DD}$ or $V_{SS}$; bus inactive.
3. Drive mode: static, duplex and triplex.
4. LCD outputs are open-circuit, $C_L$ = 50 pF typical, inputs at $V_{DD}$ or $V_{SS}$; bus inactive.
5. Resets all logic when $V_{DD} < V_{POR}$.
6. Resistance of output terminal (S1 to S32 and BP1, BP2 and BP3) with a load current of 20 µA; outputs measured one at a time.
7. LCD outputs open-circuits.

## AC CHARACTERISTICS

$V_{DD}$ = 2.5 to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 5.0 V; $T_{amb}$ = –40 to +105 °C; unless otherwise specified.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $f_{fr(LCD)}$ | LCD frame frequency (internal clock) | 50 | 84 | 175 | Hz |
| $f_{osc}$ | oscillator frequency (not available at any pin) | 116 | 224 | 405 | kHz |
| **Bus timing characteristics: serial bus interface**; note 1 | | | | | |
| $f_{SCLK}$ | SCLK clock frequency | 0 | – | 2.1 | MHz |
| $t_{SCLKL}$ | SCLK clock LOW period | 190 | – | – | ns |
| $t_{SCLKH}$ | SCLK clock HIGH period | 190 | – | – | ns |
| $t_{su(D)}$ | data set-up time | 100 | – | – | ns |
| $t_{h(D)}$ | data hold time | 100 | – | – | ns |
| $t_r$ | SCLK, SDIN rise time | – | 10 | – | ns |
| $t_f$ | SCLK, SDIN fall time | – | 10 | – | ns |
| $t_{su(en)(SDEH-SCLKH)}$ | enable set-up time (SDE HIGH to SCLK HIGH) | 250 | – | – | ns |
| $t_{su(dis)(SCLKL-SDEL)}$ | disable set-up time (SCLK LOW to SDE LOW) | 250 | – | – | ns |
| $t_{PHL(SDOUT)}$ | SDOUT HIGH-to-LOW propagation delay | 100 | – | – | ns |

**Note**

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.

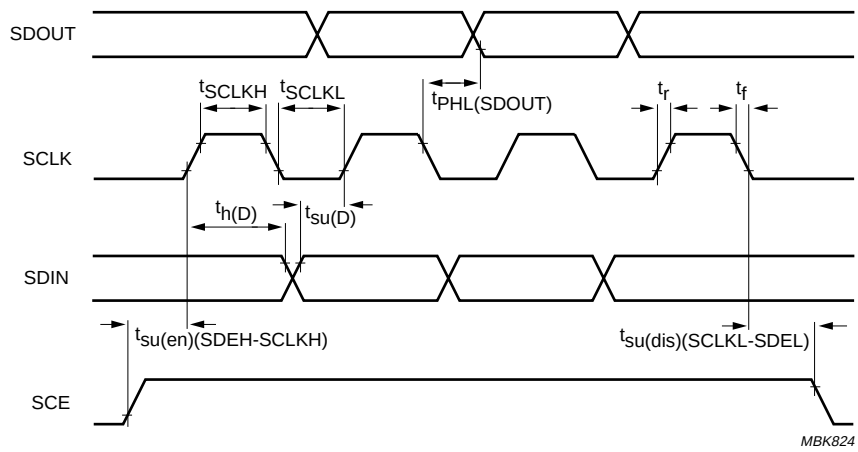
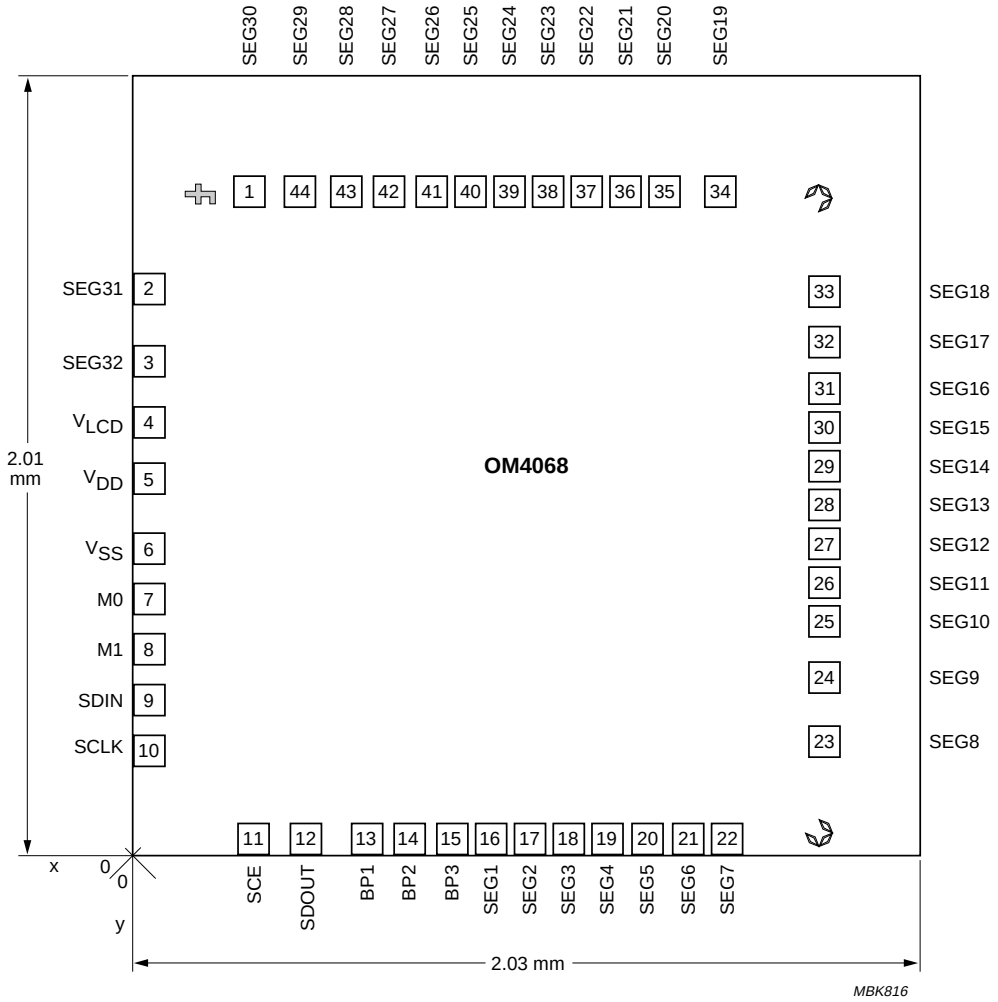



Fig.11 Serial data timing.

## BONDING PAD LOCATIONS




Dimensions in mm.

Bonding pad dimensions: 80 × 80 μm.

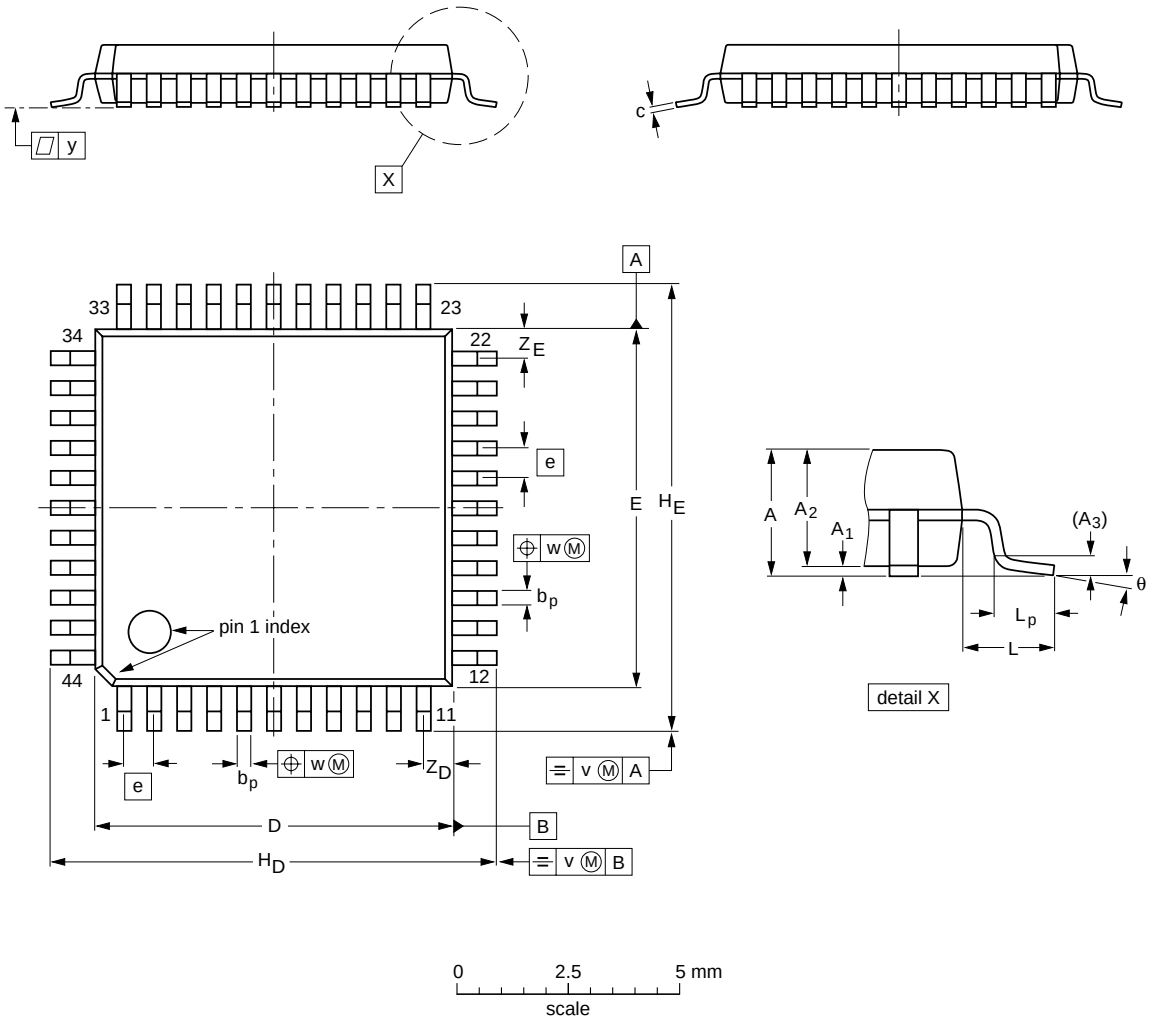
Fig.12 Bonding pad locations.

**Table 5** Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to bottom left corner of chip (see Fig.12).

| SYMBOL | PAD | x | y |
|---|---|---|---|
| $V_{DD}$ | 5 | 43.100 | 970.500 |
| $V_{SS}$ | 6 | 42.900 | 791.850 |
| M0 | 7 | 43.100 | 661.750 |
| M1 | 8 | 43.100 | 531.750 |
| SDIN | 9 | 43.100 | 401.750 |
| SCLK | 10 | 43.100 | 271.750 |
| SCE | 11 | 310.450 | 43.100 |
| SDOUT | 12 | 447.350 | 43.100 |
| BP1 | 13 | 604.800 | 43.100 |
| BP2 | 14 | 714.850 | 43.100 |
| BP3 | 15 | 824.850 | 43.100 |
| SEG1 | 16 | 924.850 | 43.100 |
| SEG2 | 17 | 1024.850 | 43.100 |
| SEG3 | 18 | 1124.850 | 43.100 |
| SEG4 | 19 | 1224.850 | 43.100 |
| SEG5 | 20 | 1327.250 | 43.100 |
| SEG6 | 21 | 1432.450 | 43.100 |
| SEG7 | 22 | 1532.650 | 43.100 |
| SEG8 | 23 | 1783.600 | 293.850 |
| SEG9 | 24 | 1783.600 | 458.850 |
| SEG10 | 25 | 1783.600 | 603.850 |
| SEG11 | 26 | 1783.600 | 703.850 |
| SEG12 | 27 | 1783.600 | 803.850 |
| SEG13 | 28 | 1783.600 | 903.850 |
| SEG14 | 29 | 1783.600 | 1003.850 |
| SEG15 | 30 | 1783.600 | 1103.850 |
| SEG16 | 31 | 1783.600 | 1203.850 |
| SEG17 | 32 | 1783.600 | 1323.850 |
| SEG18 | 33 | 1783.600 | 1453.850 |
| SEG19 | 34 | 1514.600 | 1711.100 |
| SEG20 | 35 | 1370.550 | 1711.100 |
| SEG21 | 36 | 1270.500 | 1711.100 |
| SEG22 | 37 | 1170.500 | 1711.100 |
| SEG23 | 38 | 1070.500 | 1711.100 |
| SEG24 | 39 | 970.550 | 1711.100 |
| SEG25 | 40 | 870.550 | 1711.100 |
| SEG26 | 41 | 770.550 | 1711.100 |
| SEG27 | 42 | 660.550 | 1711.100 |
| SEG28 | 43 | 550.550 | 1711.100 |
| SEG29 | 44 | 430.550 | 1711.100 |
| SEG30 | 1 | 300.550 | 1711.100 |
| SEG31 | 2 | 43.100 | 1460.050 |
| SEG32 | 3 | 43.100 | 1274.950 |
| $V_{LCD}$ | 4 | 43.100 | 1158.700 |
| **Alignment marks** | | | |
| C1 | – | 1769.6 | 1696.9 |
| C2 | – | 1770.1 | 58.4 |
| F | – | 172.0 | 1705.2 |

## PACKAGE OUTLINES

**QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm** **SOT307-2**




**DIMENSIONS (mm are the original dimensions)**

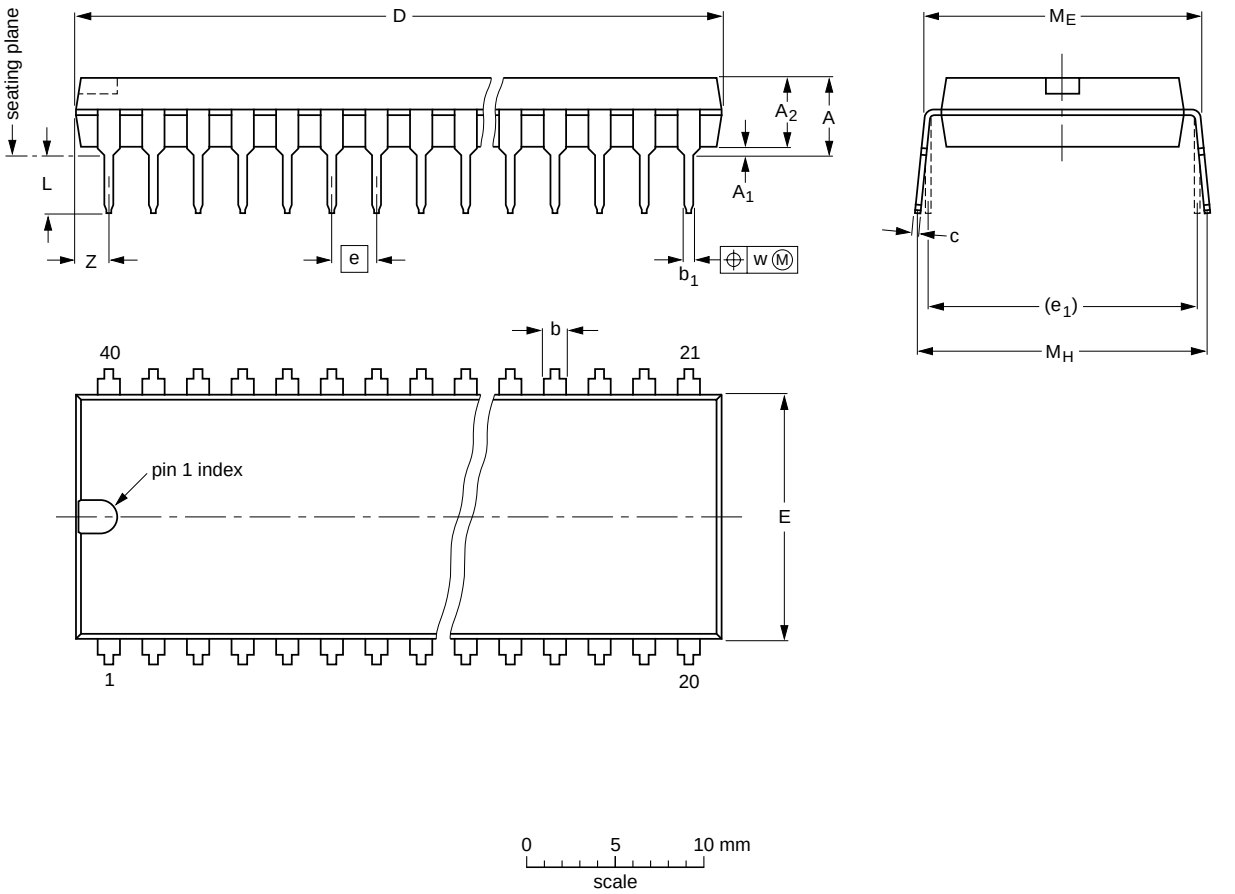
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.10 | 0.25<br>0.05 | 1.85<br>1.65 | 0.25 | 0.40<br>0.20 | 0.25<br>0.14 | 10.1<br>9.9 | 10.1<br>9.9 | 0.8 | 12.9<br>12.3 | 12.9<br>12.3 | 1.3 | 0.95<br>0.55 | 0.15 | 0.15 | 0.1 | 1.2<br>0.8 | 1.2<br>0.8 | $10^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT307-2 | | | | | | ~~95-02-04~~<br>97-08-01 |

**DIP40: plastic dual in-line package; 40 leads (600 mil)** **SOT129-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 4.0 | 1.70<br>1.14 | 0.53<br>0.38 | 0.36<br>0.23 | 52.50<br>51.50 | 14.1<br>13.7 | 2.54 | 15.24 | 3.60<br>3.05 | 15.80<br>15.24 | 17.42<br>15.90 | 0.254 | 2.25 |
| inches | 0.19 | 0.020 | 0.16 | 0.067<br>0.045 | 0.021<br>0.015 | 0.014<br>0.009 | 2.067<br>2.028 | 0.56<br>0.54 | 0.10 | 0.60 | 0.14<br>0.12 | 0.62<br>0.60 | 0.69<br>0.63 | 0.01 | 0.089 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT129-1 | 051G08 | MO-015AJ | | | | ~~92-11-17~~<br>95-01-14 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### DIP

#### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### QFP

#### Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

#### Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

| **CAUTION** |
| --- |
| **Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.** |

**If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
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| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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**NOTES**

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