TDA9901

Wideband differential digital controlled variable gain amplifier

Rev. 04 — 14 August 2008 Product data sheet

1. General description

The TDA9901 is a wideband, low-noise amplifier with differential inputs and outputs. The TDA9901 incorporates an Automatic Gain Control (AGC) function with digital control. The TDA9901 is optimized for fast switching between different gain settings, preserving small phase and amplitude error.

The TDA9901 presents an excellent combination of low noise and good linearity for a wide input frequency range. The TDA9901 is optimized for processing Input Frequency (IF) signals. It is also suited for many other applications as a general purpose digitally controlled variable gain amplifier.

The TDA9901 is able to operate from 4.75 V to 5.25 V supply for the analog part and from 3.0 V to 5.25 V for the digital part.

2. Features

- 130 MHz, –3 dB small signal bandwidth
- Digitally controlled gain
- Transistor-Transistor Logic (TTL) and CMOS compatible digital inputs (3.3 V or 5 V)
- TTL single-ended or differential clock input with Positive Emitter-Coupled Logic (PECL) compatibility
- 24 dB gain control range
- Four steps of 6 dB plus 6 dB fixed gain
- 30 dB gain maximum
- High impedance differential inputs
- Low impedance differential inputs
- High power supply rejection
- 125 nV/√Hz output voltage noise density at 30 dB gain
- Fast gain settling
- Dual control modes: transparent or latched

3. Applications

- Linear AGC systems
- Wireless infrastructure
- Fixed network
- Instrumentation
- Multipurpose amplifier
- Driver for differential ADCs (e.g. ADC1206S040/055/070 and ADC1006055/070)

4. Quick reference data

Table 1. Quick reference data

V_{DDA} = V11 to V12 = 4.75 V to 5.25 V; V_{DDD} = V18 to V17 = 3.0 V to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCA} = 5.0 V; V_{CCD} = 3.3 V and T_{amb} = 25 °C unless otherwise specified [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
I_{DDA}	analog supply current		-	30	36	mA
I_{DDD}	digital supply current		-	3.0	5.0	mA
G_{min}	minimum gain	DC input:				
		T_{amb} = 25 °C	5.78	6.11	6.40	dB
		all temperatures	5.7	6.11	6.46	dB
G_{max}	maximum gain	DC input:				
		T_{amb} = 25 °C	29.9	30.5	30.9	dB
		all temperatures	29.3	30.5	31.5	dB
$B_{\_3dB}$	−3 dB bandwidth	$V_{o(dif)(p-p)}$ = 0.125 V; T_{amb} = 25 °C	110	130	-	MHz
P_{tot}	total power dissipation		-	160	216	mW

[1] Due to on-chip regulator behavior a warm-up time of 1 minute (typical) is recommended for optimal performance.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9901TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

6. Block diagram

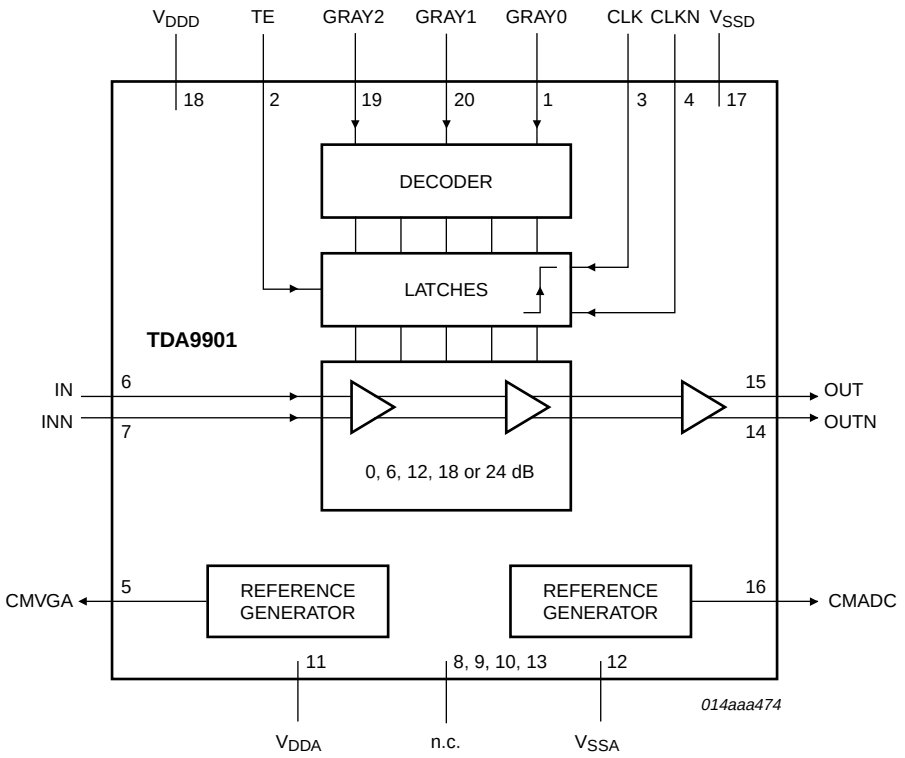


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

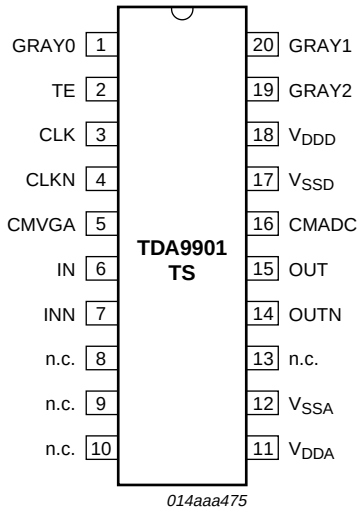


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GRAY0	1	digital control signal bit 0 input (Least Significant Bit (LSB))
TE	2	transparent enable input
CLK	3	clock input for gain control setting
CLKN	4	inverting clock input for gain control setting (active LOW)
CMVGA	5	regulator output common mode VGA input
IN	6	non-inverting analog input
INN	7	inverting analog input (active LOW)
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected
OUTN	14	inverting analog output (active LOW)
OUT	15	non-inverting analog output
CMADC	16	regulator output common mode ADC input
V_{SSD}	17	digital ground

Table 3. Pin description *…continued*

Symbol	Pin	Description
V_{DDD}	18	digital supply voltage
GRAY2	19	digital control signal bit 2 input (Most Significant Bit (MSB))
GRAY1	20	digital control signal bit 1 input

8. Functional description

The TDA9901 provides a digitally controlled variable gain function for high-frequency applications.

The TDA9901 can be operated in two different modes, depending on the value at pin TE. When TE is at logic 1, the gain can be instantly controlled when the clock signal is HIGH (transparent mode). The gain is fixed during the LOW period of the clock. When TE is at logic 0 the gain of the TDA9901 is changed at the rising edge of the clock signal.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.3	+7.0	V
V_{DDD}	digital supply voltage		–0.3	+7.0	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDD}$	–0.1	+4.0	V
V_I	input voltage		–0.3	+7.0	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W

11. Characteristics

Table 6. Characteristics

V_{DDA} = V11 to V12 = 4.75 V to 5.25 V; V_{DDD} = V18 to V17 = 3.0 V to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCA} = 5.0 V; V_{CCD} = 3.3 V and T_{amb} = 25 °C unless otherwise specified [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDD}$	−0.2	-	+2.5	V
I_{DDA}	analog supply current		-	30	36	mA
I_{DDD}	digital supply current		-	3.0	5.0	mA
P_{tot}	total power dissipation		-	160	216	mW
Variable gain amplifier transfer characteristics						
$B_{\_3dB}$	−3 dB bandwidth	$V_{o(dif)(p-p)}$ = 0.125 V; T_{amb} = 25 °C	110	130	-	MHz
$t_{d(grp)}$	group delay time	up to f_i = 20 MHz; minimum gain; T_{amb} = 25 °C	-	2.5	-	ns
$\Delta t_{d(grp)}$	group delay time variation	6 dB gain step; T_{amb} = 25 °C	-	-	300	ps
t_s	settling time	10 % to 90 % maximum output transition; $C_{L(max)}$ = 5 pF on each output; T_{amb} = 25 °C	-	-	3.6	ns
G_{step}	step of gain	DC input:				
		T_{amb} = 25 °C	5.88	6.09	6.28	dB
		all temperatures	5.6	6.09	6.56	dB
G_{min}	minimum gain	DC input:				
		T_{amb} = 25 °C	5.78	6.11	6.40	dB
		all temperatures	5.7	6.11	6.46	dB
G_{max}	maximum gain	DC input:				
		T_{amb} = 25 °C	29.9	30.5	30.9	dB
		all temperatures	29.3	30.5	31.5	dB
$\Delta G/\Delta T$	gain variation with temperature	minimum gain	-	−1.0	-	mdB/°C
		maximum gain	-	−7.5	-	mdB/°C
$\Delta G/\Delta V_{CC}$	gain variation with supply voltage	minimum gain	-	15	25	mdB/V
$\Delta V_{i(offset)}$	offset input voltage variation	6 dB gain step	-	0.8	-	mV
NF	noise figure	R_S = 100 Ω; f_i = 20 MHz				
		minimum gain	-	29.1	-	dB
		maximum gain	-	9.9	-	dB

Table 6. Characteristics *...continued*

V_{DDA} = V11 to V12 = 4.75 V to 5.25 V; V_{DDD} = V18 to V17 = 3.0 V to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCA} = 5.0 V; V_{CCD} = 3.3 V and T_{amb} = 25 °C unless otherwise specified [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{n(o)(eq)}$	equivalent output noise voltage	R_s = 100 Ω; f_i = 20 MHz; T_{amb} = 25 °C				
		G = 6 dB	-	75	-	nV/√Hz
		G = 12 dB	-	82	-	nV/√Hz
		G = 18 dB	-	97	-	nV/√Hz
		G = 24 dB	-	91	-	nV/√Hz
		G = 30 dB	-	124	-	nV/√Hz
PSRR	power supply rejection ratio	minimum gain; V_{DDA}				
		0 MHz to 20 MHz	-	57	-	dB
		20 MHz to 100 MHz	-	39	-	dB
		minimum gain; V_{DDD}				
		0 MHz to 20 MHz	-	67	-	dB
		20 MHz to 100 MHz	-	51	-	dB
CMRR	common mode rejection ratio	0 MHz to 20 MHz	-	75	-	dB
		20 MHz to 100 MHz	-	45	-	dB
Analog inputs						
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	minimum gain	-	1.0	-	V
		maximum gain	-	60.4	-	mV
$V_{i(cm)}$	common-mode input voltage		2.0	2.7	V_{DDA} − 1.9	V
I_i	input current	$V_{i(cm)}$ = 2.7 V	-	55	-	µA
R_i	input resistance		10	-	-	kΩ
C_i	input capacitance		-	-	5	pF
Analog outputs [2]						
$V_{o(dif)(p-p)max}$	maximum peak-to-peak differential output voltage	maximum gain	2.0	-	-	V
		minimum gain	2.0	-	-	V
$V_{O(cm)}$	common-mode output voltage	referenced to V_{DDA}; T_{amb} = 25 °C	V_{DDA} − 2.56	V_{DDA} − 2.42	V_{DDA} − 2.29	V
$\Delta V_{O(cm)}/\Delta T$	common-mode output voltage variation with temperature		-	−1.8	-	mV/°C
SR_{se}	single-ended slew rate		-	275	-	V/µs
R_o	output resistance		-	15	26	Ω
C_o	output capacitance		-	3	-	pF
Variable gain amplifier dynamic performance; C_L = 5 pF; R_L = 680 Ω; see Figure 6, 7, 8, 9 and 10						
α_{2H}	second harmonic level	$V_o = V_{o(max)}$				
		f_i = 0.5 MHz	-	−80	−67	dBc
		f_i = 4.43 MHz	-	−77	−67	dBc
		f_i = 12.5 MHz	-	−76	−65	dBc
		f_i = 21.4 MHz	-	−74	−62	dBc

Table 6. Characteristics *...continued*

V_{DDA} = V11 to V12 = 4.75 V to 5.25 V; V_{DDD} = V18 to V17 = 3.0 V to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCA} = 5.0 V; V_{CCD} = 3.3 V and T_{amb} = 25 °C unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{3H}	third harmonic level	$V_o = V_{o(max)}$; T_{amb} = 25 °C					
		f_i = 0.5 MHz		-	−64	−60	dBc
		f_i = 4.43 MHz		-	−64	−59	dBc
		f_i = 12.5 MHz		-	−62	−58	dBc
		f_i = 21.4 MHz		-	−61	−57	dBc
$\Delta\alpha_{3H}/\Delta T$	third harmonic level variation with temperature	f_i = 21.4 MHz		-	80	-	mdB/°C
Reference voltage output ADC: pin CMADC							
V_{ref}	reference voltage	referenced to V_{DDA}; T_{amb} = 25 °C		V_{DDA} − 1.64	V_{DDA} − 1.45	V_{DDA} − 1.26	V
R_o	output resistance	T_{amb} = 25 °C		-	17	26	Ω
$\Delta V_{o(ref)}/\Delta T$	reference output voltage variation with temperature			-	−0.11	-	mV/°C
$I_{o(max)}$	maximum output current			-	1.0	-	mA
C_o	output capacitance			-	3	-	pF
Reference voltage output VGA: pin CMVGA							
V_{ref}	reference voltage	referenced to V_{DDA}; T_{amb} = 25 °C		V_{DDA} − 2.48	V_{DDA} − 2.30	V_{DDA} − 2.17	V
R_o	output resistance	T_{amb} = 25 °C		-	9	20	Ω
$\Delta V_{o(ref)}/\Delta T$	reference output voltage variation with temperature			-	1.75	-	mV/°C
$I_{o(max)}$	maximum output current			-	1.0	-	mA
C_o	output capacitance			-	3	-	pF
Gain switching characteristics (in latched mode); f_{clk} = 52 MHz; T_{amb} = 25 °C; see Figure 3							
t_h	hold time			2.0	-	-	ns
t_{su}	set-up time			3.8	-	-	ns
t_w	pulse width			5.8	-	-	ns
t_{PD}	propagation delay			-	4.2	5.9	ns
t_s	settling time	10 % to 90 % full scale if ±6 dB gain change	[3]	-	2.6	3.2	ns
Gain switching characteristics (in transparent mode); f_{clk} = 52 MHz; T_{amb} = 25 °C; see Figure 4							
t_{PD}	propagation delay			-	6.7	9.5	ns
t_s	settling time	10 % to 90 % full scale if ±6 dB gain change	[4]	-	5.4	6.9	ns
Clock timing input: pins CLK and CLKN (see Figure 3)							
$f_{clk(max)}$	maximum clock frequency			52	-	-	MHz
$t_{w(clk)L}$	LOW clock pulse width			4.0	-	-	ns
$t_{w(clk)H}$	HIGH clock pulse width			4.0	-	-	ns

Table 6. Characteristics *...continued*

V_{DDA} = V11 to V12 = 4.75 V to 5.25 V; V_{DDD} = V18 to V17 = 3.0 V to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCA} = 5.0 V; V_{CCD} = 3.3 V and T_{amb} = 25 °C unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time			-	4.0	-	ns
t_f	fall time			-	4.0	-	ns
Digital inputs: pins TE, GRAY0, GRAY1 and GRAY2							
V_{IL}	LOW-level input voltage			0	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	V_{DDD}	V
I_{IH}	HIGH-level input current			−10	-	+10	µA
I_{IL}	LOW-level input current			−10	-	+10	µA
C_i	input capacitance			-	-	3	pF
Clock inputs in TTL mode							
V_{IL}	LOW-level input voltage		[5]	0	-	0.8	V
V_{IH}	HIGH-level input voltage		[5]	2.0	-	V_{DDD}	V
I_{IH}	HIGH-level input current			15	-	80	µA
I_{IL}	LOW-level input current			−40	-	−10	µA
C_i	input capacitance			-	-	2	pF
Clock inputs in differential mode							
V_{IL}	LOW-level input voltage	V_{DDA} = 5.0 V	[6]	3.19	-	3.52	V
V_{IH}	HIGH-level input voltage	V_{DDA} = 5.0 V	[6]	3.83	-	4.12	V
I_{IH}	HIGH-level input current			15	-	80	µA
I_{IL}	LOW-level input current			−40	-	−5	µA
C_i	input capacitance			-	-	2	pF
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage	DC voltage level = 2.5 V		0.1	-	2.0	V

[1] Due to the behavior of the on-chip regulator a warm-up time of 1 minute (typical) is recommended for optimal performance.

[2] The analog output voltages are positive with respect to V_{SSA}.

[3] In latching mode (pin TE LOW), the gain settling is latched at the rising edge of the clock input.

[4] In transparent mode, the gain settling is directly controlled by the input data pattern.

[5] The circuit may be used with a single TTL clock on CLK or CLKN. The unused clock pin has to be decoupled to ground with a 100 nF capacitance.

[6] There are four modes of operation for the clock inputs in non-TTL mode:

a) PECL mode 1: (DC level vary 1 : 1 with V_{DDA}) CLK and CLKN inputs are differential PECL levels.

b) PECL mode 2: (DC level vary 1 : 1 with V_{DDA}) CLK input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLKN decoupled to V_{SSD} via a 100 nF capacitor.

c) PECL mode 3: (DC level vary 1 : 1 with V_{DDA}) CLKN input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLK decoupled to V_{SSD} via a 100 nF capacitor.

d) AC driving mode 4: when driving the CLK input directly and with any AC signal of minimum 0.1 V (p-p) and with a DC level of 2.5 V, the gain change takes place on the rising edge of the clock signal. When driving the CLKN input with the same signal, gain change takes place on the falling edge of the clock signal. NXP Semiconductors recommends decoupling of the CLKN or CLK input to V_{SSD} via a 100 nF capacitor.

12. Additional information relating to Table 6

Table 7. Input coding

State	Gray input data code			Gain (dB)
	Pins Gray2, Gray1, Gray0			
	D2	D1	D0	
0	0	0	0	minimum
1	0	0	1	minimum + 6
2	0	1	1	minimum + 12
3	0	1	0	minimum + 18
4	1	1	0	minimum + 24
other	-	-	-	minimum + 24

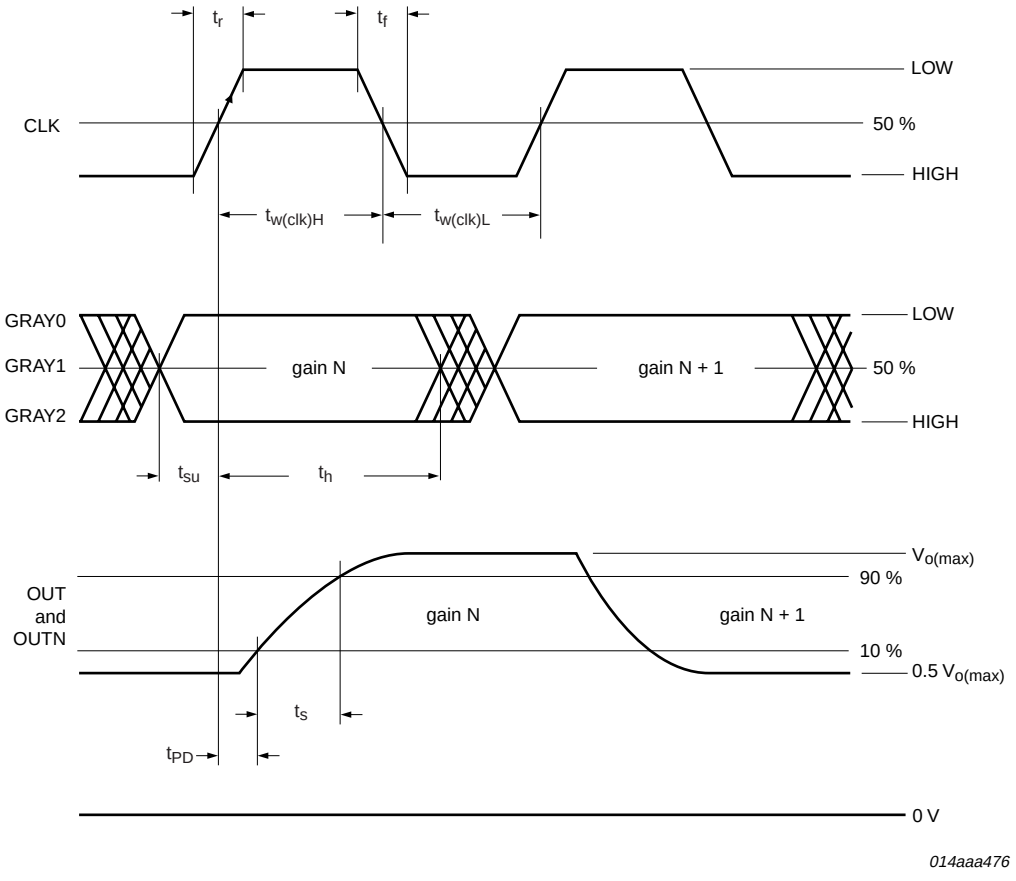


Fig 3. Latched mode timing diagram

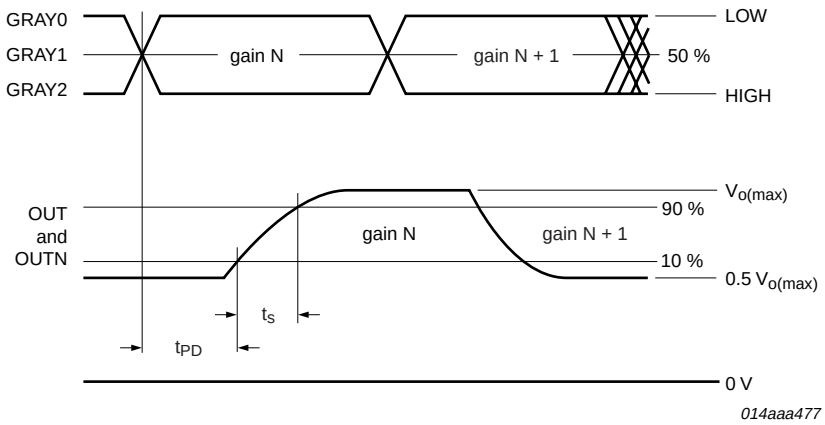
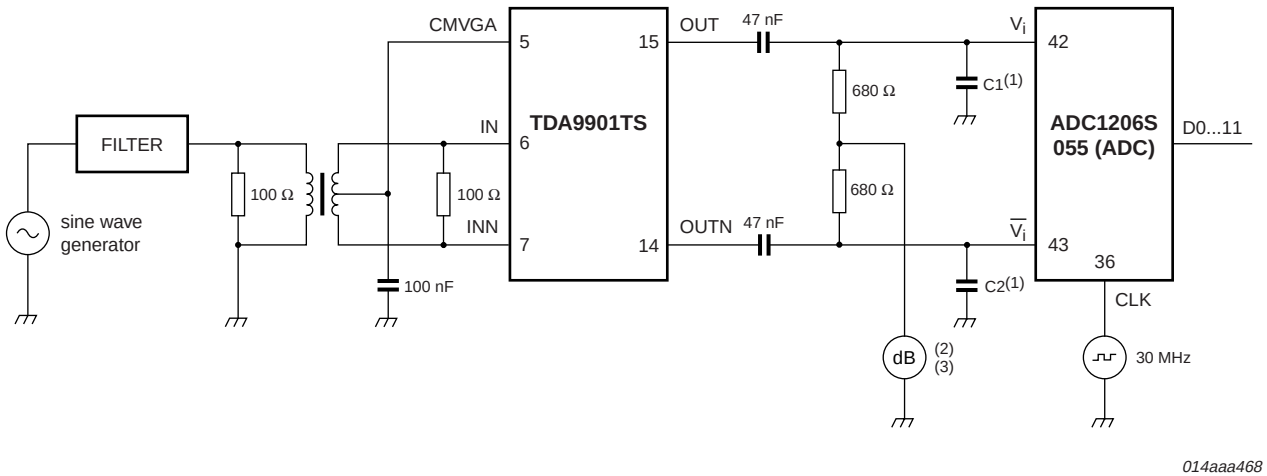


Fig 4. Transparent mode timing diagram with CLK HIGH

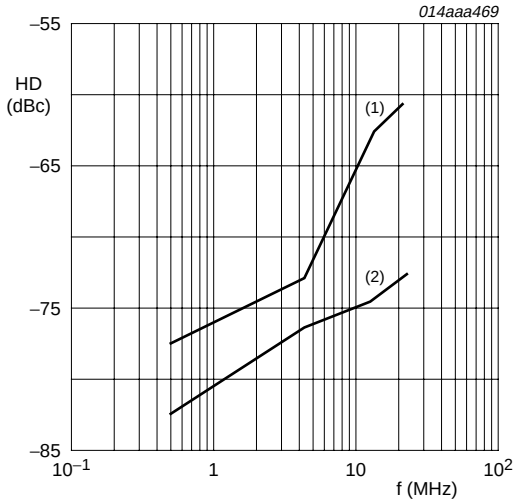


(1) C1 and C2 represent the board line capacitance. They represent about 5 pF with the ADC1206S040/055/070 input capacitance. Special care has to be taken to minimize this load in order to have the best dynamic performance.

(2) The α_{2H} and α_{3H} of the ADC1206S040/055/070 is lower than that measured on the TDA9901. This measurement method is preferred to conventional methods due to its low contribution to the α_{2H}.

(3) The chain measurement shows the harmonic distortion of the TDA9901 as the measurement from ADC1206S040/055/070 is negligible.

Fig 5. Dynamic distortion measurement diagram

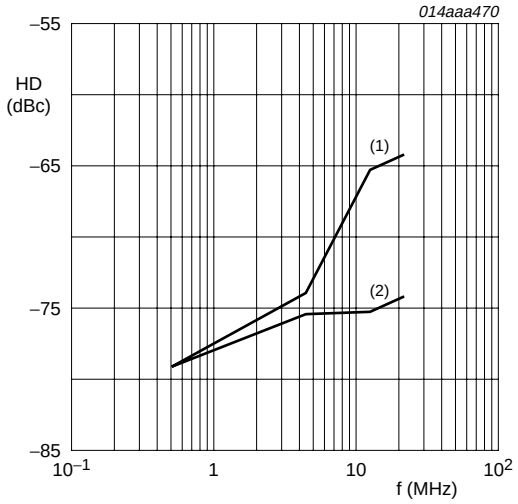


(1) α_{3H}.

(2) α_{2H}.

Typical condition; 2 V (p-p) differential output

Fig 6. Harmonic Distortion (HD) as a function of frequency for minimum gain

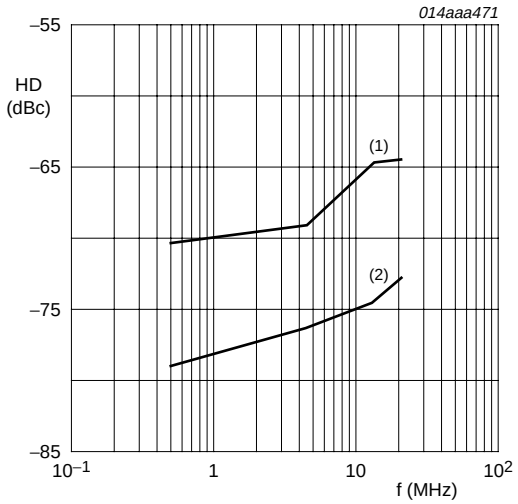


(1) α_{3H}.

(2) α_{2H}.

Typical condition; 2 V (p-p) differential output

Fig 7. Harmonic Distortion (HD) as a function of frequency for minimum gain plus 6 dB

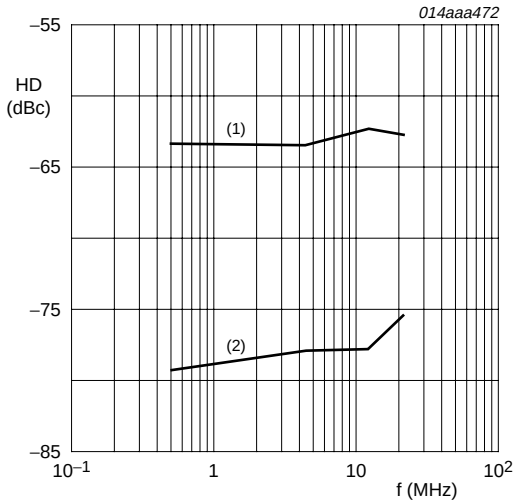


(1) α_{3H}.

(2) α_{2H}.

Typical condition; 2 V (p-p) differential output

Fig 8. Harmonic Distortion (HD) as a function of frequency for minimum gain plus 12 dB

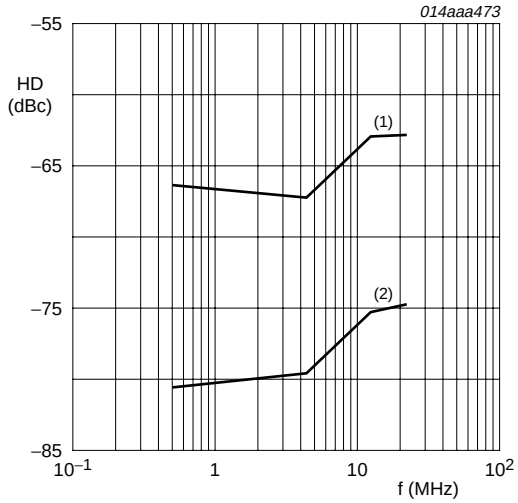


(1) α_{3H}.

(2) α_{2H}.

Typical condition; 2 V (p-p) differential output

Fig 9. Harmonic Distortion (HD) as a function of frequency for minimum gain plus 18 dB



(1) α_{3H}.

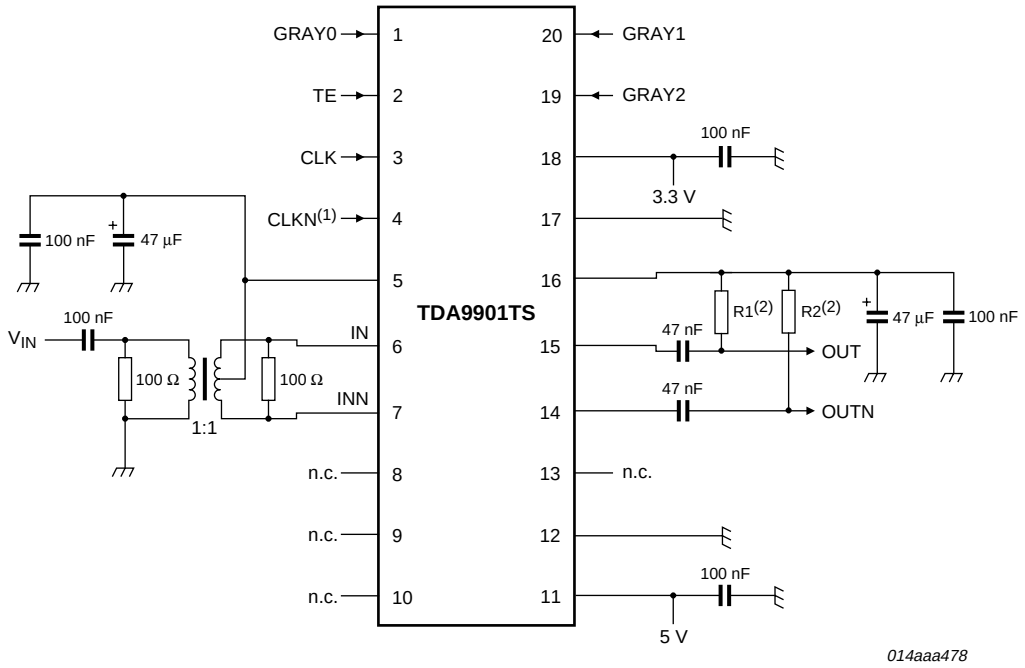
(2) α_{2H}.

Typical condition; 2 V (p-p) differential output

Fig 10. Harmonic Distortion (HD) as a function of frequency for minimum gain plus 24 dB

13. Application information

13.1 Application diagrams



(1) Single-ended clock signal can be applied if required.

(2) R1 and R2 should be at least 680 Ω.

Fig 11. Application diagram

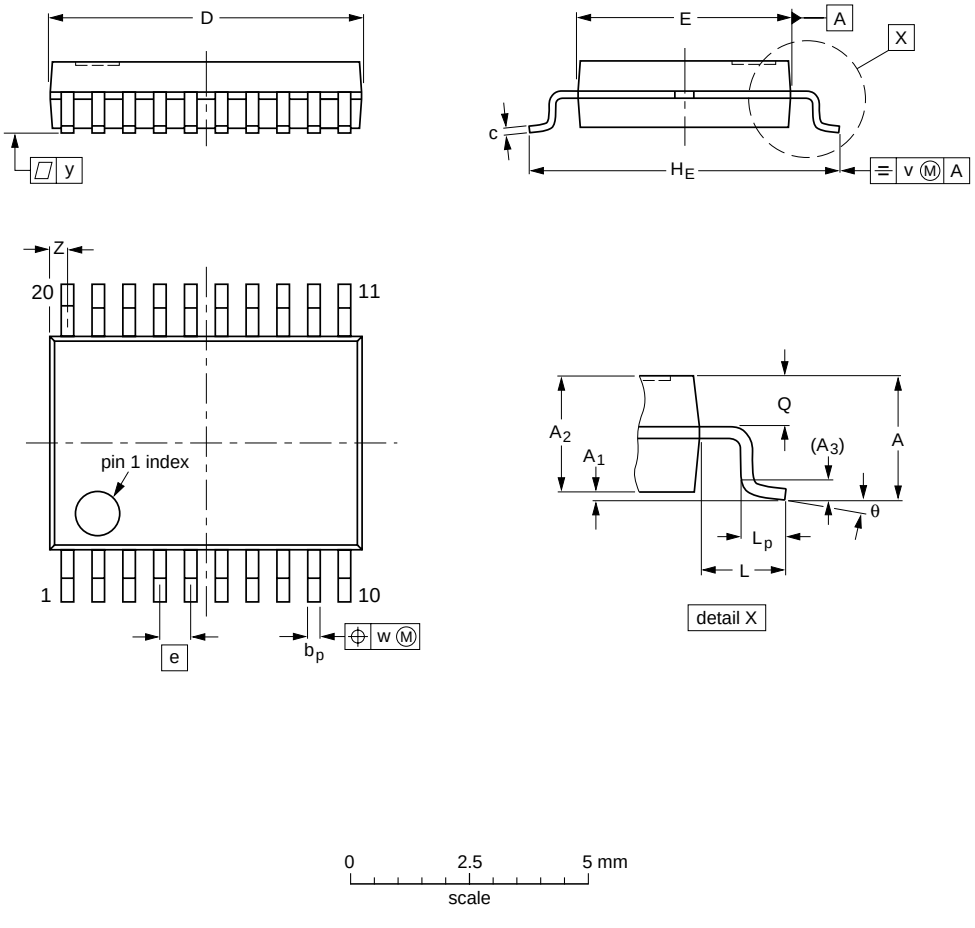
13.2 Recommended companion chip

Table 8. Recommended companion chips

Type number	Description	Sampling frequency
ADC1006S055	Single 10 bits ADC	55 MHz
ADC1006S070	Single 10 bits ADC	70 MHz
ADC1206S040	Single 12 bits ADC	40 MHz
ADC1206S055	Single 12 bits ADC	55 MHz
ADC1206S070	Single 12 bits ADC	70 MHz

14. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT266-1 (SSOP20)

15. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9901_4	20080814	Product data sheet	-	TDA9901_3
Modifications:	• Correction made to ΔV_{DD} conditions in Table 4. • Corrections made to values of $t_{d(grp)}$ and G_{step} in Table 6.			
TDA9901_3	20080611	Product specification	-	TDA9901_2
TDA9901_2	19991008	Product specification	-	TDA9901_N_1
TDA9901_N_1	19980415	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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