

## **IMPORTANT NOTICE**

*Dear customer,*

*As from February 2nd 2009, ST and Ericsson have merged Ericsson Mobile Platforms and ST-NXP Wireless into a 50/50 joint venture "ST-Ericsson".*

*As a result, the following changes are applicable to the attached document.*

- **Company name** - *ST-NXP Wireless* is replaced with **ST-Ericsson**.
- **Copyright** - the copyright notice at the bottom of each page "© ST-NXP Wireless 200x - All rights reserved", shall now read: "© ST-Ericsson, 2009 - All rights reserved".
- **Web site** - <http://www.stnwireless.com> is replaced with [www.stericsson.com](http://www.stericsson.com)
- **Contact information** - the list of sales offices previously obtained at <http://www.stnwireless.com>, is now found at [www.stericsson.com](http://www.stericsson.com) under Contacts

*If you have any questions related to the document, please contact our nearest sales office.*

*Thank you for your cooperation and understanding.*



# ISP1105/1106

Advanced USB transceivers

Rev. 09 — 19 January 2009

Product data sheet

## 1. General description

The ISP1105/1106 range of Universal Serial Bus (USB) transceivers are compliant with the *Universal Serial Bus Specification Rev. 2.0*. They can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates. The ISP1105/1106 range can be used as a USB device transceiver or a USB host transceiver.

They allow USB Application Specific ICs (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 V to 3.6 V to interface with the physical layer of the Universal Serial Bus. They have an integrated 5 V-to-3.3 V voltage regulator for direct powering via the USB supply  $V_{BUS}$ .

ISP1105 allows single-ended and differential input modes selectable by a MODE input and it is available in HVQFN16 and HBCC16 packages. ISP1106 allows only differential input mode and is available in both TSSOP16 and HBCC16 packages.

The ISP1105/1106 are ideal for portable electronics devices such as mobile phones, digital still cameras, Personal Digital Assistants (PDA) and Information Appliances (IA).

## 2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Integrated bypassable 5 V-to-3.3 V voltage regulator for powering via USB  $V_{BUS}$
- $V_{BUS}$  disconnection indication through VP and VM
- Used as a USB device transceiver or a USB host transceiver
- Stable RCV output during SE0 condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports an I/O voltage range from 1.65 V to 3.6 V
- $\pm 12$  kV ESD protection at the D+, D-,  $V_{CC(5.0)}$  and GND pins
- Full industrial operating temperature range from  $-40$  °C to  $+85$  °C
- Available in small HBCC16, HVQFN16 (only ISP1105) and TSSOP16 (only ISP1106) packages; HBCC16 and HVQFN16 are lead-free and halogen-free packages.

# ST-NXP Wireless

### 3. Applications

- Portable electronic devices, such as:
  - ◆ Mobile phone
  - ◆ Digital still camera
  - ◆ Personal Digital Assistant (PDA)
  - ◆ Information Appliance (IA).

### 4. Ordering information

**Table 1. Ordering information**

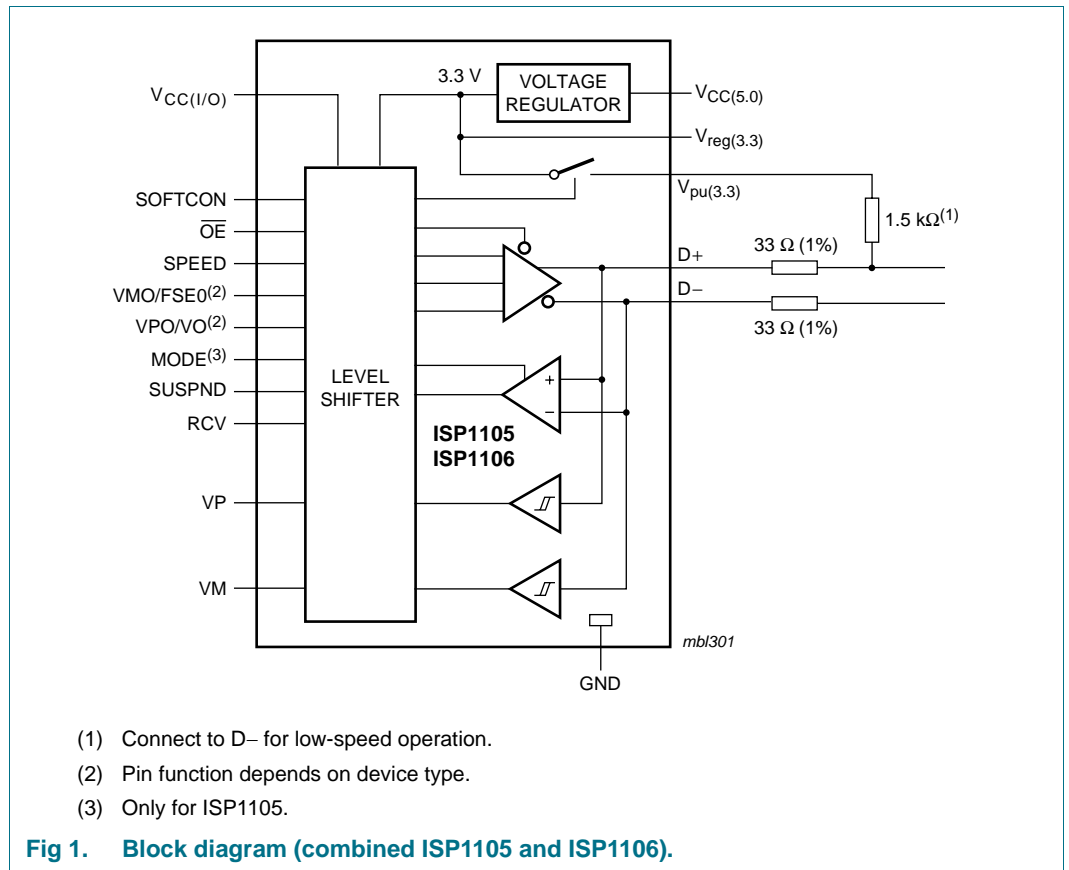
Type number	Package		Version
	Name	Description	
ISP1105BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
ISP1105W	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2
ISP1106DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
ISP1106W	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

#### 4.1 Ordering options

**Table 2. Selection guide**

Product	Package	Description
ISP1105	HVQFN16 and HBCC16	supports both single-ended and differential input modes; see <a href="#">Table 5</a> and <a href="#">Table 6</a> .
ISP1106	TSSOP16 and HBCC16	supports only the differential input mode; see <a href="#">Table 6</a> .

5. Block diagram



## 6. Pinning information

### 6.1 Pinning

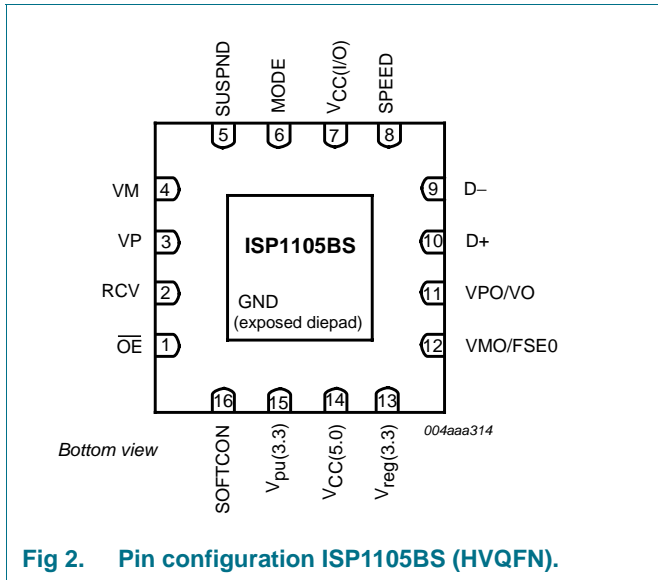


Fig 2. Pin configuration ISP1105BS (HVQFN).

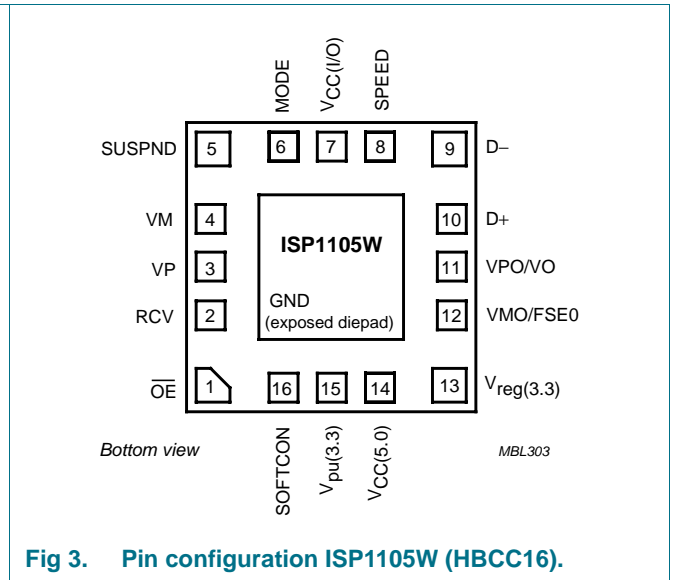


Fig 3. Pin configuration ISP1105W (HBCC16).

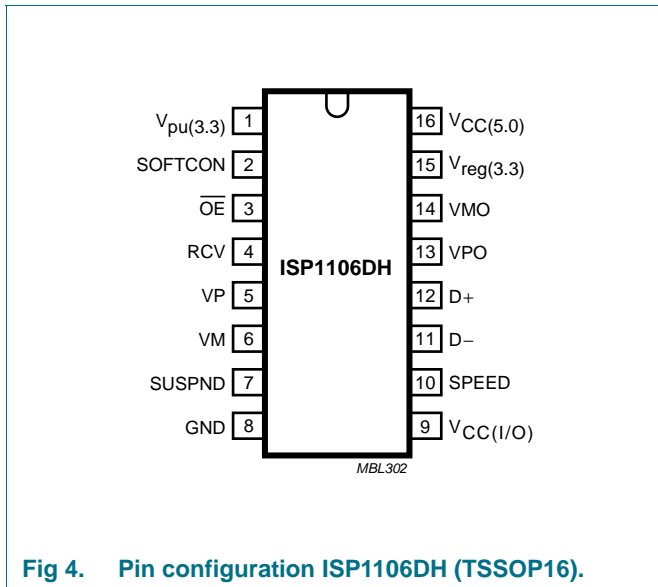


Fig 4. Pin configuration ISP1106DH (TSSOP16).

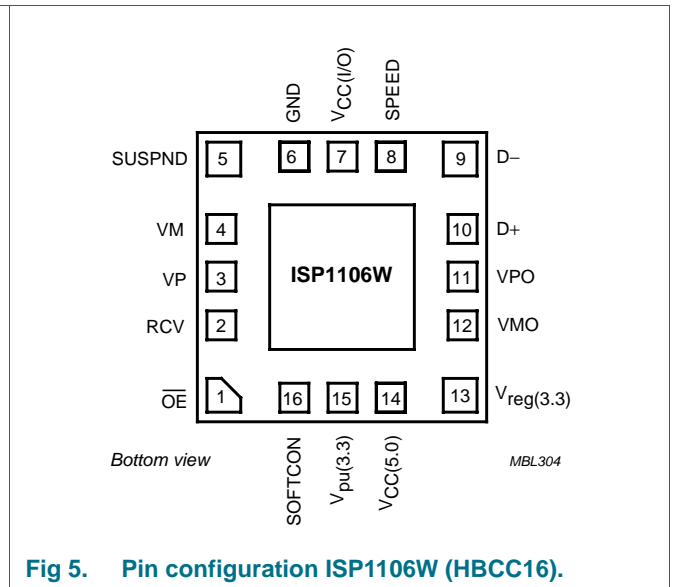


Fig 5. Pin configuration ISP1106W (HBCC16).

## 6.2 Pin description

Table 3. Pin description

Symbol <sup>[1]</sup>	Pin				Type	Description
	ISP1105		ISP1106			
	BS	W	DH	W		
$\overline{\text{OE}}$	1	1	3	1	I	output enable input (CMOS level with respect to $V_{\text{CC(I/O)}}$ , active LOW); enables the transceiver to transmit data on the USB bus input pad; push pull; CMOS
RCV	2	2	4	2	O	differential data receiver output (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); driven LOW when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition output pad; push pull; 4 mA output drive; CMOS
VP	3	3	5	3	O	single-ended D+ receiver output (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when no supply voltage is connected to $V_{\text{CC(5.0)}}$ and $V_{\text{reg(3.3)}}$ output pad; push pull; 4 mA output drive; CMOS
VM	4	4	6	4	O	single-ended D– receiver output (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when no supply voltage is connected to $V_{\text{CC(5.0)}}$ and $V_{\text{reg(3.3)}}$ output pad; push pull; 4 mA output drive; CMOS
SUSPND	5	5	7	5	I	suspend input (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level input pad; push pull; CMOS
MODE	6	6	-	-	I	mode input (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); a HIGH level enables the differential input mode (VPO, VMO) whereas a LOW level enables a single-ended input mode (VO, FSE0); see <a href="#">Table 5</a> and <a href="#">Table 6</a> input pad; push pull; CMOS
GND	die pad	die pad	8	6	-	ground supply <sup>[2]</sup>
$V_{\text{CC(I/O)}}$	7	7	9	7	-	supply voltage for digital I/O pins (1.65 V to 3.6 V). When $V_{\text{CC(I/O)}}$ is not connected, the (D+, D–) pins are in three-state; this supply pin is totally independent of $V_{\text{CC(5.0)}}$ and $V_{\text{reg(3.3)}}$ and must never exceed the $V_{\text{reg(3.3)}}$ voltage
SPEED	8	8	10	8	I	speed selection input (CMOS level with respect to $V_{\text{CC(I/O)}}$ ); adjusts the slew rate of differential data outputs D+ and D– according to the transmission speed <b>LOW</b> — low-speed (1.5 Mbit/s) <b>HIGH</b> — full-speed (12 Mbit/s) input pad; push pull; CMOS
D–	9	9	11	9	A/I/O	negative USB data bus connection (analog, differential); for low-speed mode connect to pin $V_{\text{pu(3.3)}}$ via a 1.5 k $\Omega$ resistor
D+	10	10	12	10	A/I/O	positive USB data bus connection (analog, differential); for full-speed mode connect to pin $V_{\text{pu(3.3)}}$ via a 1.5 k $\Omega$ resistor

Table 3. Pin description ...continued

Symbol <sup>[1]</sup>	Pin				Type	Description
	ISP1105		ISP1106			
	BS	W	DH	W		
VPO/VO	11	11	-	-	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$ , Schmitt trigger); see <a href="#">Table 5</a> and <a href="#">Table 6</a>
VPO	-	-	13	11		input pad; push pull; CMOS
VO	-	-	-	-		
VMO/FSE0	12	12	-	-	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$ , Schmitt trigger); see <a href="#">Table 5</a> and <a href="#">Table 6</a>
VMO	-	-	14	12		input pad; push pull; CMOS
FSE0	-	-	-	-		
$V_{reg(3.3)}$	13	13	15	13	-	<b>internal regulator option:</b> regulated supply voltage output (3.0 V to 3.6 V) during 5 V operation; a decoupling capacitor of at least 0.1 $\mu$ F is required <b>regulator bypass option:</b> used as a supply voltage input for 3.3 V $\pm$ 10 % operation
$V_{CC(5.0)}$	14	14	16	14	-	<b>internal regulator option:</b> supply voltage input (4.0 V to 5.5 V); can be connected directly to USB supply $V_{BUS}$ <b>regulator bypass option:</b> connect to $V_{reg(3.3)}$
$V_{pu(3.3)}$	15	15	1	15	-	pull-up supply voltage (3.3 V $\pm$ 10 %); connect an external 1.5 k $\Omega$ resistor on D+ (full-speed) or D- (low-speed); pin function is controlled by input SOFTCON <b>SOFTCON = LOW</b> — $V_{pu(3.3)}$ floating (high impedance); ensures zero pull-up current <b>SOFTCON = HIGH</b> — $V_{pu(3.3)} = 3.3$ V; internally connected to $V_{reg(3.3)}$
SOFTCON	16	16	2	16	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin $V_{pu(3.3)}$ , which is connected to an external 1.5 k $\Omega$ pull-up resistor; this allows USB connect/disconnect signalling to be controlled by software input pad; push pull; CMOS

[1] Symbol names with an overscore (e.g.  $\overline{NAME}$ ) indicate active LOW signals.

[2] ISP1105: ground terminal is connected to the exposed die pad (heat sink).

## 7. Functional description

### 7.1 Function selection

**Table 4. Function table**

SUSPND	OE	(D+, D-)	RCV	VP/VM	Function
L	L	driving and receiving	active	active	normal driving (differential receiver active)
L	H	receiving <sup>[1]</sup>	active	active	receiving
H	L	driving	inactive <sup>[2]</sup>	active	driving during 'suspend' <sup>[3]</sup> (differential receiver inactive)
H	H	high-Z <sup>[1]</sup>	inactive <sup>[2]</sup>	active	low-power state

[1] Signal levels on (D+, D-) are determined by other USB devices and external pull-up/down resistors.

[2] In 'suspend' mode (SUSPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out-of-suspend ('K') signalling is detected via the single-ended receivers VP and VM.

[3] During suspend, the slew-rate control circuit of low-speed operation is disabled. The (D+, D-) lines are still driven to their intended states, without slew-rate control. This is permitted because driving during suspend is used to signal remote wake-up by driving a 'K' signal (one transition from idle to 'K' state) for a period of 1 to 15 ms.

### 7.2 Operating functions

**Table 5. Driving function (pin OE = L) using single-ended input data interface for ISP1105 (pin MODE = L)**

FSE0	VO	Data
L	L	differential logic 0
L	H	differential logic 1
H	L	SE0
H	H	SE0

**Table 6. Driving function (pin OE = L) using differential input data interface for ISP1105 (pin MODE = H) and ISP1106**

VMO	VPO	Data
L	L	SE0
L	H	differential logic 1
H	L	differential logic 0
H	H	illegal state

**Table 7. Receiving function (pin OE = H)**

(D+, D-)	RCV	VP <sup>[1]</sup>	VM <sup>[1]</sup>
Differential logic 0	L	L	H
Differential logic 1	H	H	L
SE0	RCV* <sup>[2]</sup>	L	L

[1] VP = VM = H indicates the sharing mode ( $V_{CC(5.0)}$  and  $V_{reg(3.3)}$  are disconnected).

[2] RCV\* denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.



### 7.3 Power supply configurations

The ISP1105/1106 can be used with different power supply configurations, which can be changed dynamically. An overview is given in [Table 9](#).

**Normal mode** — Both  $V_{CC(I/O)}$  and  $V_{CC(5.0)}$  or ( $V_{CC(5.0)}$  and  $V_{reg(3.3)}$ ) are connected. For 5 V operation,  $V_{CC(5.0)}$  is connected to a 5 V source (4.0 V to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3 V operation, both  $V_{CC(5.0)}$  and  $V_{reg(3.3)}$  are connected to a 3.3 V source (3.0 V to 3.6 V).  $V_{CC(I/O)}$  is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.

**Disable mode** —  $V_{CC(I/O)}$  is not connected,  $V_{CC(5.0)}$  or ( $V_{CC(5.0)}$  and  $V_{reg(3.3)}$ ) are connected. In this mode, the internal circuits of the ISP1105/1106 ensure that the (D+, D-) pins are in three-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of  $V_{CC(I/O)}$  lost.

**Sharing mode** —  $V_{CC(I/O)}$  is connected, ( $V_{CC(5.0)}$  and  $V_{reg(3.3)}$ ) are not connected. In this mode, the (D+, D-) pins are made three-state and the ISP1105/1106 allows external signals of up to 3.6 V to share the (D+, D-) lines. The internal circuits of the ISP1105/1106 ensure that virtually no current (maximum 10  $\mu$ A) is drawn via the (D+, D-) lines. The power consumption through pin  $V_{CC(I/O)}$  drops to the low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode. Pin RCV is made LOW. Some hysteresis is built into the detection of  $V_{reg(3.3)}$  lost.

**Table 8. Pin states in disable or sharing mode**

Pins	Disable mode state	Sharing mode state
$V_{CC(5.0)}$ / $V_{reg(3.3)}$	5 V input / 3.3 V output; 3.3 V input / 3.3 V input	not present
$V_{CC(I/O)}$	not present	1.65 V to 3.6 V input
$V_{pu(3.3)}$	high impedance (off)	high impedance (off)
(D+, D-)	high impedance	high impedance
(VP, VM)	invalid <sup>[1]</sup>	H
RCV	invalid <sup>[1]</sup>	L
Inputs (VO/VPO, FSE0/VMO, SPEED, MODE <sup>[2]</sup> , SUSPND, OE, SOFTCON)	high impedance	high impedance

[1] High impedance or driven LOW.

[2] ISP1105 only.

**Table 9. Power supply configuration overview**

$V_{CC(5.0)}$ or $V_{reg(3.3)}$	$V_{CC(I/O)}$	Configuration	Special characteristics
Connected	connected	normal mode	-
Connected	not connected	disable mode	(D+, D-) and $V_{pu(3.3)}$ high impedance; VP, VM, RCV: invalid <sup>[1]</sup>
Not connected	connected	sharing mode	(D+, D-) and $V_{pu(3.3)}$ high impedance; VP, VM driven HIGH; RCV driven LOW

[1] High impedance or driven LOW.

## 7.4 Power supply input options

The ISP1105/1106 range has two power supply input options.

**Internal regulator** —  $V_{CC(5.0)}$  is connected to 4.0 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). The  $V_{reg(3.3)}$  pin becomes a 3.3 V output reference.

**Regulator bypass** —  $V_{CC(5.0)}$  and  $V_{reg(3.3)}$  are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from the  $V_{reg(3.3)}$  power supply. The voltage range is 3.0 V to 3.6 V to comply with the USB specification.

The supply voltage range for each input option is specified in [Table 10](#).

**Table 10. Power supply input options**

Input option	$V_{CC(5.0)}$	$V_{reg(3.3)}$	$V_{CC(I/O)}$
Internal regulator	supply input for internal regulator (4.0 V to 5.5 V)	voltage reference output (3.3 V, 300 $\mu$ A)	supply input for digital I/O pins (1.65 V to 3.6 V)
Regulator bypass	connected to $V_{reg(3.3)}$ with maximum voltage drop of 0.3 V (2.7 V to 3.6 V)	supply input (3.0 V to 3.6 V)	supply input for digital I/O pins (1.65 V to 3.6 V)

## 8. Electrostatic discharge (ESD)

### 8.1 ESD protection

The pins that are connected to the USB connector (D+, D-,  $V_{CC(5.0)}$  and GND) have a minimum of  $\pm 12$  kV ESD protection. The  $\pm 12$  kV measurement is limited by the test equipment. Capacitors of  $4.7 \mu\text{F}$  connected from  $V_{\text{reg}(3.3)}$  to GND and  $V_{CC(5.0)}$  to GND are required to achieve this  $\pm 12$  kV ESD protection (see [Figure 6](#)).

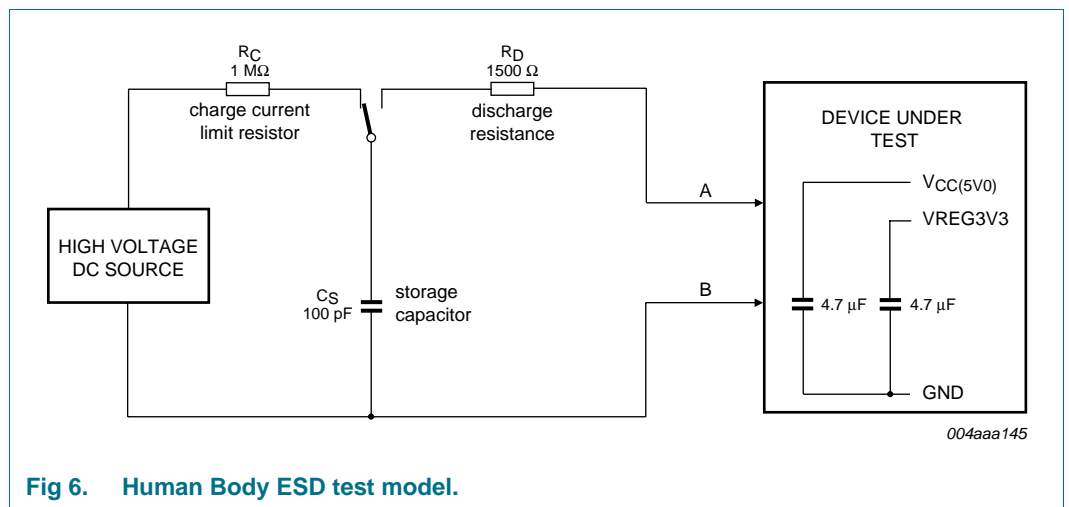


Fig 6. Human Body ESD test model.

### 8.2 ESD test conditions

A detailed report on test set-up and results is available on request.

## 9. Limiting values

**Table 11. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5.0)}$	supply voltage		-0.5	+6.0	V
$V_{CC(I/O)}$	I/O supply voltage		-0.5	+4.6	V
$V_{reg(3.3)}$	regulated supply voltage		-0.5	+4.6	V
$V_I$	DC input voltage		-0.5	$V_{CC(I/O)} + 0.5$	V
$I_{lu}$	latch-up current	$V_I = -1.8 \text{ V to } 5.4 \text{ V}$	-	100	mA
$V_{esd}$	electrostatic discharge voltage	$I_{LI} < 1 \mu\text{A}$	[1][2]		
		on pins D+, D-, $V_{CC(5.0)}$ and GND	-12000	+12000	V
		on other pins	-2000	+2000	V
$T_{stg}$	storage temperature		-40	+125	°C

[1] Testing equipment limits measurement to only  $\pm 12 \text{ kV}$ . Capacitors needed on  $V_{CC(5.0)}$  and  $V_{reg(3.3)}$ ; see [Section 8](#).

[2] Equivalent to discharging a 100 pF capacitor via a 1.5 k $\Omega$  resistor (Human Body Model).

## 10. Recommended operating conditions

**Table 12. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5.0)}$	supply voltage (internal regulator option)	5 V operation	4.0	5.0	5.5	V
$V_{reg(3.3)}$	supply voltage (regulator bypass option)	3.3 V operation	3.0	3.3	3.6	V
$V_{CC(I/O)}$	I/O supply voltage		1.65	-	3.6	V
$V_I$	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (D+/D-)		0	-	3.6	V
$T_{amb}$	operating ambient temperature		-40	-	+85	°C

## 11. Static characteristics

**Table 13. Static characteristics: supply pins**

$V_{CC} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{reg(3.3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 10](#) for valid voltage level combinations;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage output	internal regulator option; $I_{load} \leq 300\ \mu\text{A}$	[1][2] 3.0	3.3	3.6	V
$I_{CC}$	operating supply current	full-speed transmitting and receiving at 12 Mbit/s; $C_L = 50\text{ pF}$ on D+/D-	[3] -	4	8	mA
$I_{CC(I/O)}$	operating I/O supply current	full-speed transmitting and receiving at 12 Mbit/s	[3] -	1	2	mA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	full-speed idle: $V_{D+} > 2.7\text{ V}$ , $V_{D-} < 0.3\text{ V}$ ; SE0: $V_{D+} < 0.3\text{ V}$ , $V_{D-} < 0.3\text{ V}$	[4] -	-	500	$\mu\text{A}$
$I_{CC(I/O)(static)}$	static I/O supply current	full-speed idle, SE0 or suspend	-	-	20	$\mu\text{A}$
$I_{CC(susp)}$	suspend supply current	SUSPND = HIGH	[4] -	-	20	$\mu\text{A}$
$I_{CC(dis)}$	disable mode supply current	$V_{CC(I/O)}$ not connected	[4] -	-	20	$\mu\text{A}$
$I_{CC(I/O)(sharing)}$	sharing mode I/O supply current	$V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected	-	-	20	$\mu\text{A}$
$I_{Dx(sharing)}$	sharing mode load current on pins D+ and D-	$V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected; SOFTCON = LOW; $V_{Dx} = 3.6\text{ V}$	-	-	10	$\mu\text{A}$
$V_{reg(3.3)th}$	regulated supply voltage detection threshold	$1.65\text{ V} \leq V_{CC(I/O)} \leq V_{reg(3.3)}$ ; $2.7\text{ V} \leq V_{reg(3.3)} \leq 3.6\text{ V}$	-	-	0.8	V
		supply lost	-	-	-	V
		supply present	[5] 2.4	-	-	V
$V_{reg(3.3)hys}$	regulated supply voltage detection hysteresis	$V_{CC(I/O)} = 1.8\text{ V}$	-	0.45	-	V
$V_{CC(I/O)th}$	I/O supply voltage detection threshold	$V_{reg(3.3)} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.5	V
		supply lost	-	-	-	V
		supply present	1.4	-	-	V
$V_{CC(I/O)hys}$	I/O supply voltage detection hysteresis	$V_{reg(3.3)} = 3.3\text{ V}$	-	0.45	-	V

[1]  $I_{load}$  includes the pull-up resistor current via pin  $V_{pu(3.3)}$ .

[2] In 'suspend' mode, the minimum voltage is 2.7 V.

[3] Maximum value is characterized only, not tested in production.

[4] Excluding any load current and  $V_{pu(3.3)}/V_{sw}$  source current to the 1.5 k $\Omega$  and 15 k $\Omega$  pull-up and pull-down resistors (200  $\mu\text{A}$  typ.).

[5] When  $V_{CC(I/O)} < 2.7\text{ V}$ , the minimum value for  $V_{th(reg(3.3)(present))}$  is 2.0 V.

**Table 14. Static characteristics: digital pins**

$V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC(I/O)} = 1.65\text{ to }3.6\text{ V}</math></b>						
Input levels						
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
$V_{IH}$	HIGH-level input voltage		$0.6V_{CC(I/O)}$	-	-	V
Output levels						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.15	V
		$I_{OL} = 2\text{ mA}$	-	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 100\text{ }\mu\text{A}$	$V_{CC(I/O)} - 0.15$	-	-	V
		$I_{OH} = 2\text{ mA}$	$V_{CC(I/O)} - 0.4$	-	-	V
Leakage current						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
<b>Example 1: <math>V_{CC(I/O)} = 1.8\text{ V} \pm 0.15\text{ V}</math></b>						
Input levels						
$V_{IL}$	LOW-level input voltage		-	-	0.5	V
$V_{IH}$	HIGH-level input voltage		1.2	-	-	V
Output levels						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.15	V
		$I_{OL} = 2\text{ mA}$	-	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 100\text{ }\mu\text{A}$	1.5	-	-	V
		$I_{OH} = 2\text{ mA}$	1.25	-	-	V
<b>Example 2: <math>V_{CC(I/O)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>						
Input levels						
$V_{IL}$	LOW-level input voltage		-	-	0.7	V
$V_{IH}$	HIGH-level input voltage		1.7	-	-	V
Output levels						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.15	V
		$I_{OL} = 2\text{ mA}$	-	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 100\text{ }\mu\text{A}$	2.15	-	-	V
		$I_{OH} = 2\text{ mA}$	1.9	-	-	V
<b>Example 3: <math>V_{CC(I/O)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>						
Input levels						
$V_{IL}$	LOW-level input voltage		-	-	0.9	V
$V_{IH}$	HIGH-level input voltage		2.15	-	-	V
Output levels						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.15	V
		$I_{OL} = 2\text{ mA}$	-	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 100\text{ }\mu\text{A}$	2.85	-	-	V
		$I_{OH} = 2\text{ mA}$	2.6	-	-	V
<b>Capacitance</b>						
$C_{IN}$	input capacitance	pin to GND	-	-	10	pF

**Table 15. Static characteristics: analog I/O pins (D+, D-)**

$V_{CC} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{reg(3.3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input levels</b>						
<b>Differential receiver</b>						
$V_{DI}$	differential input sensitivity	$ V_{I(D+)} - V_{I(D-)} $	0.2	-	-	V
$V_{CM}$	differential common mode voltage	includes $V_{DI}$ range	0.8	-	2.5	V
<b>Single-ended receiver</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{hys}$	hysteresis voltage		0.4	-	0.7	V
<b>Output levels</b>						
$V_{OL}$	LOW-level output voltage	$R_L = 1.5\text{ k}\Omega$ to $+3.6\text{ V}$	-	-	0.3	V
$V_{OH}$	HIGH-level output voltage	$R_L = 15\text{ k}\Omega$ to GND	[1] 2.8	-	3.6	V
<b>Leakage current</b>						
$I_{LZ}$	OFF-state leakage current		-1	-	+1	$\mu\text{A}$
<b>Capacitance</b>						
$C_{IN}$	transceiver capacitance	pin to GND	-	-	20	pF
<b>Resistance</b>						
$Z_{DRV}$	driver output impedance	steady-state drive	[2] 34	39	44	$\Omega$
$Z_{INP}$	input impedance		10	-	-	$\text{M}\Omega$
$R_{SW}$	internal switch resistance at pin $V_{pu(3.3)}$		-	-	10	$\Omega$
<b>Termination</b>						
$V_{TERM}$	termination voltage for upstream port pull-up ( $R_{PU}$ )		[3][4] 3.0	-	3.6	V

[1]  $V_{OH(min)} = V_{reg(3.3)} - 0.2\text{ V}$ .

[2] Includes external resistors of  $33\ \Omega \pm 1\%$  on both D+ and D-.

[3] This voltage is available at pins  $V_{reg(3.3)}$  and  $V_{pu(3.3)}$ .

[4] In 'suspend' mode the minimum voltage is 2.7 V.

## 12. Dynamic characteristics

**Table 16. Dynamic characteristics: analog I/O pins (D+, D-)**

$V_{CC} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{reg(3.3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 10](#) for valid voltage level combinations;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Driver characteristics</b>						
<b>Full-speed mode</b>						
$t_{FR}$	rise time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 10 % to 90 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 7</a>	4	-	20	ns
$t_{FF}$	fall time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 90 % to 10 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 7</a>	4	-	20	ns
FRFM	differential rise/fall time matching ( $t_{FR}/t_{FF}$ )	excluding the first transition from idle state	90	-	111.1	%
$V_{CRS}$	output signal crossover voltage	excluding the first transition from idle state; see <a href="#">Figure 10</a>	<a href="#">2</a> 1.3	-	2.0	V
<b>Low-speed mode</b>						
$t_{LR}$	rise time	$C_L = 50\text{ pF to }600\text{ pF}$ ; 10 % to 90 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 7</a>	75	-	300	ns
$t_{LF}$	fall time	$C_L = 50\text{ pF to }600\text{ pF}$ ; 90 % to 10 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 7</a>	75	-	300	ns
LRFM	differential rise/fall time matching ( $t_{LR}/t_{LF}$ )	excluding the first transition from idle state	80	-	125	%
$V_{CRS}$	output signal crossover voltage	excluding the first transition from idle state; see <a href="#">Figure 10</a>	<a href="#">2</a> 1.3	-	2.0	V
<b>Driver timing</b>						
<b>Full-speed mode</b>						
$t_{PLH(drv)}$	driver propagation delay (VO/VPO, FSE0/VMO to D+,D-)	LOW-to-HIGH; see <a href="#">Figure 10</a>	-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (VO/VPO, FSE0/VMO to D+,D-)	HIGH-to-LOW; see <a href="#">Figure 10</a>	-	-	18	ns
$t_{PHZ}$	driver disable delay ( $\overline{OE}$ to D+,D-)	HIGH-to-OFF; see <a href="#">Figure 8</a>	-	-	15	ns
$t_{PLZ}$	driver disable delay ( $\overline{OE}$ to D+,D-)	LOW-to-OFF; see <a href="#">Figure 8</a>	-	-	15	ns
$t_{PZH}$	driver enable delay ( $\overline{OE}$ to D+,D-)	OFF-to-HIGH; see <a href="#">Figure 8</a>	-	-	15	ns
$t_{PZL}$	driver enable delay ( $\overline{OE}$ to D+,D-)	OFF-to-LOW; see <a href="#">Figure 8</a>	-	-	15	ns
<b>Low-speed mode</b>						

**Not specified:** low-speed delay timings are dominated by the slow rise/fall times  $t_{LR}$  and  $t_{LF}$ .



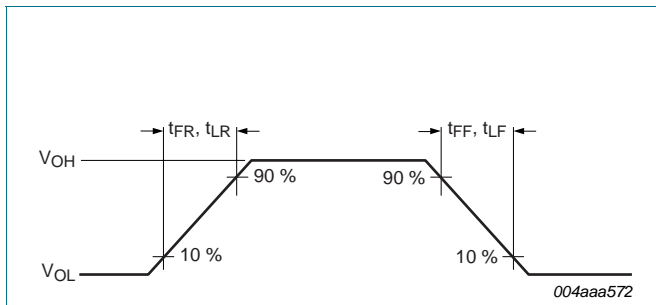
**Table 16. Dynamic characteristics: analog I/O pins (D+, D-) ...continued**

$V_{CC} = 4.0\text{ V to }5.5\text{ V}$  or  $V_{reg(3.3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$ ;  $V_{GND} = 0\text{ V}$ ; see [Table 10](#) for valid voltage level combinations;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.<sup>[1]</sup>

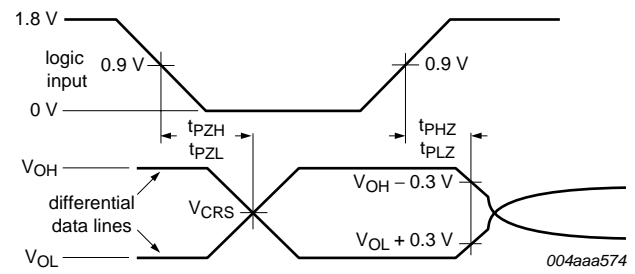
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Receiver timings (full-speed and low-speed mode)</b>						
<b>Differential receiver</b>						
$t_{PLH(rcv)}$	propagation delay (D+,D- to RCV)	LOW-to-HIGH; see <a href="#">Figure 9</a>	-	-	15	ns
$t_{PHL(rcv)}$	propagation delay (D+,D- to RCV)	HIGH-to-LOW; see <a href="#">Figure 9</a>	-	-	15	ns
<b>Single-ended receiver</b>						
$t_{PLH(se)}$	propagation delay (D+,D- to VP, VM)	LOW-to-HIGH; see <a href="#">Figure 9</a>	-	-	18	ns
$t_{PHL(se)}$	propagation delay (D+,D- to VP, VM)	HIGH-to-LOW; see <a href="#">Figure 9</a>	-	-	18	ns

[1] Test circuit: see [Figure 13](#).

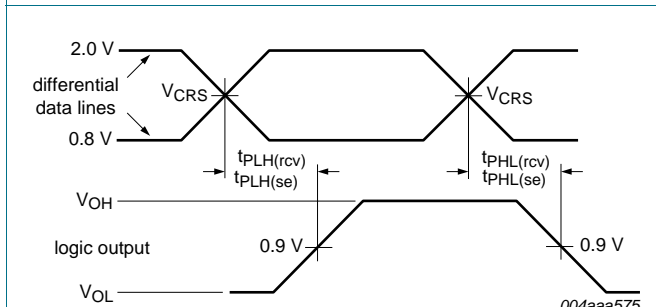
[2] Characterized only, not tested. Limits guaranteed by design.



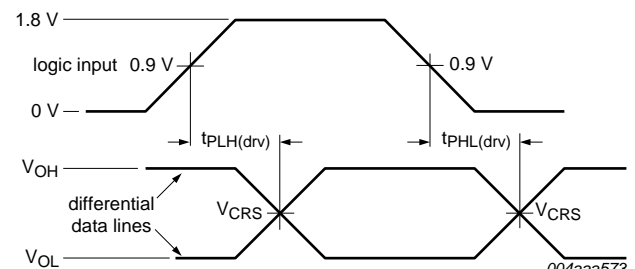
**Fig 7. Rise and fall times.**



**Fig 8. Timing of  $\overline{OE}$  to D+, D-.**

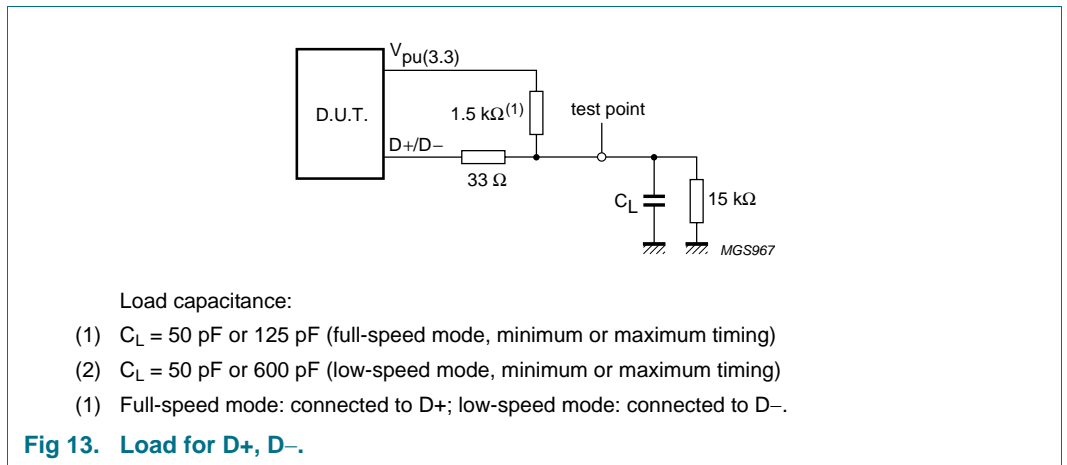
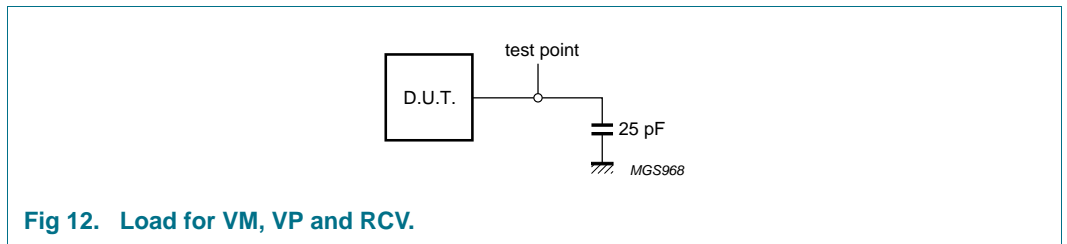
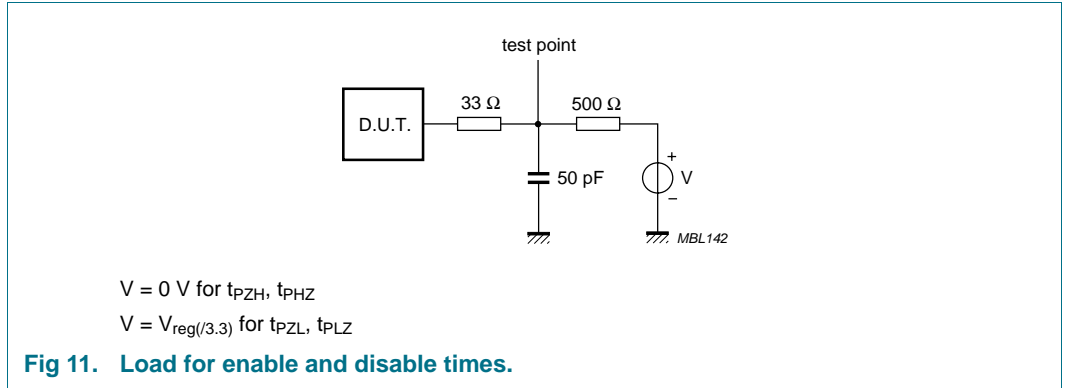


**Fig 9. Timing of D+, D- to RCV, VP, VM.**



**Fig 10. Timing of VO/PO, FSE0/VMO to D+, D-.**

13. Test information



14. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm

SOT639-2

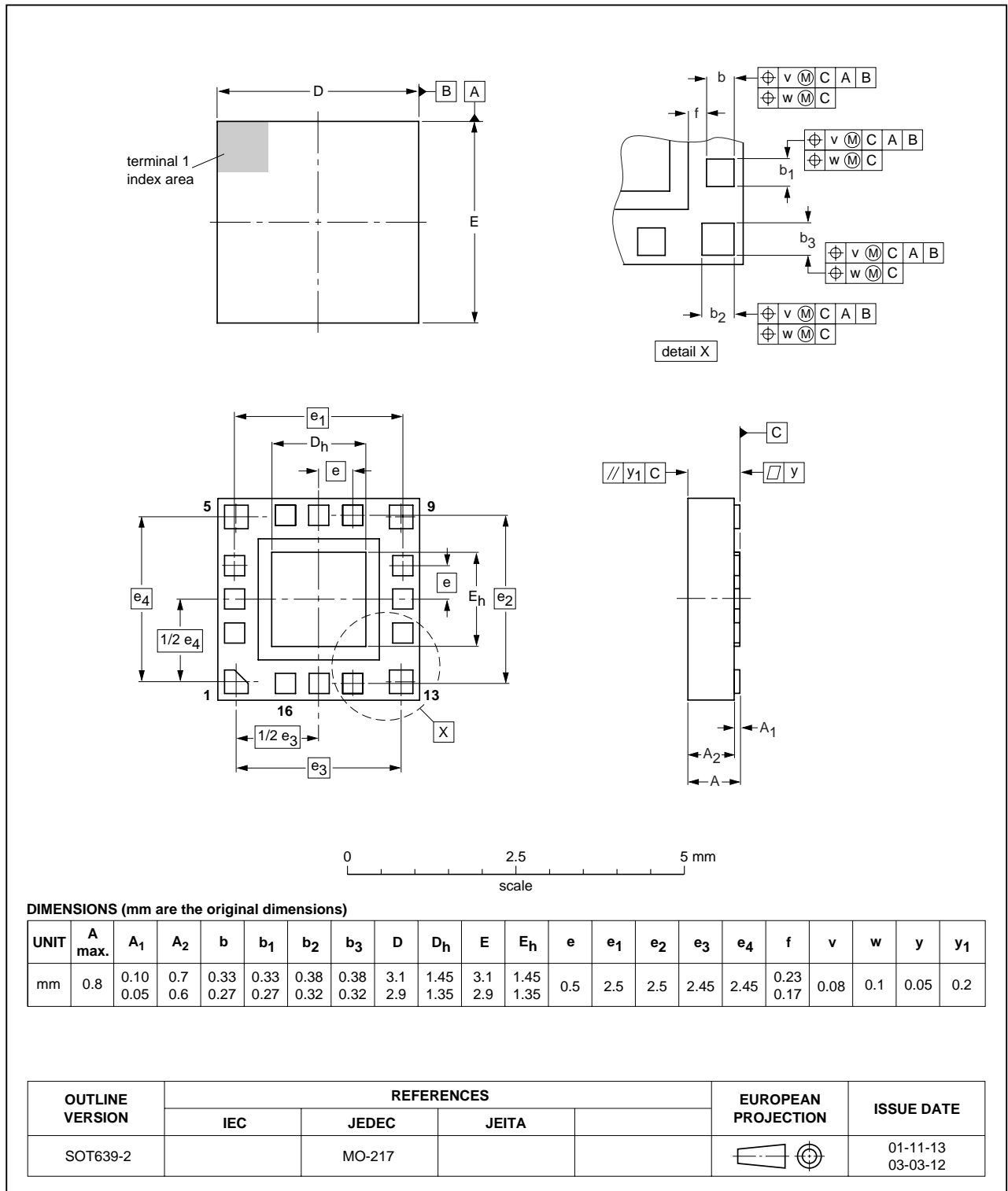


Fig 14. HBCC16 package outline.

**HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm**

**SOT758-1**

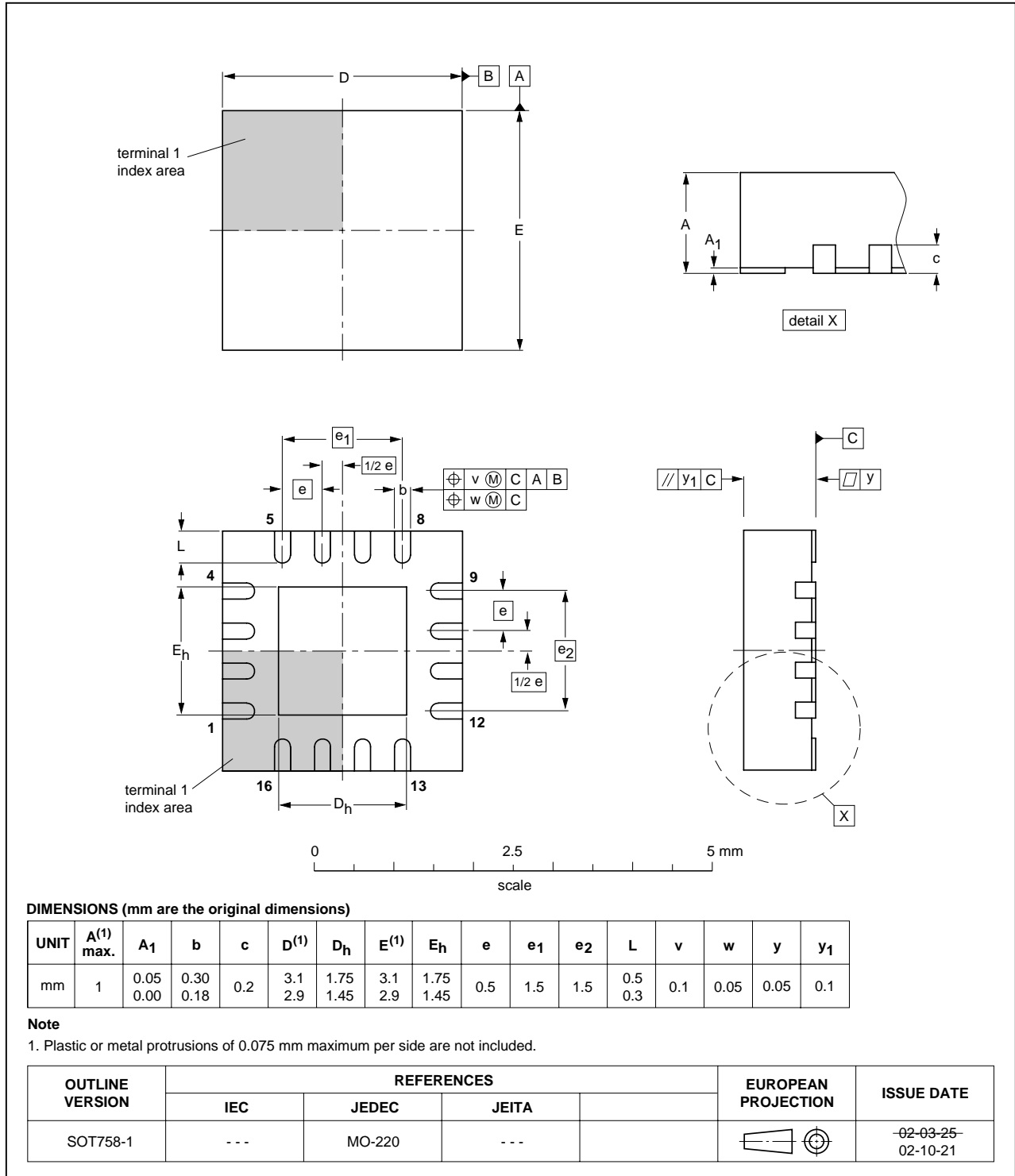


Fig 15. HVQFN16 package outline.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

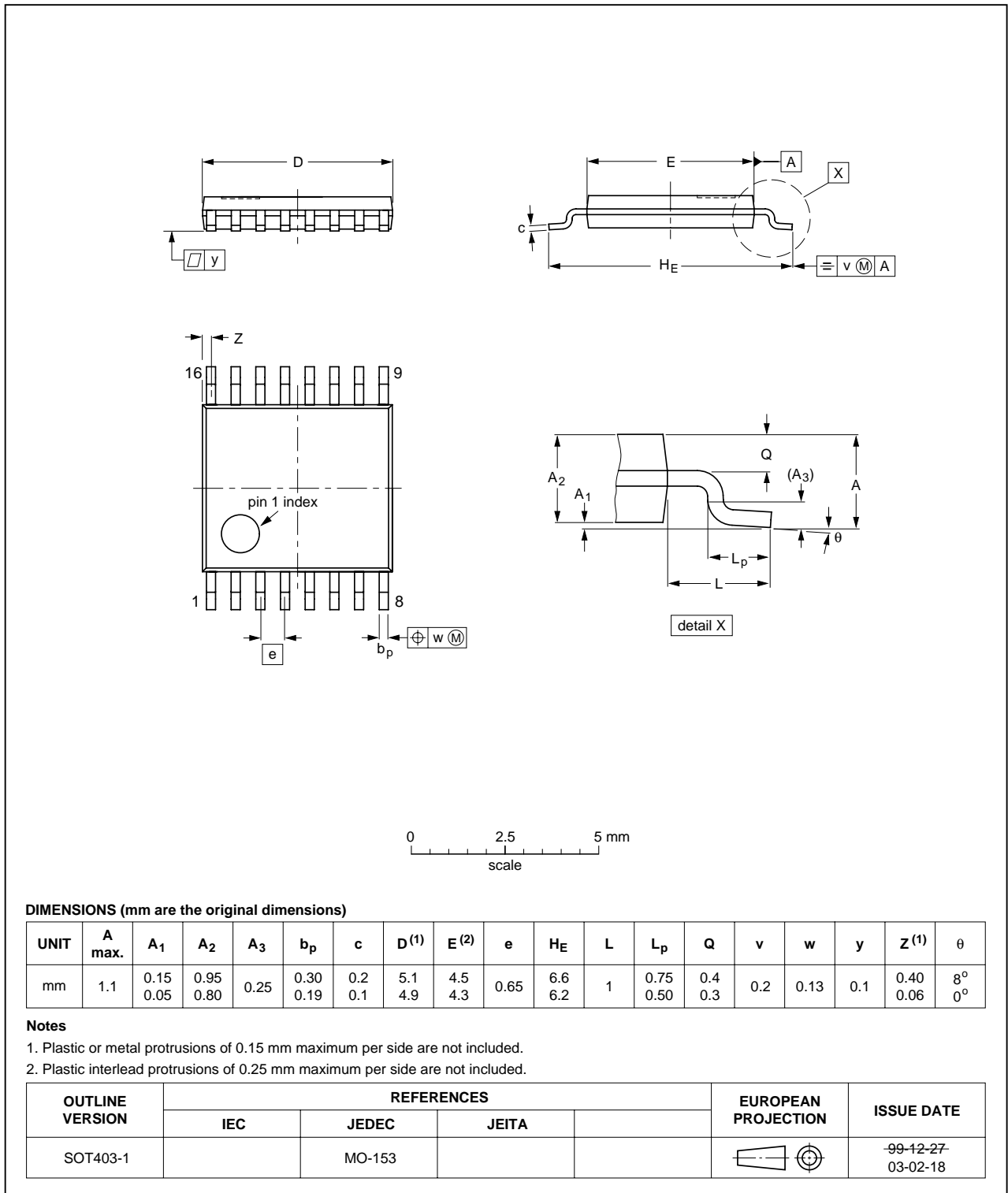


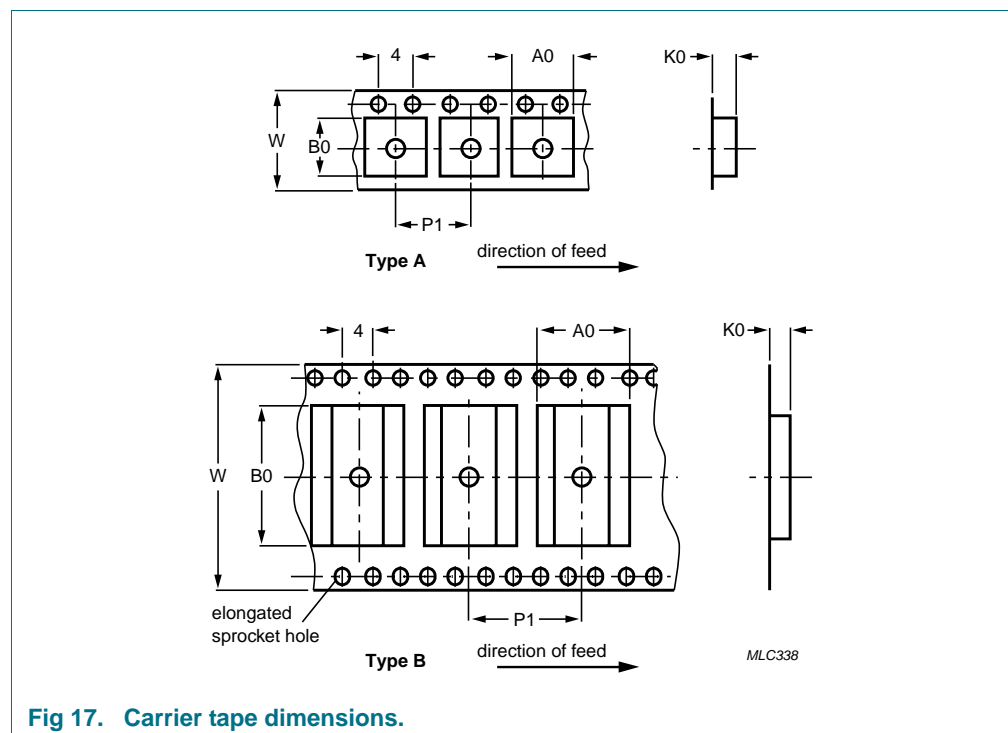
Fig 16. TSSOP16 package outline.

## 15. Packing information

The ISP1105/1106W (HBCC16 package) is delivered on a type A carrier tape, see [Figure 17](#). The tape dimensions are given in [Table 17](#).

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is  $\pm 0.02$  mm. The camber must not exceed 1 mm in 100 mm.



**Fig 17. Carrier tape dimensions.**

**Table 17. Type A carrier tape dimensions for ISP1105/1106W**

Dimension	Value	Unit
A <sub>0</sub>	3.3	mm
B <sub>0</sub>	3.3	mm
K <sub>0</sub>	1.1	mm
P <sub>1</sub>	8.0	mm
W	12.0 ± 0.3	mm

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 18](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

**Table 18. SnPb eutectic process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

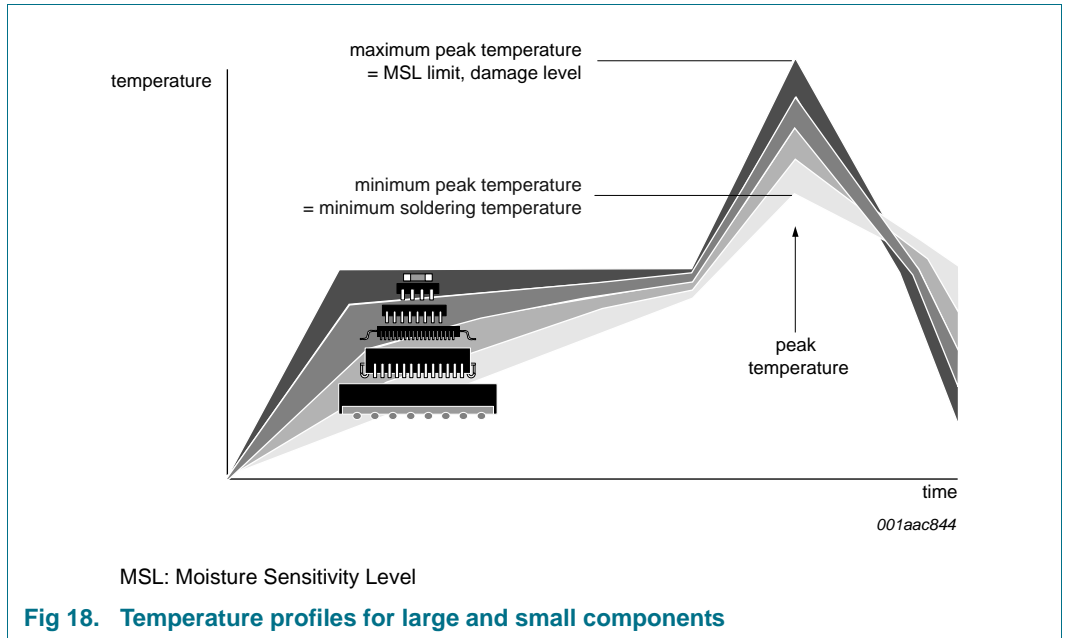
**Table 19. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 18](#).



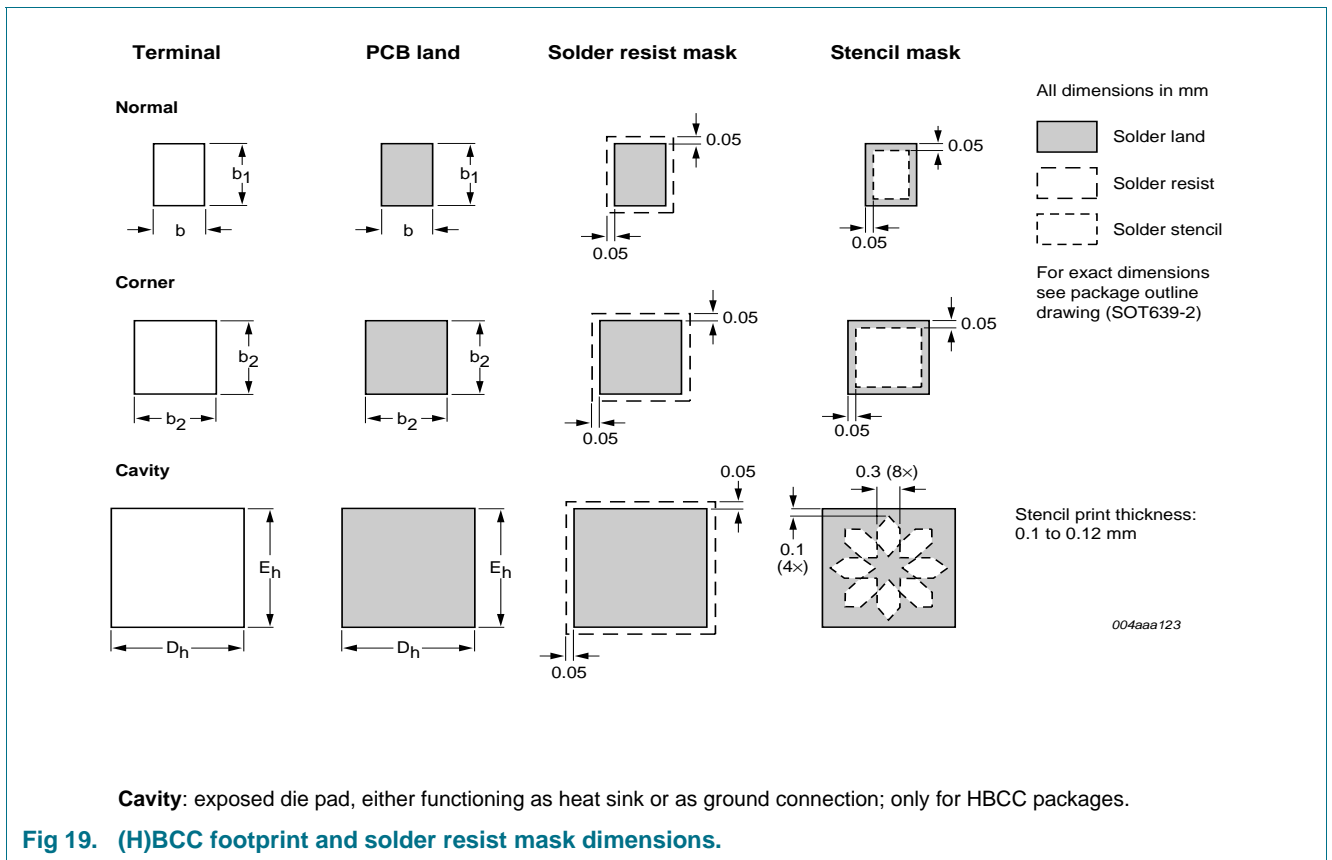


For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

## 17. Additional soldering information

### 17.1 (H)BCC packages: footprint

The surface material of the terminals on the resin protrusion consists of a 4-layer metal structure (Au, Pd, Ni and Pd). The Au + Pd layer (0.1 μm min.) ensures solderability, the Ni layer (5 μm min.) prevents diffusion, and the Pd layer on top (0.5 μm min.) ensures effective wire bonding.



### 17.2 (H)BCC packages: reflow soldering profile

The conditions for reflow soldering of (H)BCC packages are as follows:

- **Preheating time:** minimum 90 s at  $T = 145$  to  $155$  °C
- **Soldering time:** minimum 90 s (BCC) or minimum 100 s (HBCC) at  $T > 183$  °C
- **Peak temperature:**
  - Ambient temperature:  $T_{amb(max)} = 260$  °C
  - Device surface temperature:  $T_{case(max)} = 255$  °C.

## 18. Revision history

**Table 20. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1105_1106_9	20090119	Product data sheet	-	ISP1105_1106-08
Modifications:		<ul style="list-style-type: none"> <li>Globally changed Philips Semiconductors and Philips to ST-NXP Wireless. Also updated the legal text.</li> <li><a href="#">Section 8.1 "ESD protection"</a>: removed the second paragraph.</li> </ul>		
ISP1105_1106-08 (9397 750 09529)	20040219	Product data		ISP1105_1106_1107-07
ISP1105_1106_1107-07 (9397 750 08872)	20020329	Product data		ISP1105_1106_1107-06
ISP1105_1106_1107-06 (9397 750 08681)	20011130	Product data		ISP1105_1106_1107-05
ISP1105_1106_1107-05 (9397 750 08643)	20010903	Product data		ISP1105_1106_1107-04
ISP1105_1106_1107-04 (9397 750 08515)	20010802	Preliminary data		ISP1105_1106_1107-03
ISP1105_1106_1107-03 (9397 750 07879)	20010704	Preliminary data	-	ISP1107-02
ISP1107-02 (9397 750 06899)	20010205	Objective specification; ISP1107 stand-alone data sheet only	-	ISP1107-01
ISP1107-01 (9397 750 08643)	20000223	Objective specification; ISP1107 stand-alone data sheet only	--	-

## 19. Tables

Table 1.	Ordering information	2
Table 2.	Selection guide	2
Table 3.	Pin description	5
Table 4.	Function table	7
Table 5.	Driving function (pin $\overline{OE} = L$ ) using single-ended input data interface for ISP1105 (pin MODE = L)	7
Table 6.	Driving function (pin $\overline{OE} = L$ ) using differential input data interface for ISP1105 (pin MODE = H) and ISP1106	7
Table 7.	Receiving function (pin $\overline{OE} = H$ )	7
Table 8.	Pin states in disable or sharing mode	8
Table 9.	Power supply configuration overview	8
Table 10.	Power supply input options	9
Table 11.	Limiting values	11
Table 12.	Recommended operating conditions	11
Table 13.	Static characteristics: supply pins	12
Table 14.	Static characteristics: digital pins	13
Table 15.	Static characteristics: analog I/O pins (D+, D-)	14
Table 16.	Dynamic characteristics: analog I/O pins (D+, D-)	15
Table 17.	Type A carrier tape dimensions for ISP1105/1106W	21
Table 18.	SnPb eutectic process (from J-STD-020C)	23
Table 19.	Lead-free process (from J-STD-020C)	23
Table 20.	Revision history	26

## 20. Figures

Fig 1.	Block diagram (combined ISP1105 and ISP1106).	3
Fig 2.	Pin configuration ISP1105BS (HVQFN).	4
Fig 3.	Pin configuration ISP1105W (HBCC16).	4
Fig 4.	Pin configuration ISP1106DH (TSSOP16).	4
Fig 5.	Pin configuration ISP1106W (HBCC16).	4
Fig 6.	Human Body ESD test model.	10
Fig 7.	Rise and fall times.	16
Fig 8.	Timing of $\overline{OE}$ to D+, D-.	16
Fig 9.	Timing of D+, D- to RCV, VP, VM.	16
Fig 10.	Timing of VO/VPO, FSE0/VMO to D+, D-.	16
Fig 11.	Load for enable and disable times.	17
Fig 12.	Load for VM, VP and RCV.	17
Fig 13.	Load for D+, D-.	17
Fig 14.	HBCC16 package outline.	18
Fig 15.	HVQFN16 package outline.	19
Fig 16.	TSSOP16 package outline.	20
Fig 17.	Carrier tape dimensions.	21
Fig 18.	Temperature profiles for large and small components.	24
Fig 19.	(H)BCC footprint and solder resist mask dimensions.	25

## 21. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>
<b>2</b>	<b>Features</b> . . . . .	<b>1</b>
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>
4.1	Ordering options . . . . .	2
<b>5</b>	<b>Block diagram</b> . . . . .	<b>3</b>
<b>6</b>	<b>Pinning information</b> . . . . .	<b>4</b>
6.1	Pinning . . . . .	4
6.2	Pin description . . . . .	5
<b>7</b>	<b>Functional description</b> . . . . .	<b>7</b>
7.1	Function selection . . . . .	7
7.2	Operating functions . . . . .	7
7.3	Power supply configurations . . . . .	8
7.4	Power supply input options . . . . .	9
<b>8</b>	<b>Electrostatic discharge (ESD)</b> . . . . .	<b>10</b>
8.1	ESD protection . . . . .	10
8.2	ESD test conditions . . . . .	10
<b>9</b>	<b>Limiting values</b> . . . . .	<b>11</b>
<b>10</b>	<b>Recommended operating conditions</b> . . . . .	<b>11</b>
<b>11</b>	<b>Static characteristics</b> . . . . .	<b>12</b>
<b>12</b>	<b>Dynamic characteristics</b> . . . . .	<b>15</b>
<b>13</b>	<b>Test information</b> . . . . .	<b>17</b>
<b>14</b>	<b>Package outline</b> . . . . .	<b>18</b>
<b>15</b>	<b>Packing information</b> . . . . .	<b>21</b>
<b>16</b>	<b>Soldering of SMD packages</b> . . . . .	<b>22</b>
16.1	Introduction to soldering . . . . .	22
16.2	Wave and reflow soldering . . . . .	22
16.3	Wave soldering . . . . .	22
16.4	Reflow soldering . . . . .	23
<b>17</b>	<b>Additional soldering information</b> . . . . .	<b>25</b>
17.1	(H)BCC packages: footprint . . . . .	25
17.2	(H)BCC packages: reflow soldering profile . . . . .	25
<b>18</b>	<b>Revision history</b> . . . . .	<b>26</b>
<b>19</b>	<b>Tables</b> . . . . .	<b>27</b>
<b>20</b>	<b>Figures</b> . . . . .	<b>28</b>
<b>21</b>	<b>Contents</b> . . . . .	<b>29</b>

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