

DATA SHEET

TEA1110A

Low voltage versatile telephone
transmission circuit with dialler
interface

Product specification
Supersedes data of 1997 Apr 22
File under Integrated Circuits, IC03

2000 Feb 15

Low voltage versatile telephone transmission circuit with dialler interface

TEA1110A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding voltage drop over external polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 k Ω) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 k Ω) for electret microphones
- DTMF input with confidence tone
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- AGC line loss compensation for microphone and earpiece amplifiers.

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines, answering machines.

GENERAL DESCRIPTION

The TEA1110A is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

$I_{\text{line}} = 15 \text{ mA}$; $V_{\text{EE}} = 0 \text{ V}$; $R_{\text{SLPE}} = 20 \text{ }\Omega$; AGC pin connected to V_{EE} ; $Z_{\text{line}} = 600 \text{ }\Omega$; $f = 1 \text{ kHz}$;
 $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ for TEA1110A(T); $T_{\text{j}} = 25 \text{ }^\circ\text{C}$ for TEA1110AUH; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	$V_{\text{CC}} = 2.9 \text{ V}$	–	1.1	1.4	mA
V_{CC}	supply voltage for peripherals	$I_{\text{P}} = 0 \text{ mA}$	–	2.9	–	V
G_{vtrx}	typical voltage gain					
	microphone amplifier (not adjustable)	$V_{\text{MIC}} = 4 \text{ mV (RMS)}$	–	43.7	–	dB
ΔG_{vtrx}	receiving amplifier range	$V_{\text{IR}} = 4 \text{ mV (RMS)}$	19	–	33	dB
	gain control range for microphone and receiving amplifiers with respect to $I_{\text{line}} = 15 \text{ mA}$	$I_{\text{line}} = 85 \text{ mA}$	–	5.9	–	dB
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	$\overline{\text{MUTE}} = \text{LOW}$	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1110A	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
TEA1110AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1110AUH	–	bare die; on foil	–

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BLOCK DIAGRAM

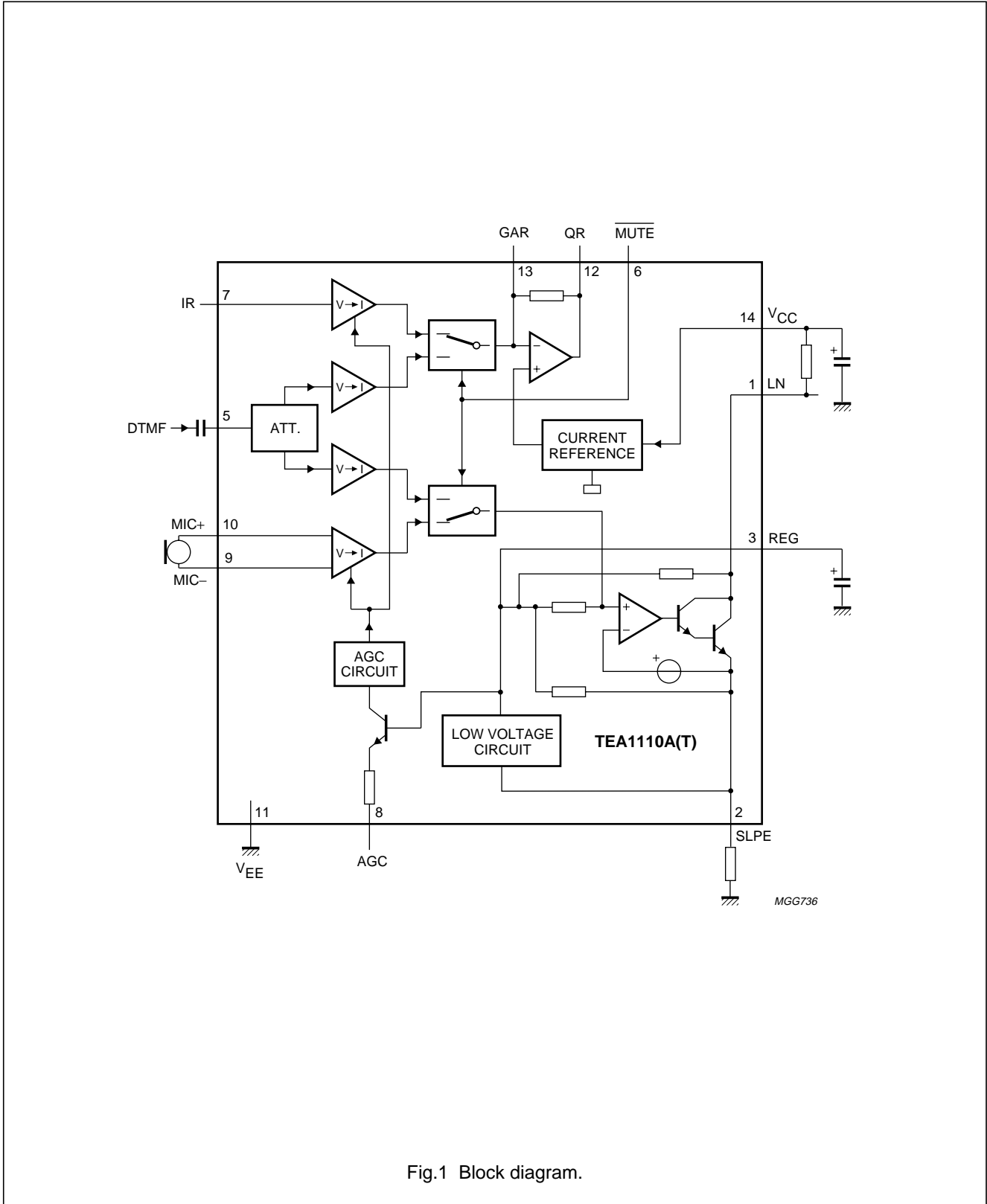


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	PAD	DESCRIPTION
	TEA1110A(T)	TEA1110AUH	
LN	1	1	positive line terminal
SLPE	2	2	slope (DC resistance) adjustment
REG	3	3	line voltage regulator decoupling
n.c.	4	4	not connected
DTMF	5	5	dual-tone multi-frequency input
$\overline{\text{MUTE}}$	6	6	mute input to select speech or dialling mode (active LOW)
IR	7	7	receiving amplifier input
AGC	8	8	automatic gain control/ line loss compensation
MIC-	9	9	inverting microphone amplifier input
MIC+	10	10	non-inverting microphone amplifier input
V_{EE}	11	11	negative line terminal
QR	12	12	earpiece amplifier output
GAR	13	13	earpiece amplifier gain adjustment
V_{CC}	14	14	supply voltage for internal circuit

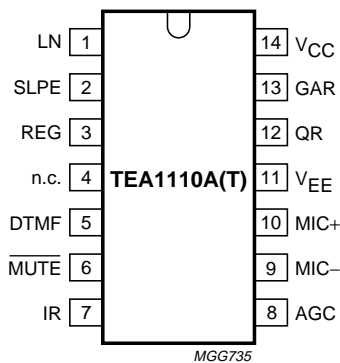


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1110A and its peripherals is obtained from the telephone line; see Fig.3.

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. V_{ref} is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). V_{ref} equals 3.35 V and can be increased by connecting R_{VA} between pins REG and SLPE (see Fig.4), or decreased by connecting R_{VA} between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate V_{ref} and is decoupled by C_{REG} , which is connected to V_{EE} . This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current.

The voltage at pin LN is:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I^*$$

Where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_P = supply current for peripheral circuits

I^* = current consumed between LN and V_{EE} .

The preferred value for R_{SLPE} is 20 Ω . Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the gain control characteristics, the sidetone level and the maximum output swing on the line.

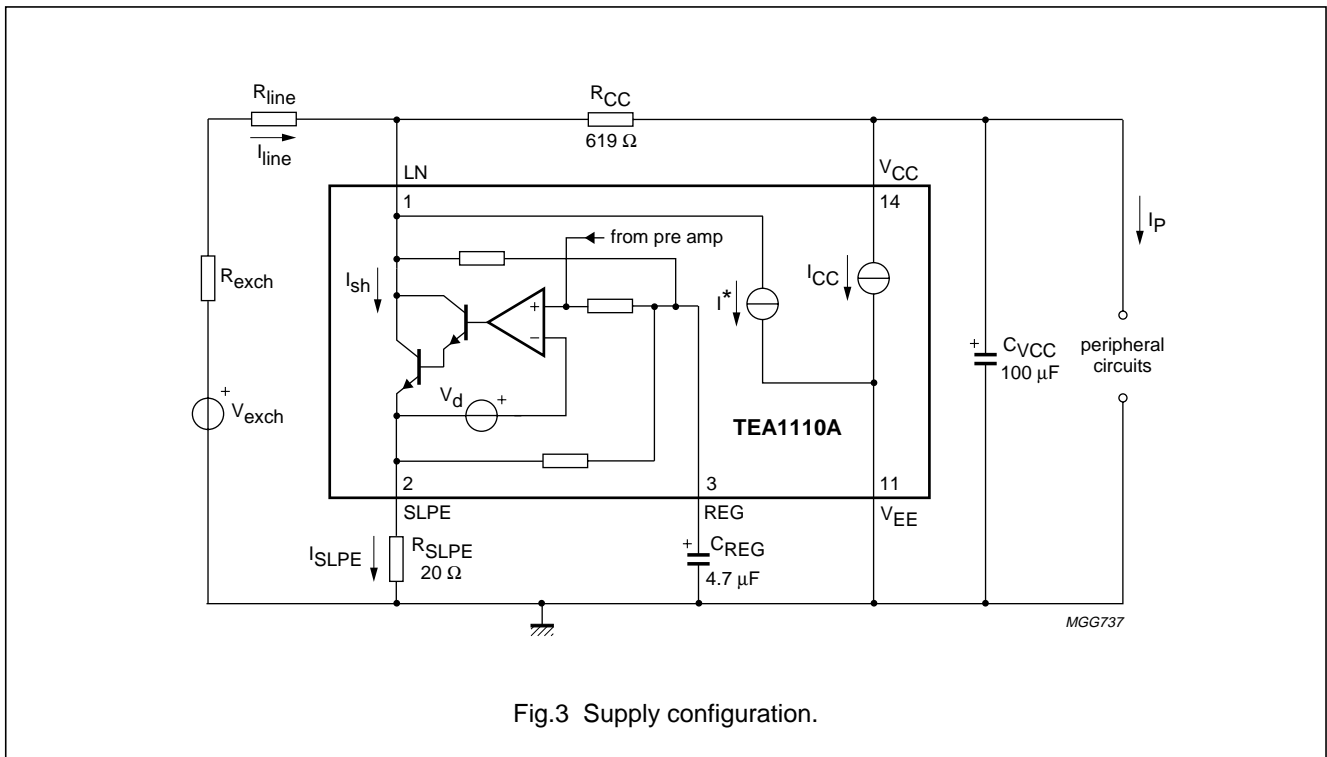


Fig.3 Supply configuration.

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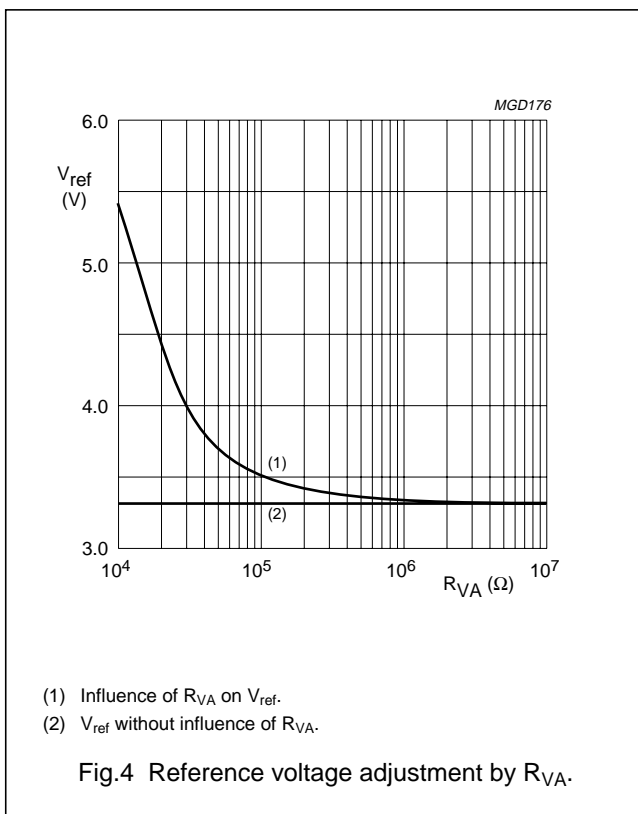
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The internal circuitry of the TEA1110A is supplied from pin V_{CC} . This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC} . It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula: $V_{CC} = V_{CC0} - R_{CCint} \times (I_P - I_{rec})$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC} \text{ (see also Figs 5 and 6).}$$

R_{CCint} is the internal equivalent resistance of the voltage supply, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.



Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuit is illustrated in Fig.7.

Microphone amplifier (pins MIC+ and MIC-)

The TEA1110A has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC- is 64 k Ω (2×32 k Ω). The voltage gain from pins MIC+/MIC- to pin LN is set at 43.7 dB (typ).

Automatic gain control is provided on this amplifier for line loss compensation.

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 k Ω . The voltage gain from pin IR to pin QR is set at 33 dB (typ). The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 14 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 125 k Ω . The condition $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_P current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1110A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω /km and an average attenuation of 1.2 dB/km). The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE} .

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This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin MUTE)

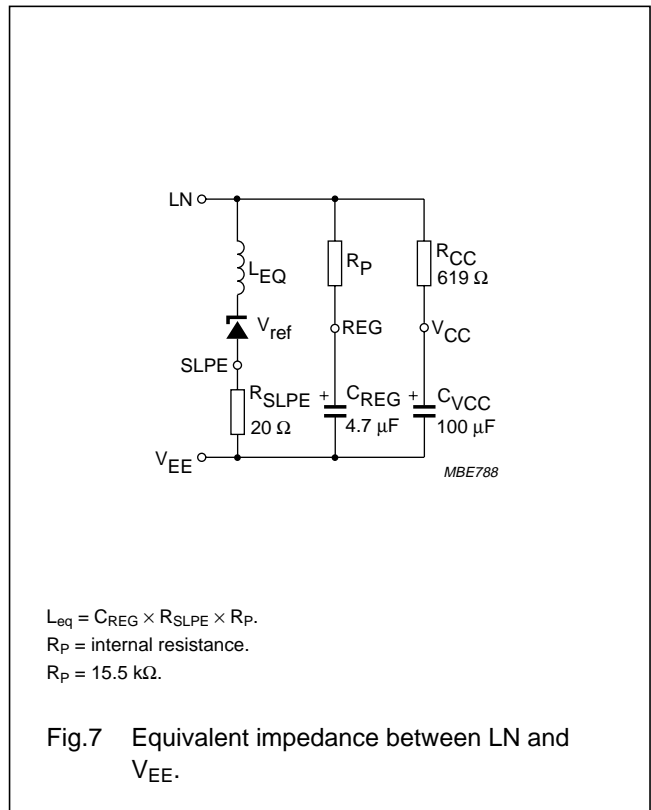
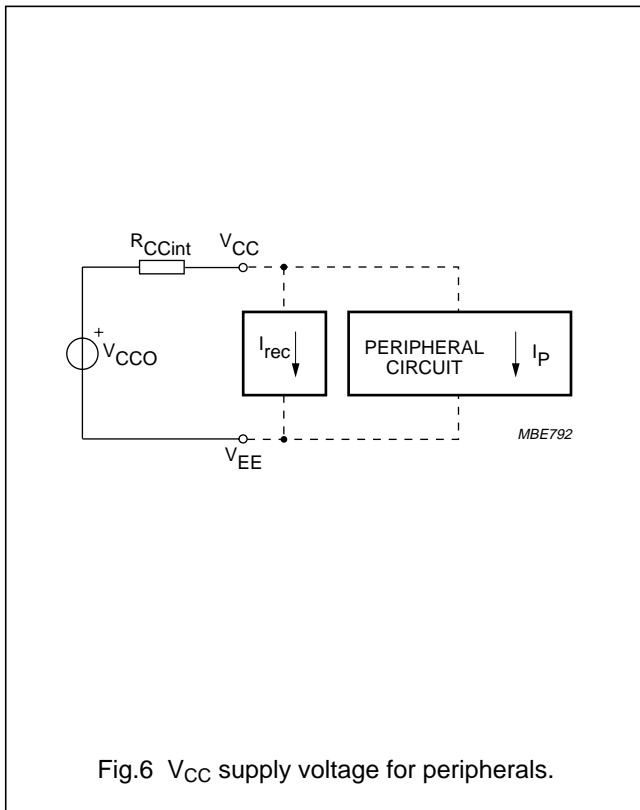
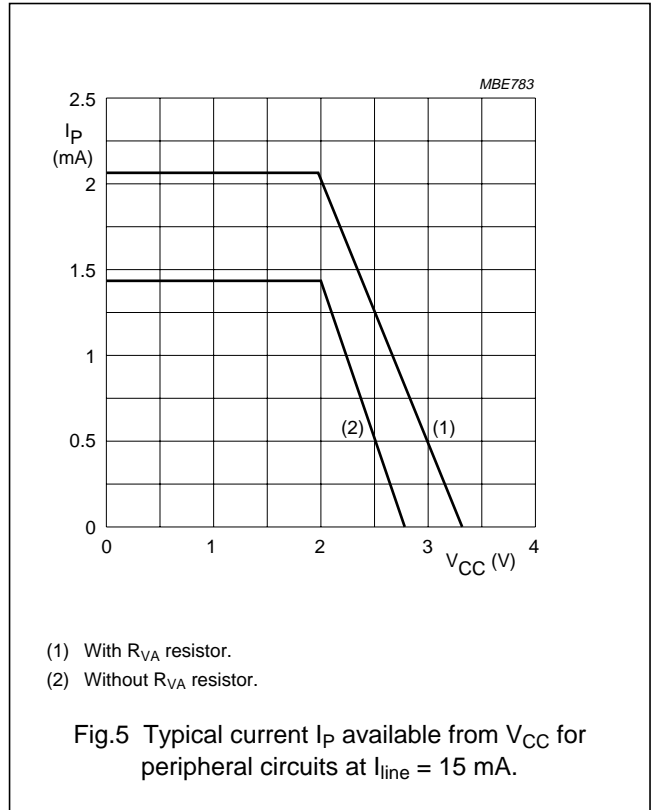
The mute function performs the switching between the speech mode and the dialling mode. When MUTE is LOW, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When MUTE is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled. A pull-up resistor is included at the input.

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1110A has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.3 dB.

The automatic gain control has no effect on the DTMF amplifier.



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SIDETONE SUPPRESSION

The TEA1110A anti-sidetone network comprising R_{CC}/Z_{line} , R_{ast1} , R_{ast2} , R_{ast3} , R_{SLPE} and Z_{bal} (see Fig.8) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal} .

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value of Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1110A (as shown in Fig.13) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.9) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication "Applications Handbook for Wired Telecom Systems, IC03b", order number 9397 750 00811.

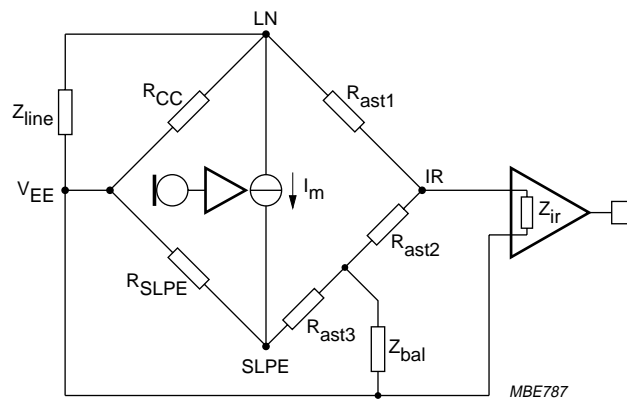


Fig.8 Equivalent circuit of TEA1110A family anti-sidetone bridge.

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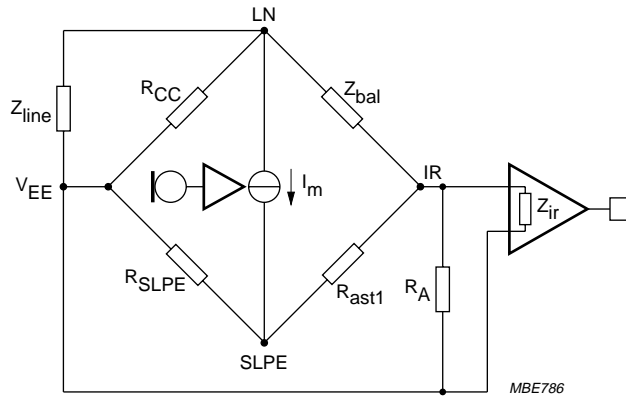


Fig.9 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{LN}	positive continuous line voltage		V _{EE} - 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V _{EE} - 0.4	13.2	V
V _{n(max)}	maximum voltage on all pins		V _{EE} - 0.4	V _{CC} + 0.4	V
I _{line}	line current	R _{SLPE} = 20 Ω; see Figs 10 and 11	-	140	mA
P _{tot}	total power dissipation	T _{amb} = 75 °C; see Figs 10 and 11			
	TEA1110A		-	588	mW
	TEA1110AT		-	384	mW
	TEA1110AUH; note 1		-	-	mW
T _{stg}	storage temperature		-40	+125	°C
T _{amb}	operating ambient temperature		-25	+75	°C
T _j	junction temperature		-	+125	°C

Note

1. Mostly dependent on the maximum required ambient temperature, on the voltage between LN and SLPE and on the thermal resistance between die ambient temperature. This thermal resistance depends on the application board layout and on the materials used. Figure 12 shows the safe operating area versus this thermal resistance for ambient temperature T_{amb} = 75 °C

HANDLING

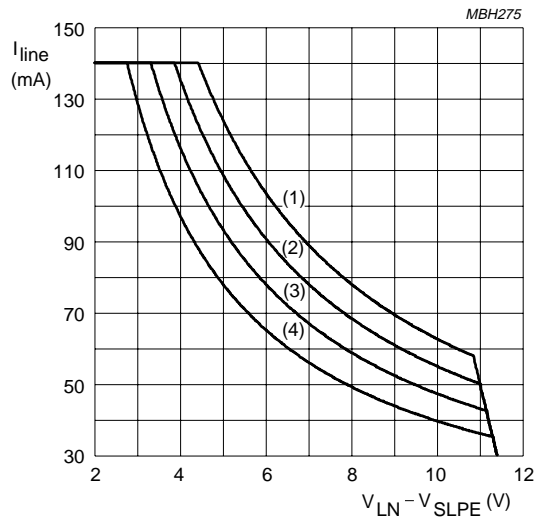
This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with "MIL STD 883C - method 3015".

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient; mounted on epoxy board 40.1 × 19.1 × 1.5 mm	in free air		
	TEA1110A		85	K/W
	TEA1110AT		130	K/W
	TEA1110AUH		tbf by customer in application	K/W

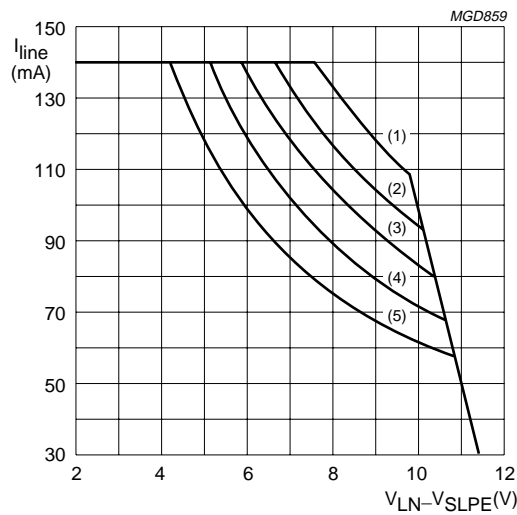
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- (1) $T_{amb} = 45\text{ }^{\circ}\text{C}$; $P_{tot} = 0.615\text{ W}$.
- (2) $T_{amb} = 55\text{ }^{\circ}\text{C}$; $P_{tot} = 0.538\text{ W}$.
- (3) $T_{amb} = 65\text{ }^{\circ}\text{C}$; $P_{tot} = 0.461\text{ W}$.
- (4) $T_{amb} = 75\text{ }^{\circ}\text{C}$; $P_{tot} = 0.384\text{ W}$.

Fig.10 SO14 Safe operating area (TEA1110AT).

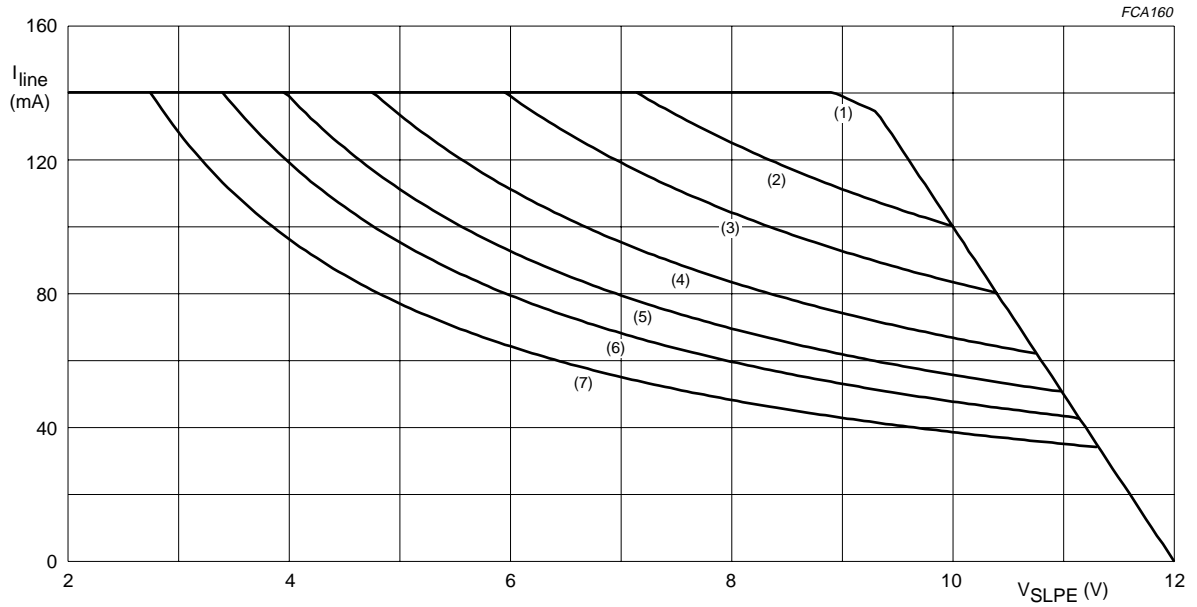


- (1) $T_{amb} = 35\text{ }^{\circ}\text{C}$; $P_{tot} = 1.058\text{ W}$.
- (2) $T_{amb} = 45\text{ }^{\circ}\text{C}$; $P_{tot} = 0.941\text{ W}$.
- (3) $T_{amb} = 55\text{ }^{\circ}\text{C}$; $P_{tot} = 0.823\text{ W}$.
- (4) $T_{amb} = 65\text{ }^{\circ}\text{C}$; $P_{tot} = 0.705\text{ W}$.
- (5) $T_{amb} = 75\text{ }^{\circ}\text{C}$; $P_{tot} = 0.588\text{ W}$.

Fig.11 DIP14 Safe operating area (TEA1110A).

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LINE	R _{th(j-a)} (K/W)
(1)	40
(2)	50
(3)	60
(4)	75
(5)	90
(6)	105
(7)	130

Fig.12 Safe operating area at T_{amb} = 75 °C (TEA1110AUH).

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CHARACTERISTICS

$I_{line} = 15 \text{ mA}$; $V_{EE} = 0 \text{ V}$; $R_{SLPE} = 20 \text{ }\Omega$; AGC pin connected to V_{EE} ; $Z_{line} = 600 \text{ }\Omega$; $f = 1 \text{ kHz}$;
 $T_{amb} = 25 \text{ }^\circ\text{C}$ for TEA1110A(T); $T_j = 25 \text{ }^\circ\text{C}$ for TEA1110AUH; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	$I_{line} = 1 \text{ mA}$	–	1.6	–	V
		$I_{line} = 4 \text{ mA}$	–	2.3	–	V
		$I_{line} = 15 \text{ mA}$	3.35	3.65	3.95	V
		$I_{line} = 140 \text{ mA}$	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)} = 27 \text{ k}\Omega$	–	4.4	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to $25 \text{ }^\circ\text{C}$	$T_{amb} = -25 \text{ to } +75 \text{ }^\circ\text{C}$	–	± 30	–	mV
I_{CC}	internal current consumption	$V_{CC} = 2.9 \text{ V}$	–	1.1	1.4	mA
V_{CC}	supply voltage for peripherals	$I_P = 0 \text{ mA}$	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	$I_P = 0.5 \text{ mA}$	–	550	620	Ω
Microphone amplifier (pins MIC+ and MIC–)						
$ Z_i $	input impedance differential between pins MIC+ and MIC– single-ended between pins MIC+/MIC– and V_{EE}		–	64	–	k Ω
			–	32	–	k Ω
G_{vtx}	voltage gain from MIC+/MIC– to LN	$V_{MIC} = 4 \text{ mV (RMS)}$	42.7	43.7	44.7	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	$f = 300 \text{ to } 3400 \text{ Hz}$	–	± 0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to $25 \text{ }^\circ\text{C}$	$T_{amb} = -25 \text{ to } +75 \text{ }^\circ\text{C}$	–	± 0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	$I_{line} = 15 \text{ mA}$; THD = 2%	1.4	1.7	–	V
		$I_{line} = 4 \text{ mA}$, THD = 10%	–	0.8	–	V
V_{notx}	noise output voltage at pin LN; pins MIC+/MIC– shorted through $200 \text{ }\Omega$	psophometrically weighted (P53 curve)	–	–78.5	–	dBmp
Receiving amplifier (pins IR, QR and GAR)						
$ Z_i $	input impedance		–	20	–	k Ω
G_{vrx}	voltage gain from IR to QR	$V_{IR} = 4 \text{ mV (RMS)}$	32	33	34	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referred to 1 kHz	$f = 300 \text{ to } 3400 \text{ Hz}$	–	± 0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referred to $25 \text{ }^\circ\text{C}$	$T_{amb} = -25 \text{ to } +75 \text{ }^\circ\text{C}$	–	± 0.3	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	14	dB
$V_{o(rms)}$	maximum receiving signal (RMS value)	$I_P = 0$ mA sine wave drive; $R_L = 150 \Omega$; THD = 2%	–	0.25	–	V
		$I_P = 0$ mA sine wave drive; $R_L = 450 \Omega$; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	$G_{vrx} = 33$ dB; IR open-circuit; $R_L = 150 \Omega$; psophometrically weighted (P53 curve)	–	–87	–	dBVp
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to $I_{line} = 15$ mA	$I_{line} = 85$ mA	–	5.9	–	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for minimum gain		–	56	–	mA
DTMF amplifier (pin DTMF)						
$ Z_i $	input impedance		–	20	–	k Ω
G_{vdtmf}	voltage gain from DTMF to LN	$V_{DTMF} = 20$ mV (RMS); MUTE = LOW	24.1	25.3	26.5	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referred to 1 kHz	$f = 300$ to 3400 Hz	–	± 0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referred to 25 °C	$T_{amb} = -25$ to +75 °C	–	± 0.4	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	$V_{DTMF} = 20$ mV (RMS); $R_L = 150 \Omega$	–	–15	–	dB
Mute function (pin MUTE)						
V_{IL}	LOW level input voltage		$V_{EE} - 0.4$	–	$V_{EE} + 0.3$	V
V_{IH}	HIGH level input voltage		$V_{EE} + 1.5$	–	$V_{CC} + 0.4$	V
I_{MUTE}	input current		–	1.5	–	μ A
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	MUTE = LOW	–	80	–	dB

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APPLICATION INFORMATION

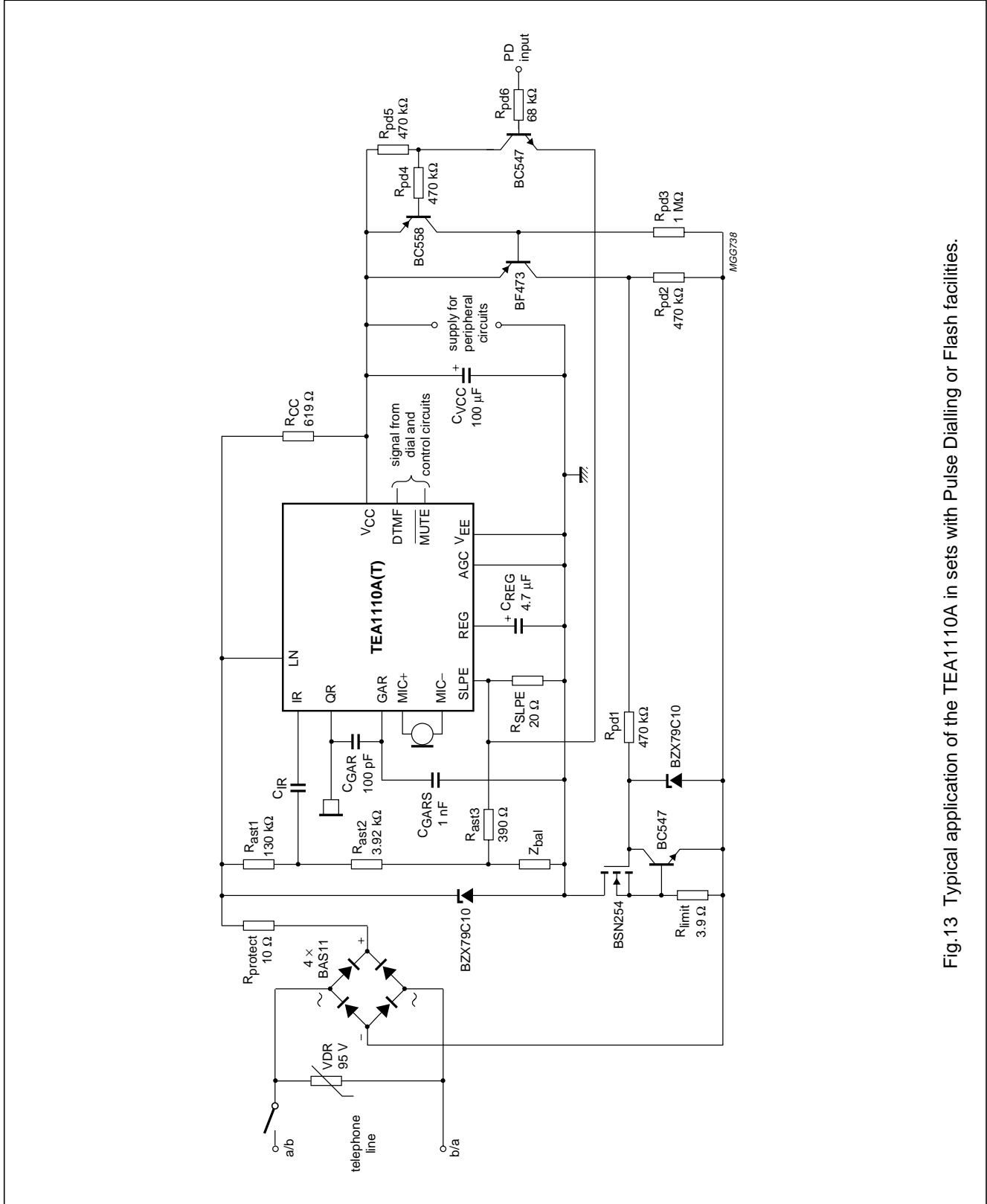


Fig.13 Typical application of the TEA1110A in sets with Pulse Dialling or Flash facilities.

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BONDING PAD LOCATIONS FOR TEA1110AUH

All x/y coordinates represent the position of the centre of the pad (in μm) with respect to the origin ($x/y = 0/0$) of the die (see Fig.14). The size of all pads is $80\ \mu\text{m} \times 80\ \mu\text{m}$.

SYMBOL	PAD	COORDINATES	
		x	y
LN	1	123	782
SLPE	2	251	459
REG	3	490.2	459
n.c.	4	685	459
DTMF	5	1174	459
MUTE	6	1450	459
IR	7	1449	664
AGC	8	1449.2	1006.8
MIC-	9	1297	1200
MIC+	10	1108	1200
V _{EE}	11	678	1200
QR	12	318.2	1200.2
GAR	13	123	1201
V _{CC}	14	123	1017.8

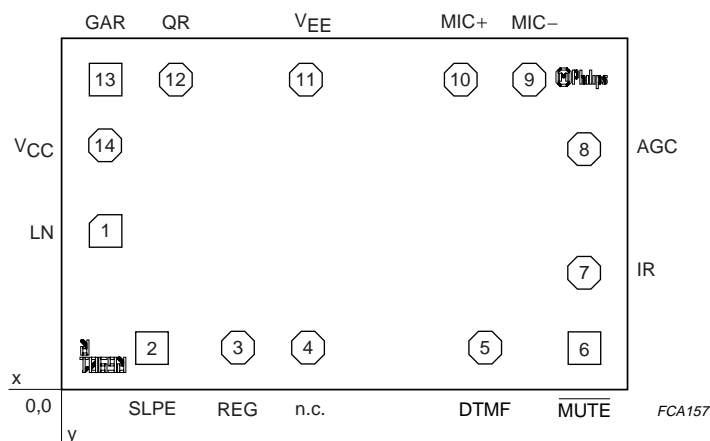


Fig.14 TEA1110AUH bonding pad locations.

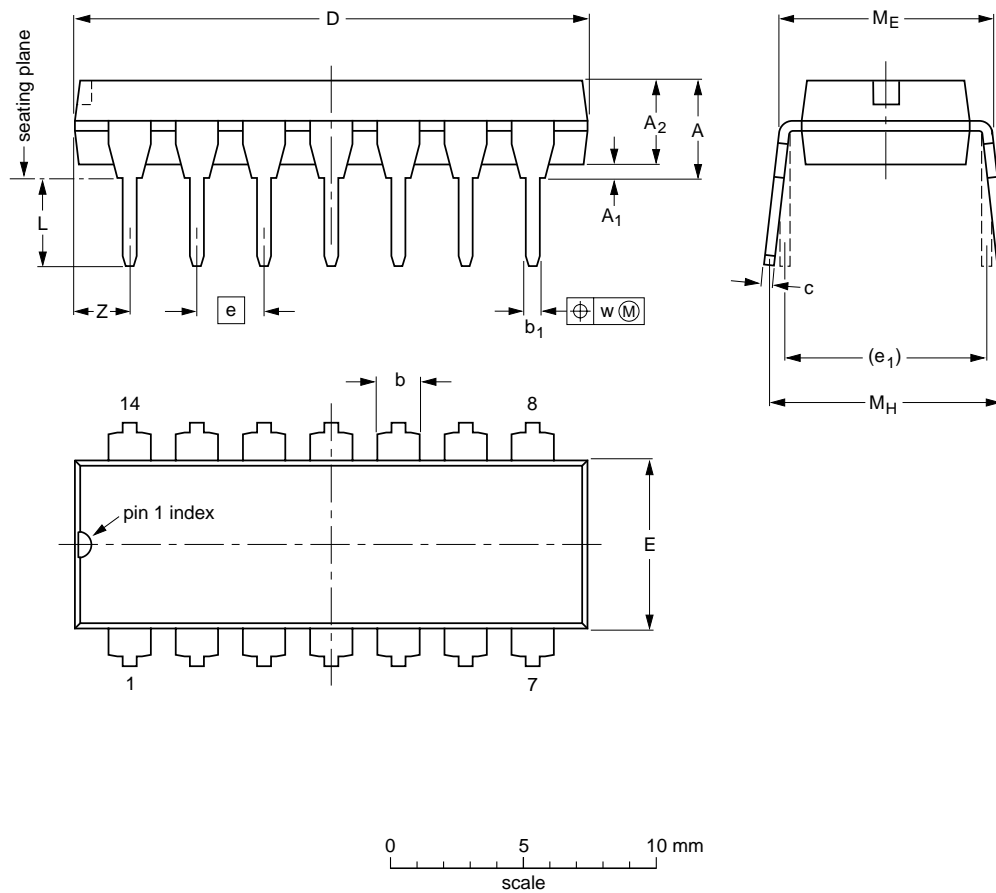
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PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

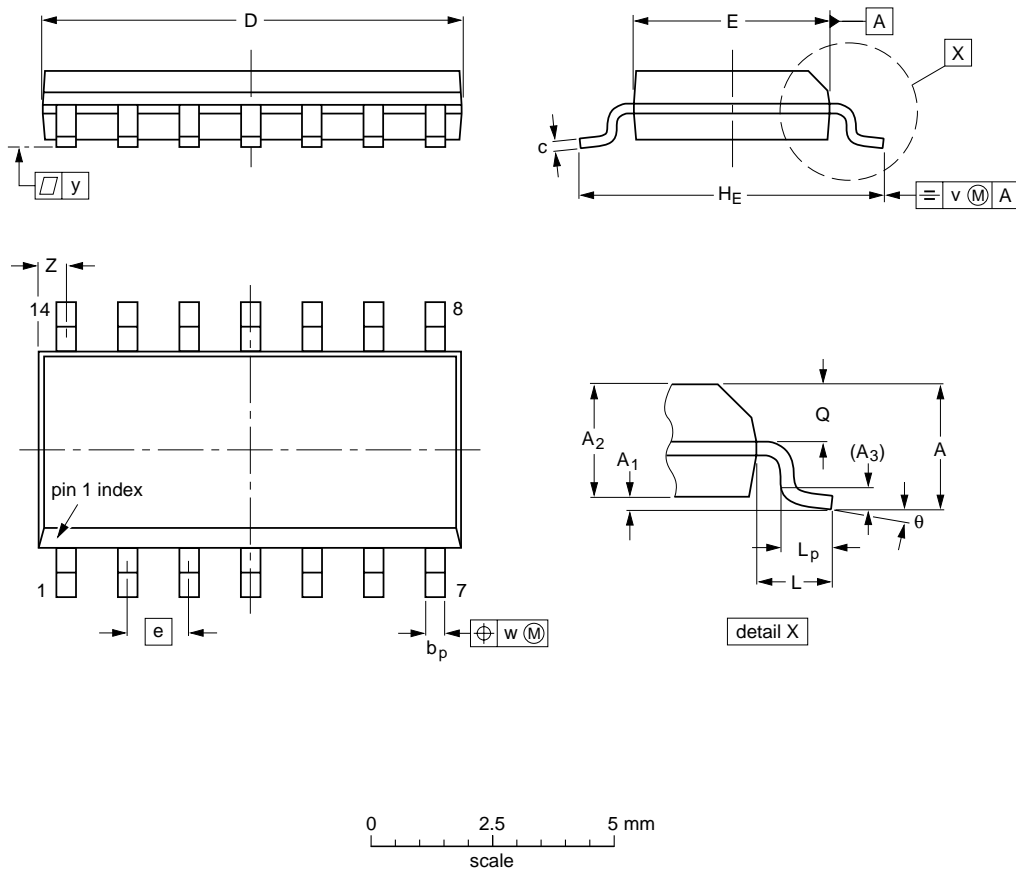
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			95-03-11 99-12-27

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

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When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽³⁾	suitable	–
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	–
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	–

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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NOTES

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