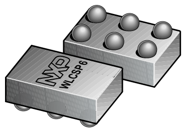


BGU8103UK

SiGe:C LNA MMIC for GPS, GLONASS, Galileo and COMPASS

Rev. 1 — 25 January 2016 **Preliminary data sheet**

1. General description

The BGU8103UK is an ultra low current and Low-Noise Amplifier (LNA) for GNSS receiver applications. It comes as an extremely small and thin Wafer Level Chip Scale Package (WLCSP). This product is only used in an overmolded module. The BGU8103UK requires only one external matching inductor.

The BGU8103UK adapts itself to the changing environment resulting from co-habitation of different radio systems in modern cellular handsets. It has been designed for ultra low power consumption and optimal performance when jamming signals from co-existing cellular transmitters are present. At low jamming power levels, it delivers 18.5 dB gain at a noise figure of 0.80 dB and a supply current of 1.2 mA. During high jamming power levels, resulting for example from a cellular transmit burst, it temporarily increases its bias current to improve sensitivity.

2. Features and benefits

- Optimized performance at a low supply current of 1.2 mA
- Covers full GNSS L1 band, from 1559 MHz to 1610 MHz
- Noise figure = 0.80 dB
- Gain 18.5 dB
- Input 1 dB compression point of –17 dBm
- Out of band $IP3_i$ of –11 dBm
- Supply voltage 1.5 V to 3.1 V
- Integrated supply decoupling capacitor
- Power-down mode current consumption < 1 μA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Integrated DC blocking at both RF input and output
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Available in a WLCSP 0.69 mm × 0.44 mm × 0.29 mm: SOT1445-1
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level 1

3. Applications

- LNA for GPS
- GLONASS
- Galileo and COMPASS (BeiDou) in smart phones
- Feature phones
- Tablet PCs
- Digital still cameras
- Digital video cameras
- RF front-end modules
- Complete GNSS modules and wearable applications

4. Quick reference data

Table 1. Quick reference data

f = 1575 MHz; V_{CC} = 1.8 V; $V_{I(ENABLE)} \geq$ 0.8 V; P_i < –40 dBm; T_{amb} = 25 °C; input matched to 50 Ω using a 12 nH inductor; see Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
I_{CC}	supply current		-	1.2	-	mA
G_p	power gain	no jammer	-	18.5	-	dB
NF	noise figure	P_i = –40 dBm; no jammer [1]	-	0.8	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression		-	–17	-	dBm
$IP3_i$	input third-order intercept point	[2]	-	–11	-	dBm

[1] PCB losses are subtracted.

[2] f_1 = 1713 MHz; f_2 = 1851 MHz; P_i = –20 dBm at f_1; P_i = –65 dBm at f_2.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BGU8103UK	WLCSP6	wafer level chip-scale package; 6 bumps; 0.69 × 0.44 × 0.29 mm	SOT1445-1

6. Marking

Table 3. Marking codes

Type number	Marking code
BGU8103UK	single character, indicating assembly month[1]

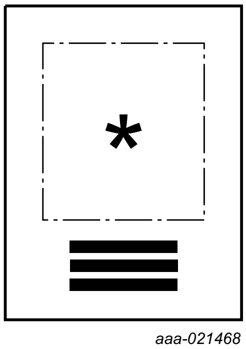
[1] Month codes see Table 4.

Table 4. Calender marking month code

Replace asterisk (*) by character in table, see Figure 1.

Year[1]	Month											
	J	**F**	**M**	**A**	**M**	**J**	**J**	**A**	**S**	**O**	**N**	**D**
2015	A	B	C	D	E	F	G	H	I	J	K	L
2016	M	N	O	P	Q	R	S	T	U	V	W	X
2017	Y	Z	b	d	f	h	3	4	5	6	7	9

[1] Rotates every 3 years.



Pin A1 location: the marking stripes below character indicate the side where pin A1 is located.

Fig 1. Marking code description example

7. Block diagram

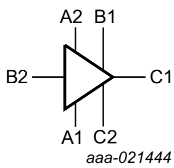


Fig 2. Block diagram

8. Pinning information

8.1 Pinning

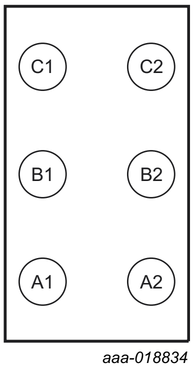


Fig 3. Bump side view

8.2 Pin description

Table 5. Bump description

Symbol	Bump	Description
GND	A1	ground
V_{CC}	B1	supply voltage
RF_OUT	C1	RF output
ENABLE	A2	enable
RF_IN	B2	RF input
GND_RF	C2	ground RF

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	RF input AC coupled	[1]	–0.5	+5.0	V
$V_{I(ENABLE)}$	input voltage on pin ENABLE	$V_{I(ENABLE)} < V_{CC} + 0.6$ V	[1][2]	–0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC; $V_{I(RF\_IN)} < V_{CC} + 0.6$ V	[1][2][3]	–0.5	+5.0	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC; $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V	[1][2][3]	–0.5	+5.0	V
P_i	input power		[1]	-	10	dBm
P_{tot}	total power dissipation	$T_{sp} \leq 130$ °C		-	55	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C

Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to JEDEC standard JS-001-2010	-	±2	kV
		Charged Device Model (CDM) according to JEDEC standard JESD22-C101C	-	±2	kV

[1] Stressed with pulses of 200 ms in duration, with application circuit as in Figure 4.

[2] Warning: due to internal ESD diode protection, the applied DC voltage shall not exceed V_{CC} + 0.6 V and shall not exceed 5.0 V in order to avoid excess current.

[3] The RF input and RF output are AC coupled through internal DC blocking capacitors.

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		–40	+25	+85	°C
$V_{I(ENABLE)}$	input voltage on pin ENABLE	OFF state	-	-	0.3	V
		ON state	0.8	-	-	V

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12. Characteristics

Table 9. Characteristics at V_{CC} = 1.8 V

f = 1575 MHz; V_{CC} = 1.8 V; $V_{I(ENABLE)} \geq 0.8$ V; $P_i < -40$ dBm; T_{amb} = 25 °C; input matched to 50 Ω using a 12 nH inductor; see Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	$V_{I(ENABLE)} \geq 0.8$ V					
		$P_i < -40$ dBm		-	1.2	-	mA
		$P_i = -20$ dBm		-	2.5	-	mA
		$V_{I(ENABLE)} \leq 0.3$ V		-	-	1	µA
G_p	power gain	no jammer		-	18.5	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 850 MHz		-	20.0	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 1850 MHz		-	20.0	-	dB
RL_{in}	input return loss	$P_i < -40$ dBm		-	8	-	dB
		$P_i = -20$ dBm		-	9	-	dB
RL_{out}	output return loss	$P_i < -40$ dBm		-	11	-	dB
		$P_i = -20$ dBm		-	11	-	dB
ISL	isolation			-	35	-	dB
NF	noise figure	$P_i = -40$ dBm; no jammer	[1]	-	0.8	-	dB
		$P_i = -40$ dBm; no jammer	[2]	-	0.9	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 850 MHz	[2]	-	1.1	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 1850 MHz	[2]	-	1.4	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression			-	−17	-	dBm
$IP3_i$	input third-order intercept point		[3]	-	−11	-	dBm
IMD3	third-order intermodulation distortion	output referred	[3]	-	−64	-	dBm
t_{on}	turn-on time	time from $V_{I(ENABLE)}$ ON to 90 % of the gain		-	-	2	µs
t_{off}	turn-off time	time from $V_{I(ENABLE)}$ OFF to 10 % of the gain		-	-	1	µs

[1] PCB losses are subtracted.

[2] Including PCB losses.

[3] f_1 = 1713 MHz; f_2 = 1851 MHz; $P_i = -20$ dBm at f_1; $P_i = -65$ dBm at f_2.

Table 10. Characteristics at V_{CC} = 2.85 V

f = 1575 MHz; V_{CC} = 2.85 V; $V_{I(ENABLE)} \geq 0.8$ V; $P_i < -40$ dBm; T_{amb} = 25 °C; input matched to 50 Ω using a 12 nH inductor; see Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	$V_{I(ENABLE)} \geq 0.8$ V					
		$P_i < -40$ dBm		-	1.2	-	mA
		$P_i = -20$ dBm		-	2.5	-	mA
		$V_{I(ENABLE)} \leq 0.3$ V		-	-	1	μA
G_p	power gain	no jammer		-	18.5	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 850 MHz		-	20.0	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 1850 MHz		-	20.0	-	dB
RL_{in}	input return loss	$P_i < -40$ dBm		-	8	-	dB
		$P_i = -20$ dBm		-	9	-	dB
RL_{out}	output return loss	$P_i < -40$ dBm		-	11	-	dB
		$P_i = -20$ dBm		-	11	-	dB
ISL	isolation			-	35	-	dB
NF	noise figure	$P_i = -40$ dBm; no jammer	[1]	-	0.8	-	dB
		$P_i = -40$ dBm; no jammer	[2]	-	0.9	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 850 MHz	[2]	-	1.1	-	dB
		$P_{jam} = -20$ dBm; f_{jam} = 1850 MHz	[2]	-	1.4	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression			-	–14	-	dBm
$IP3_i$	input third-order intercept point		[3]	-	–9	-	dBm
IMD3	third-order intermodulation distortion	output referred	[3]	-	–68	-	dBm
t_{on}	turn-on time	time from $V_{I(ENABLE)}$ ON to 90 % of the gain		-	-	2	μs
t_{off}	turn-off time	time from $V_{I(ENABLE)}$ OFF to 10 % of the gain		-	-	1	μs

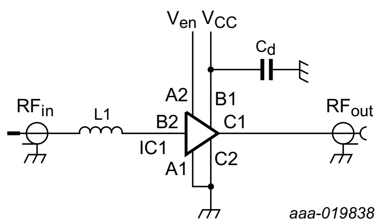
[1] PCB losses are subtracted.

[2] Including PCB losses.

[3] f_1 = 1713 MHz; f_2 = 1851 MHz; $P_i = -20$ dBm at f_1; $P_i = -65$ dBm at f_2.

13. Application information

13.1 GNSS LNA



For a list of components, see Table 11.

Fig 4. Schematics GNSS LNA evaluation board

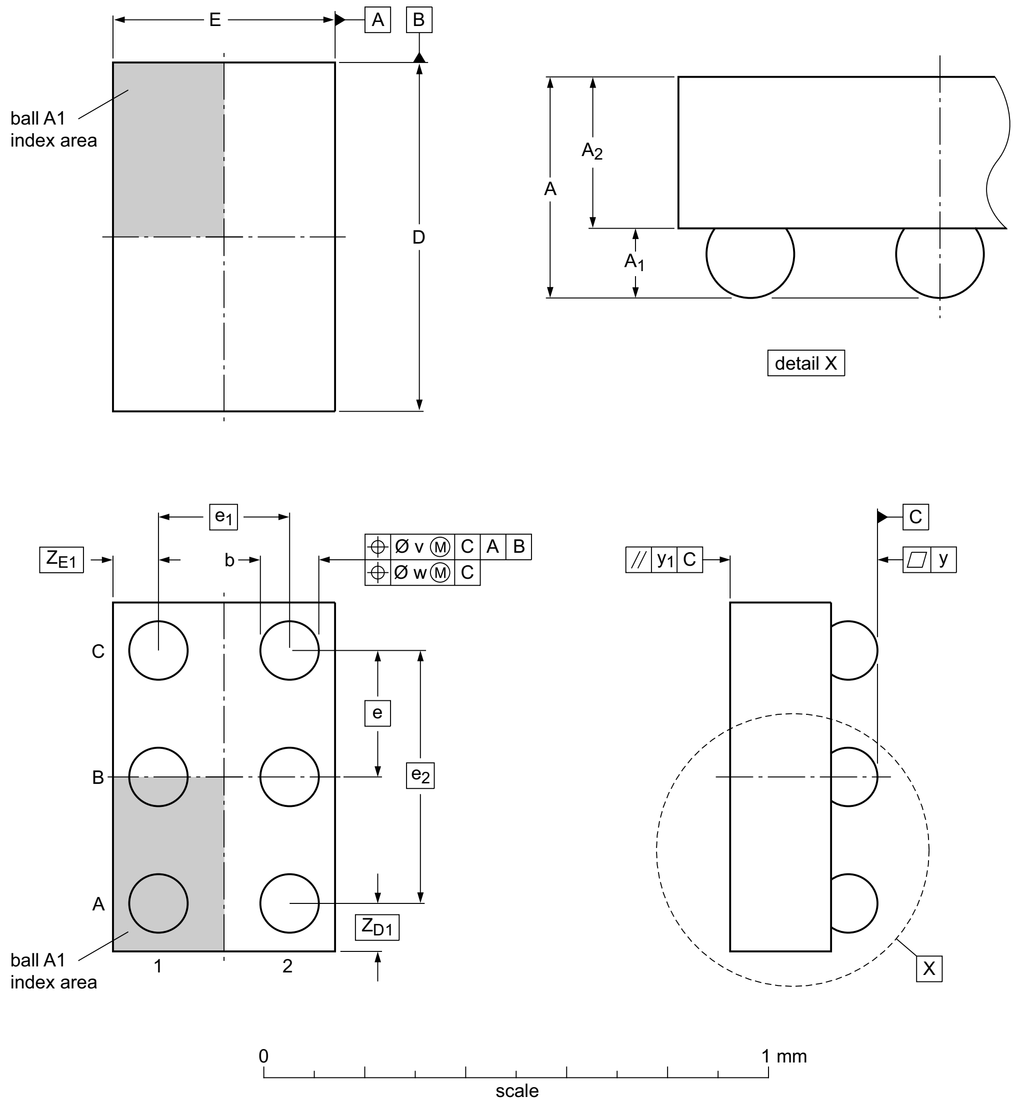
Table 11. List of components

For schematics, see Figure 4.

Component	Description	Value	Remarks
C_d	decoupling capacitor	1 nF	to suppress power supply noise
IC1	BGU8103UK	-	NXP Semiconductors
L1	high-quality matching inductor	12 nH	Murata LQW15A

14. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 0.44 x 0.29 mm **SOT1445-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1	Z_{D1}	Z_{E1}
	max	0.31	0.105	0.215	0.131	0.705	0.455								0.105	0.10
mm	nom	0.29	0.090	0.200	0.116	0.690	0.440	0.25	0.26	0.50	0.15	0.05	0.03	0.05	0.095	0.09
	min	0.27	0.075	0.185	0.101	0.675	0.425								0.085	0.08

sot1445-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1445-1						~~15-04-28~~ 15-05-11

Fig 5. Package outline SOT1445-1 (WLCSP6)

15. Handling information

15.1 ElectroStatic Discharge (ESD)

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

16. Mounting

This WLCSP is only used in an overmolded module (using MUF).

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
LNA	Low-Noise Amplifier
HBM	Human Body Model
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded UnderFill
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon
WLCSP	Wafer Level Chip Scale Package

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGU8103UK v.1	20160225	Preliminary data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
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