Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- · Very fast switching
- AEC-Q101 qualified

3. Applications

- Relay driver
- · High-speed line driver
- · High-side load switch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-	-4.1	Α
Static char	racteristics		·	·			
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -2.4 \text{ A}; T_j = 25 \text{ °C}$		-	48	55	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<u> </u>	D -
2	D	drain		
3	G	gate	0 1 1 2 3	G (F)
4	S	source	TSOP6 (SOT457)	s
5	D	drain		017aaa257
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN48XPA	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN48XPA	ВА

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-4.1	Α
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2.5	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-20	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	530	mW
			[1]	-	1.3	W
		T _{sp} = 25 °C		-	6.3	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drai	n diode		'	'		
Is	source current	T _{amb} = 25 °C	[1]	-	-1.4	Α

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

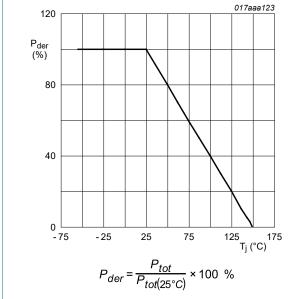


Fig. 1. Normalized total power dissipation as a function of junction temperature

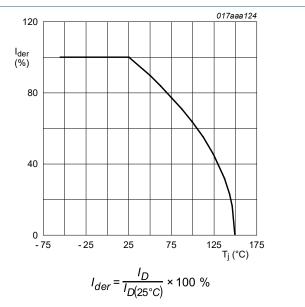


Fig. 2. Normalized continuous drain current as a function of junction temperature

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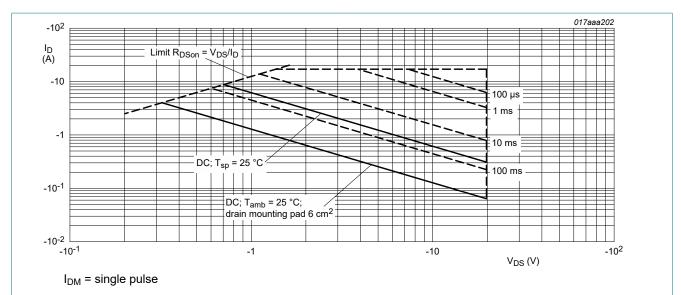


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from	in free air	[1]	-	204	235	K/W
	junction to ambient		[2]	-	84	97	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	17	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

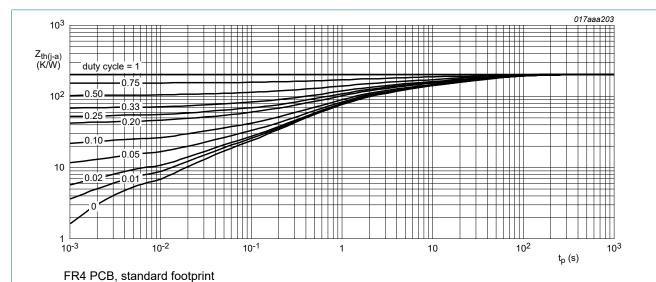
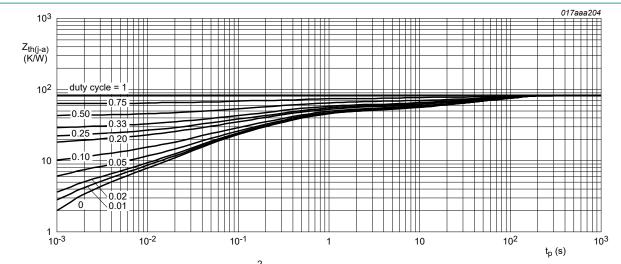


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	-0.75	-1	-1.25	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
		V _{DS} = -20 V; V _{GS} = 0 V; T _j = 150 °C	-	-	-10	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
R _{DSon}	drain-source on-state	$V_{GS} = -4.5 \text{ V}; I_D = -2.4 \text{ A}; T_j = 25 \text{ °C}$	-	48	55	mΩ
	resistance	$V_{GS} = -4.5 \text{ V}; I_D = -2.4 \text{ A}; T_j = 150 \text{ °C}$	-	70	80	mΩ
		$V_{GS} = -2.5 \text{ V}; I_D = -2 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	72	82	mΩ
9fs	forward transconductance	$V_{DS} = -5 \text{ V}; I_D = -2.4 \text{ A}; T_j = 25 \text{ °C}$	-	10	-	S
Dynamic ch	aracteristics			'		
Q _{G(tot)}	total gate charge	$V_{DS} = -10 \text{ V}; I_D = -1 \text{ A}; V_{GS} = -4.5 \text{ V};$	-	8.7	13	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.8	-	nC
Q_{GD}	gate-drain charge		-	1.7	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V;	-	1000	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	130	-	pF
C _{rss}	reverse transfer capacitance		-	90	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -1 A; V _{GS} = -5 V;	-	15	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	22	-	ns
t _{d(off)}	turn-off delay time		-	51	-	ns
t _f	fall time	1	-	22	-	ns
Source-drai	in diode		1		-	
V_{SD}	source-drain voltage	I _S = -2.4 A; V _{GS} = 0 V; T _i = 25 °C	-	-0.75	-1	V

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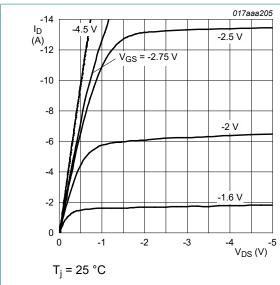


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

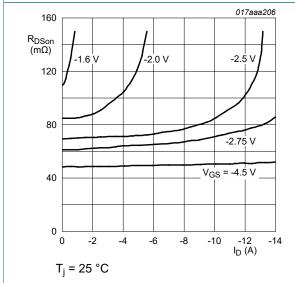


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

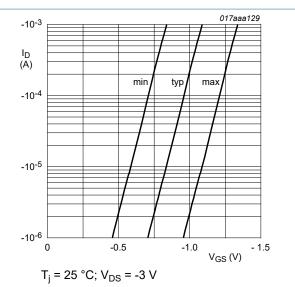


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

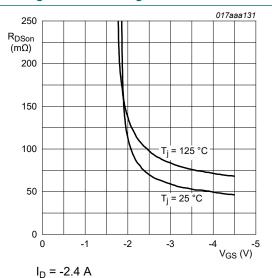


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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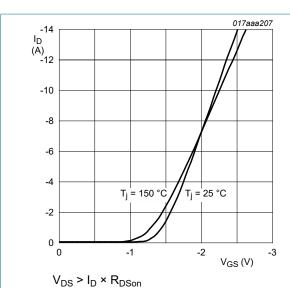


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

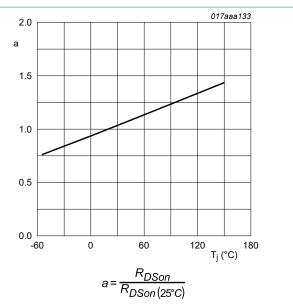


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

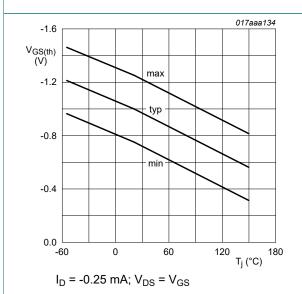
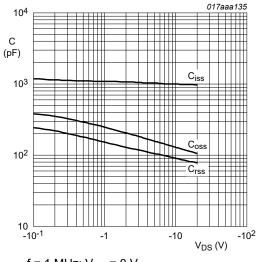


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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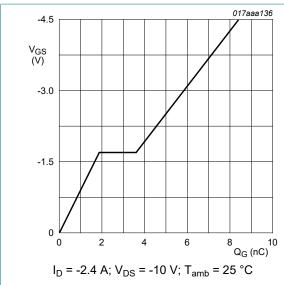


Fig. 14. Gate-source voltage as a function of gate charge; typical values

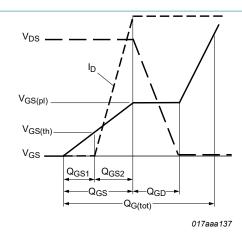


Fig. 15. Gate charge waveform definitions

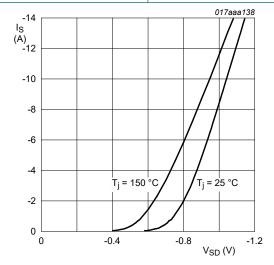
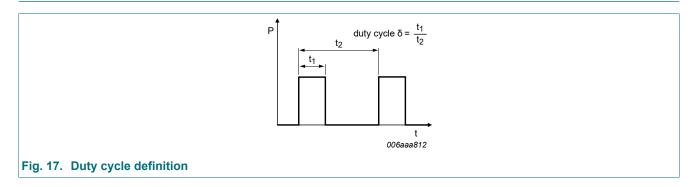


Fig. 16. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0 V$

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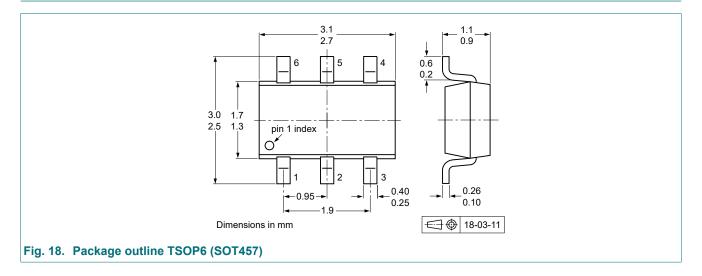
11. Test information



Quality information

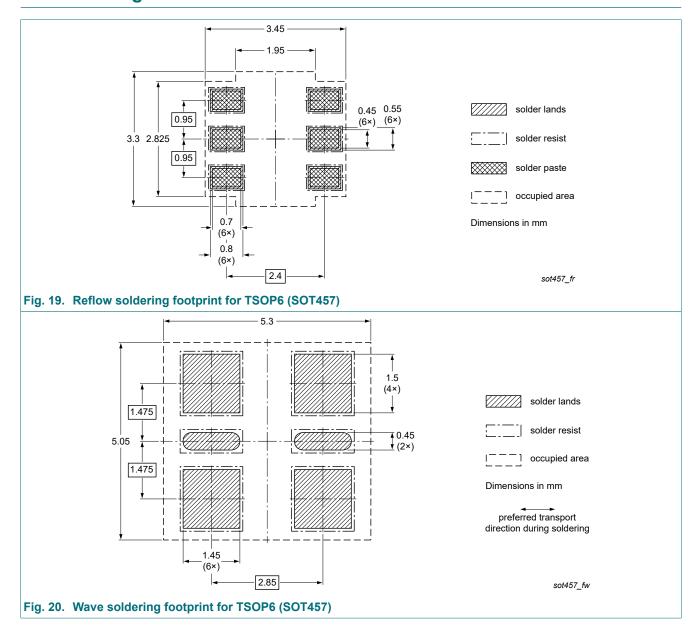
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN48XPA v.1	20190517	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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