4-Bit binary counters — 54F161A, 54F163A

FEATURES

- Synchronous counting and loading
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset (54F161A)
- Synchronous reset (54F163A)
- High-speed synchronous expansion
- Typical count rate of 120MHz

DESCRIPTION

Synchronous 4-bit (54F161A, 54F163A) counters feature an internal carry look- ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D0 - D3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q0 - Q3) in 54F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 54F163A, the clear function is synchronous. A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q0 - Q3) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure B).

For conventional operation of 54F161A and 54F163A, the following transitions should be avoided:

1. High-to-Low transition on the CEP or CET input if Clock is Low.
2. Low-to-High transition on the Parallel Enable input when CP is Low, if the count enables and $\overline{MR}$ are High at or before the transition.

For 54F163A there is an additional transition to be avoided:

3. Low-to-high transition on the $\overline{MR}$ input when Clock is Low, if the Enable and $\overline{PE}$ inputs are High at or before the transition. The TC output is subject to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F161A/BEA 54F163A/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F161A/BFA 54F163A/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F161A/B2A 54F163A/B2A	CQCC2-N20

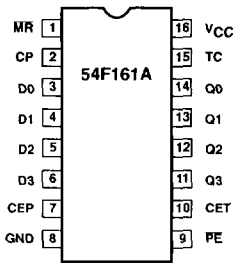
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

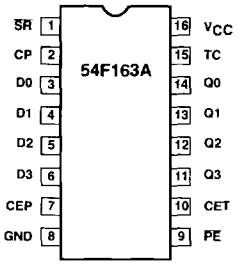
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CEP	Count enable parallel input	1.0/1.0	20µA/0.6mA
CET	Count enable trickle input	1.0/2.0	20µA/1.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous master reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous reset input (active Low)	1.0/2.0	20µA/1.2mA
D0 - D3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel enable input (active Low)	1.0/2.0	20µA/1.2mA
Q0 - Q3	Flip-flop outputs	50/33	1.0mA/20mA
tC	Terminal count output	50/33	1.0mA/20mA

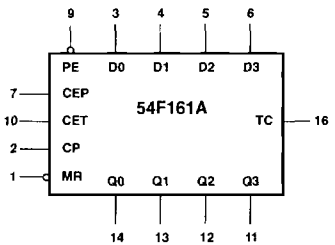
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

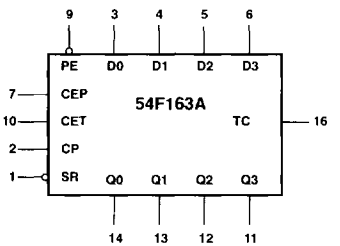
PIN CONFIGURATION



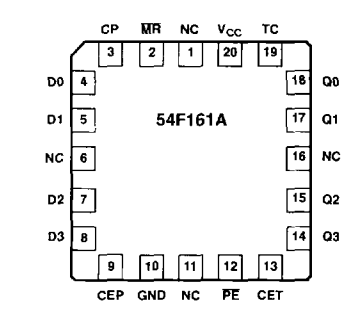
LOGIC SYMBOL



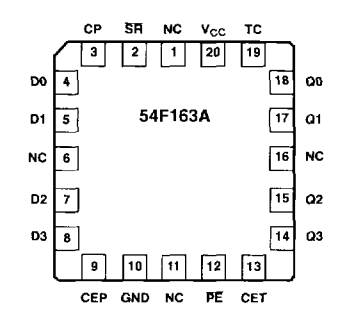




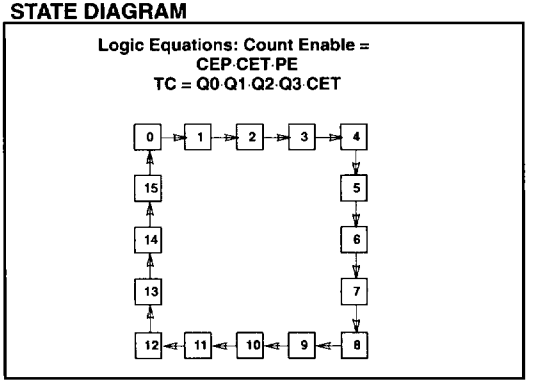
LLCC LEAD CONFIGURATION



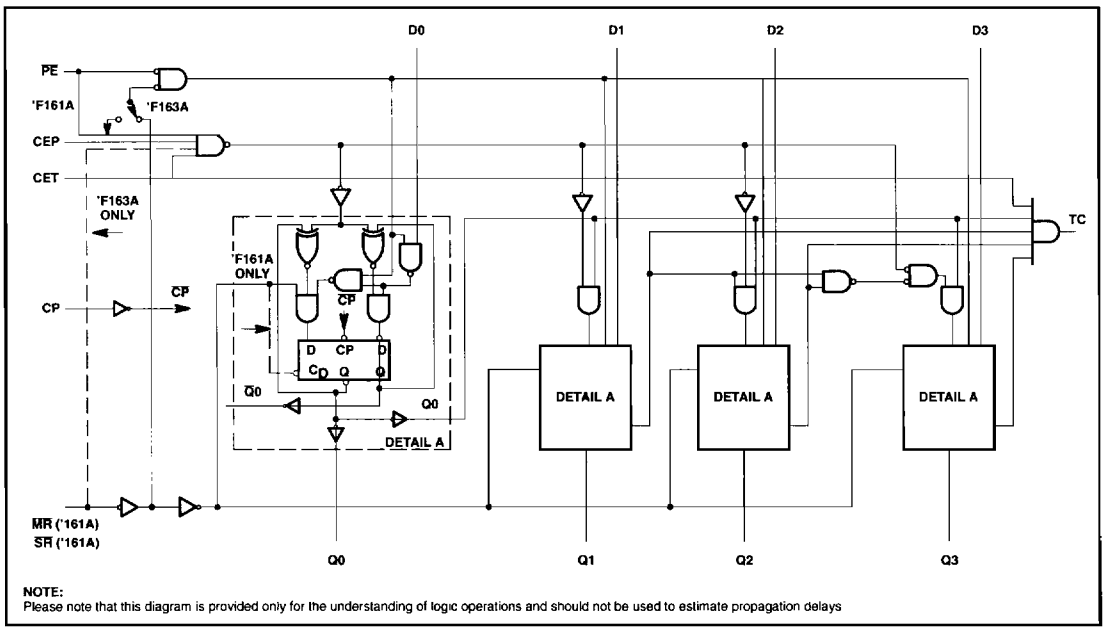
LLCC LEAD CONFIGURATION



STATE DIAGRAM



LOGIC DIAGRAM



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

MODE SELECT — FUNCTION TABLE, 54F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l[2]	h	X	q_n	L

MODE SELECT — FUNCTION TABLE, 54F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(2)
Count	h	↑	h	h	h	X	count	(2)
Hold (do nothing)	h	X	l	X	h	X	q_n	(2)
	h	X	X	l	h	X	q_n	L

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTES:
(1) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54F161A)
(2) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54F163A)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20.0	ma
T_{amb}	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	CET, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 2.7V			40	µA
		Other inputs				20	µA
I_{IL}	Low-level input current	CET, $\overline{SR}$, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V			-1.2	mA
		Other inputs				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	-60		-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX			55	mA
		I_{CCL}				55	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		75[5]		MHz
t_{PLH} t_{PHL}	Propagation delay *CP to Q_n*	Waveform 1 *$\overline{PE}$ = High*	2.0 3.5	4.0 7.0	6.5 10.0	2.0 3.5	7.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = Low	2.0 3.0	4.0 6.0	7.0 8.5	2.0 3.0	8.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	4.0 3.5	10.0 14.0	14.0 16.0	4.0 3.5	16.5 18.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	Waveform 2	2.0 2.0	4.5 4.5	7.5 7.5	2.0 2.0	9.0 9.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n (54F161A)	Waveform 3	5.5	9.0	12.0	5.5	14.0	ns
t_{PHL}	Propagation delay *$\overline{MR}$ to TC (54F161A)*	Waveform 3	4.5		11.5	4.5	14.0	ns

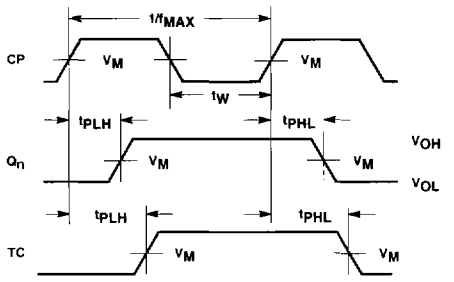
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 5	5.0 5.0			5.5 5.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 5	2.0 2.0			2.5 2.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	11.0 8.5			13.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	2.0 0			2.0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP	Waveform 4	11.0 5.0			13.0 6.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP	Waveform 4	2.0 0			2.0 0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width (load), High or Low	Waveform 1	6.5 3.5			9.0 4.0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width (count), High or Low	Waveform 1	6.5 3.5			9.0 4.0		ns ns
$t_w(L)$	$\overline{MR}$ pulse width Low (54F161A)	Waveform 3	5.0			9.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP (54F161A)	Waveform 3	6.0			6.0		ns

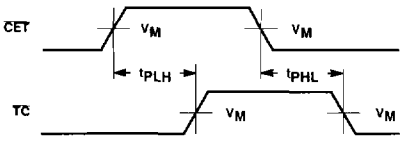
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with the outputs left open and by setting the outputs Low for I_{CCL} and again by setting the outputs high for I_{CCH}.
5. These parameters are guaranteed, but not tested.
6. Pulse width tests are guaranteed as specified, but tested at 7.0ns due to tester limitations.

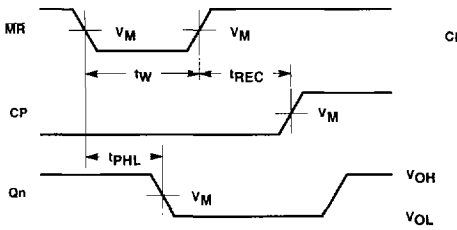
AC WAVEFORMS



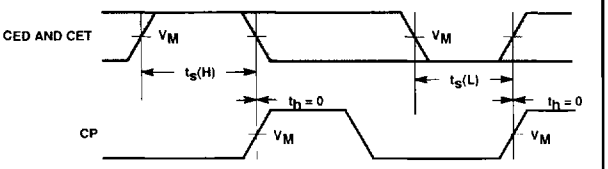
Waveform 1. Clock to Output Delays, Maximum Clock Frequency, and Clock Pulse Width



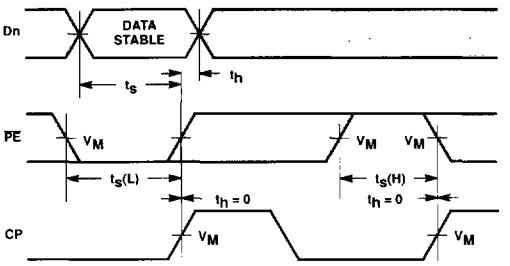
Waveform 2. Propagation Delays CET Input to TC Output



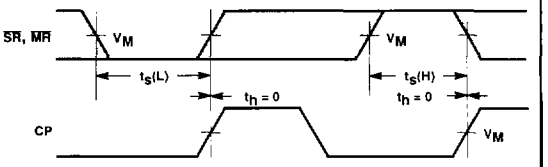
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time (54F161A)



Waveform 4. CEP and CET Setup and Hold Times



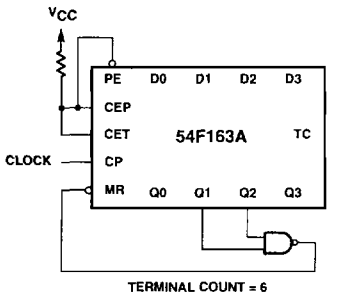
Waveform 5. Parallel Data and Parallel Enable Setup and Hold Times



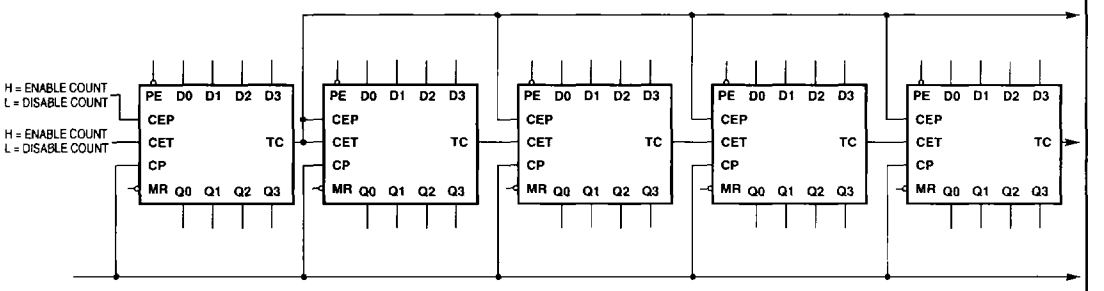
Waveform 6. Synchronous Reset Setup, Pulse Width and Hold Times (54F163A)

NOTE: For all waveforms $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance

APPLICATION DIAGRAM

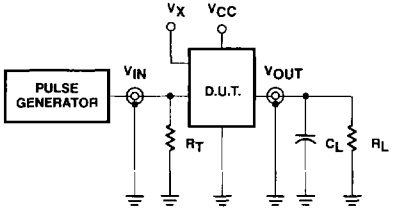


a. A Maximum Count Modifying Scheme
Terminal Count = 6

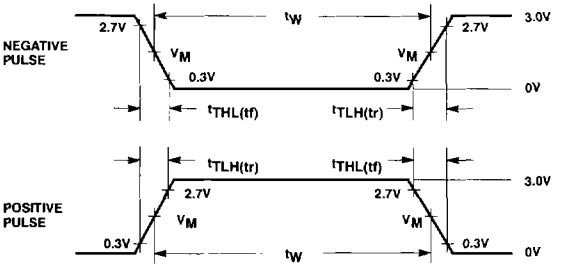


b. Synchronous Multistage Counting Scheme

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



VM = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns