

DATA SHEET

AU2903

Low power dual voltage comparator

Product data
Supersedes data of 1994 Aug 31
File under Integrated Circuits, IC11 Handbook

2001 Aug 03

Low power dual voltage comparator

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DESCRIPTION

The AU2903 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

FEATURES

- Wide single supply voltage range 2.0 V_{DC} to 36 V_{DC}, or dual supplies ±1.0 V_{DC}, to ±18 V_{DC}
- Very low supply current drain (0.8 mA) independent of supply voltage (2.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators.

PIN CONFIGURATION

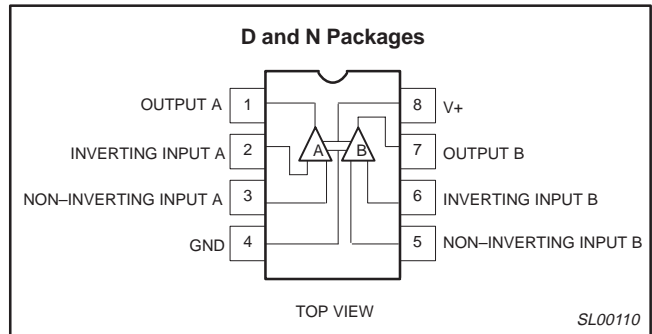


Figure 1. Pin configuration.

EQUIVALENT CIRCUIT

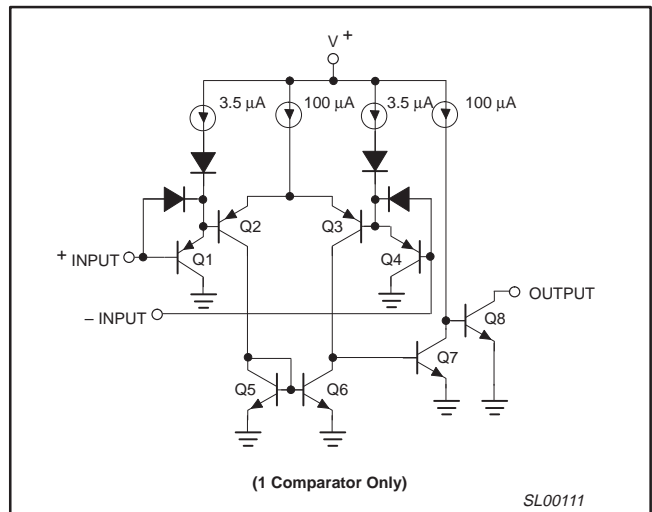


Figure 2. Equivalent circuit.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	-40 °C to +125 °C	AU2903D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40 °C to +125 °C	AU2903N	SOT97-1

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ± 18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation; $T_{amb} = 25\text{ }^{\circ}\text{C}$ (still-air) ³		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground ¹	Continuous	
I_{IN}	Input current ($V_{IN} < -0.3 V_{DC}$) ²	50	mA
T_{amb}	Operating temperature range	-40 to +125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
T_{sld}	Lead soldering temperature (10 sec max)	230	$^{\circ}\text{C}$

NOTES:

- Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $V+$.
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $V+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3 V_{DC}$.
- Derate above $25\text{ }^{\circ}\text{C}$, at the following rates:
 N package at $9.3\text{ mW}/^{\circ}\text{C}$
 D package at $6.2\text{ mW}/^{\circ}\text{C}$

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DC AND AC ELECTRICAL CHARACTERISTICS

 $V_+ = 5 V_{DC}$; $-40\text{ °C} \leq T_{amb} \leq +125\text{ °C}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	Limits			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage ²	$T_{amb} = 25\text{ °C}$ Over temp.		± 2.0	± 3	mV
				± 2.5	± 5	mV
V_{CM}	Input common-mode voltage range ^{3, 6}	$T_{amb} = 25\text{ °C}$ Over temp.	0		$V_+ - 1.5$	V
			0		$V_+ - 2.0$	V
V_{IDR}	Differential input voltage ¹	Keep all $V_{IN} \geq 0 V_{DC}$ (or V_- if need)			V_+	V
I_{BIAS}	Input bias current ⁴	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_{amb} = 25\text{ °C}$ Over temp.		25	250	nA
				200	500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_{amb} = 25\text{ °C}$ Over temp.		± 5	± 50	nA
				± 50	± 200	nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$; $V_{IN(+)} = 0$; $V_O \leq 1.5V_{DC}$; $T_{amb} = 25\text{ °C}$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1 V_{DC}$; $V_{IN(-)} = 0$ $V_O = 5 V_{DC}$; $T_{amb} = 25\text{ °C}$ $V_O = 30 V_{DC}$; over temp.		0.1		nA
					1.0	μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_{amb} = 25\text{ °C}$ $V_+ = 30 V$; over temp.		0.8	1	mA
				1	2.5	mA
A_V	Voltage gain	$R_L \geq 15\text{ k}\Omega$; $V_+ = 15 V_{DC}$; $T_{amb} = 25\text{ °C}$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1 V_{DC}$; $V_{IN(+)} = 0$; $I_{SINK} \leq 4\text{ mA}$ $T_{amb} = 25\text{ °C}$ Over temp.		400	400	mV
					700	mV
t_{LSR}	Large-signal response time	$V_{IN} = \text{TTL logic swing}$; $V_{REF} = 1.4 V_{DC}$; $V_{RL} = 5 V_{DC}$; $R_L = 5.1\text{ k}\Omega$; $T_{amb} = 25\text{ °C}$		300		ns
t_R	Response time ⁵	$V_{RL} = 5 V_{DC}$; $R_L = 5.1\text{ k}\Omega$ $T_{amb} = 25\text{ °C}$		1.3		μs

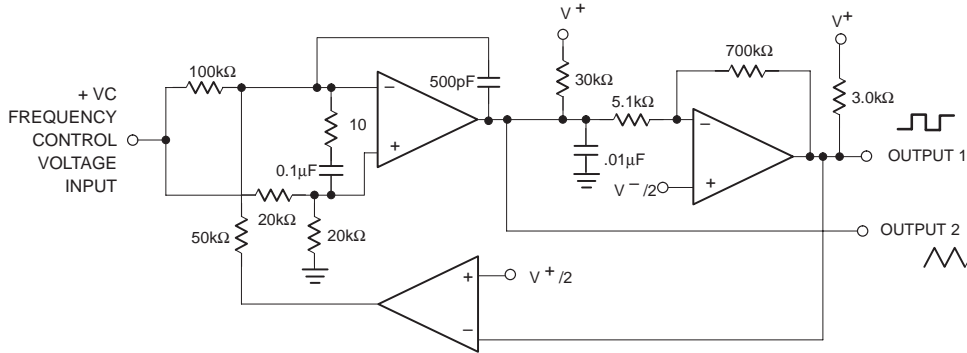
NOTES:

- Positive excursions of input voltage may exceed the power supply level by 17 V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3 V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
- At output switch point, $V_O \approx 1.4 V_{DC}$, $R_S = 0\ \Omega$ with V_+ from $5 V_{DC}$ to $30 V_{DC}$ and over the full input common-mode range ($0 V_{DC}$ to $V_+ - 1.5 V_{DC}$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_+ - 1.5 V$, but either or both inputs can go to $30 V_{DC}$ without damage.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a 100 mV input step with a 5 mV overdrive.
- For input signals that exceed V_{CC} , only the over-driven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

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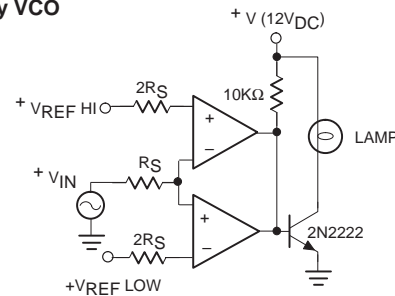
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TYPICAL APPLICATIONS

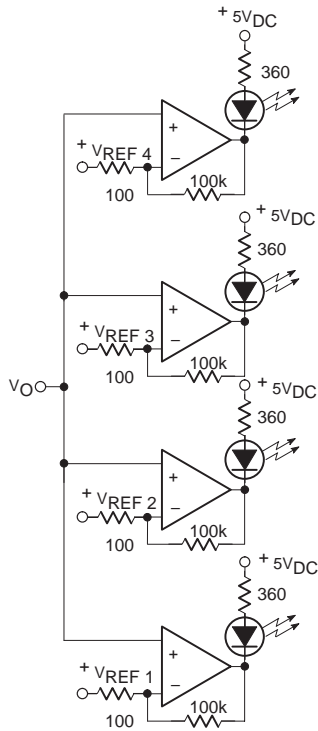


NOTES:
 $V+ = 30V_{DC}$
 $+250mV_{DC} \leq V_C = 50V_{DC}$
 $700H \leq f_O = 100kHz$

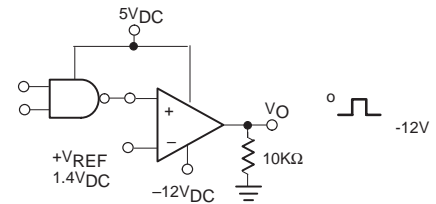
Two-Decade High-Frequency VCO



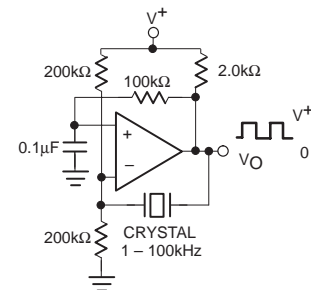
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter



Crystal-Controlled Oscillator

NOTE:
 Input of unused comparators should be grounded.

SL00112

Figure 3. Typical applications.

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TYPICAL PERFORMANCE CHARACTERISTICS

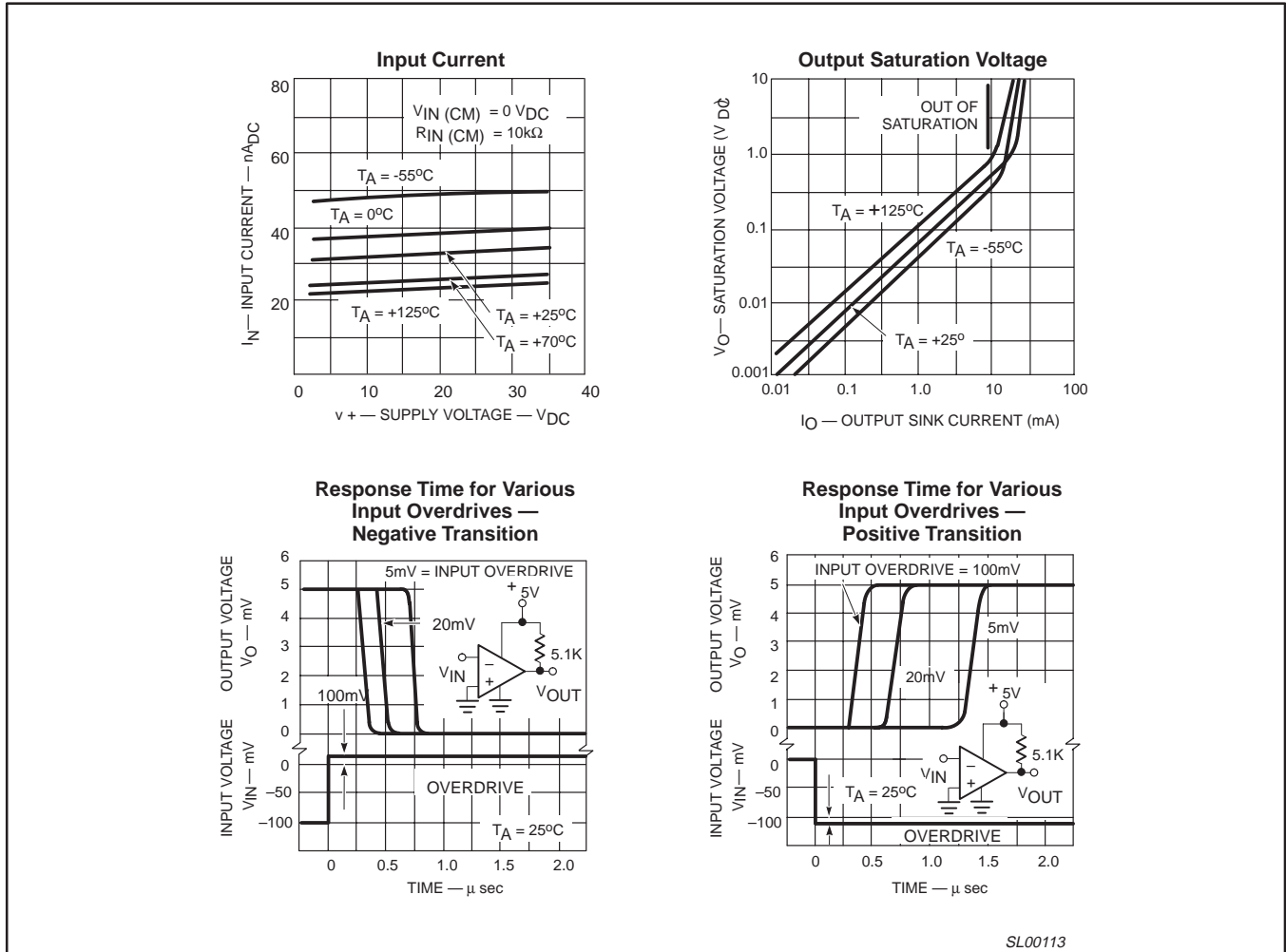


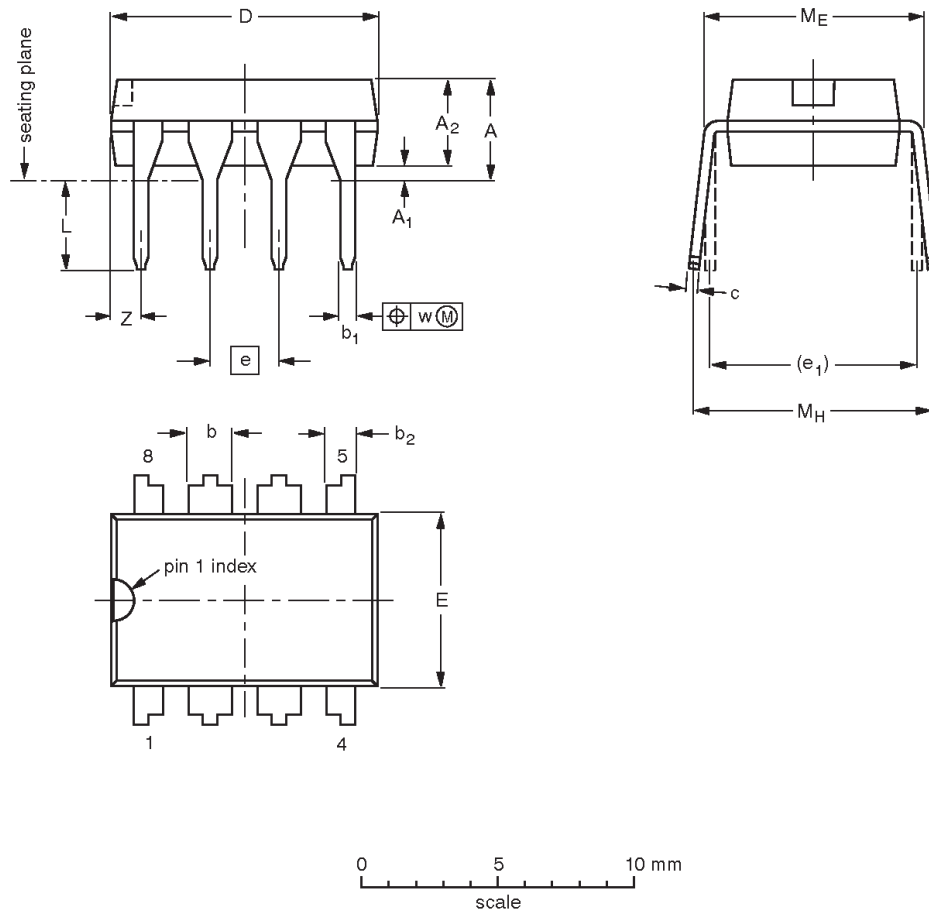
Figure 4. Typical performance characteristics.

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DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			95-02-04 99-12-27

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SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22 99-12-27

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NOTES

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
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