

FUSB303 Autonomous USB Type-C™ Port Controller with I²C and GPIO Control

FUSB303

Description

The FUSB303 device is a fully autonomous USB Type-C™ controller optimized for 15 W or less applications. The FUSB303 offers CC logic detection for Source Port role, Sink Port role, DRP, and accessory detection support, as well as Dead Battery support as defined in USB-C specifications. The FUSB303 features configurable address I²C access to support multiple ports per system or it can operate autonomously configured by just pins. The FUSB303 features ultra-low power during operation, and an ultra-thin, 12-Lead QFN package.

Features

- Fully Autonomous USB-C™ Port Controller
- Supports Latest Type-C™ Specification Release 1.3
- Source, Sink, and DRP Port role Configuration with Optional Accessory Support
- Try.SRC and Try.SNK Modes for Preferring Source Role or Sink Role Respectively
- V_{DD} Operating Range, 2.85 V – 5.5 V
- Typical Low Power Operation: I_{CC} < 10 μA
- GPIO and I²C Configuration
- Max 28 V DC Tolerance on ID, VBUS_DET, CC1 and CC2
- Dead Battery Support (Sink Port Role when No Power Applied)
- 4 kV HBM ESD Protection for Connector Pins
- Small Packaging, 12 Lead QFN (1.6 mm × 1.6 mm × 0.375 mm)

Applications

- Smartphones
- Tablets
- Laptops
- Accessories
- Industrial
- Power Banks



ON Semiconductor®

www.onsemi.com



QFN12
CASE 722AG

MARKING DIAGRAM



1

| | |
|----|-----------------------|
| UD | = FUSB303 Device Code |
| KK | = Lot Trace Code |
| _ | = Pin #1 Identifier |
| XY | = Two Digit Date Code |
| Z | = Assembly Plant Code |

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

FUSB303

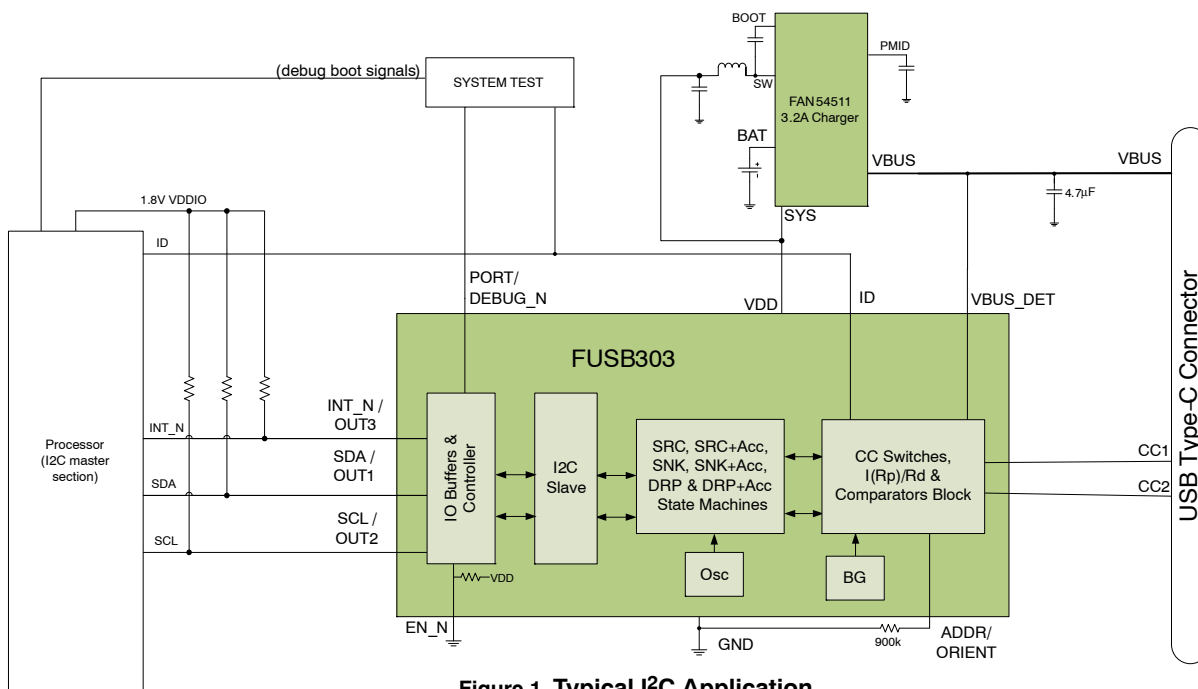


Figure 1. Typical I²C Application

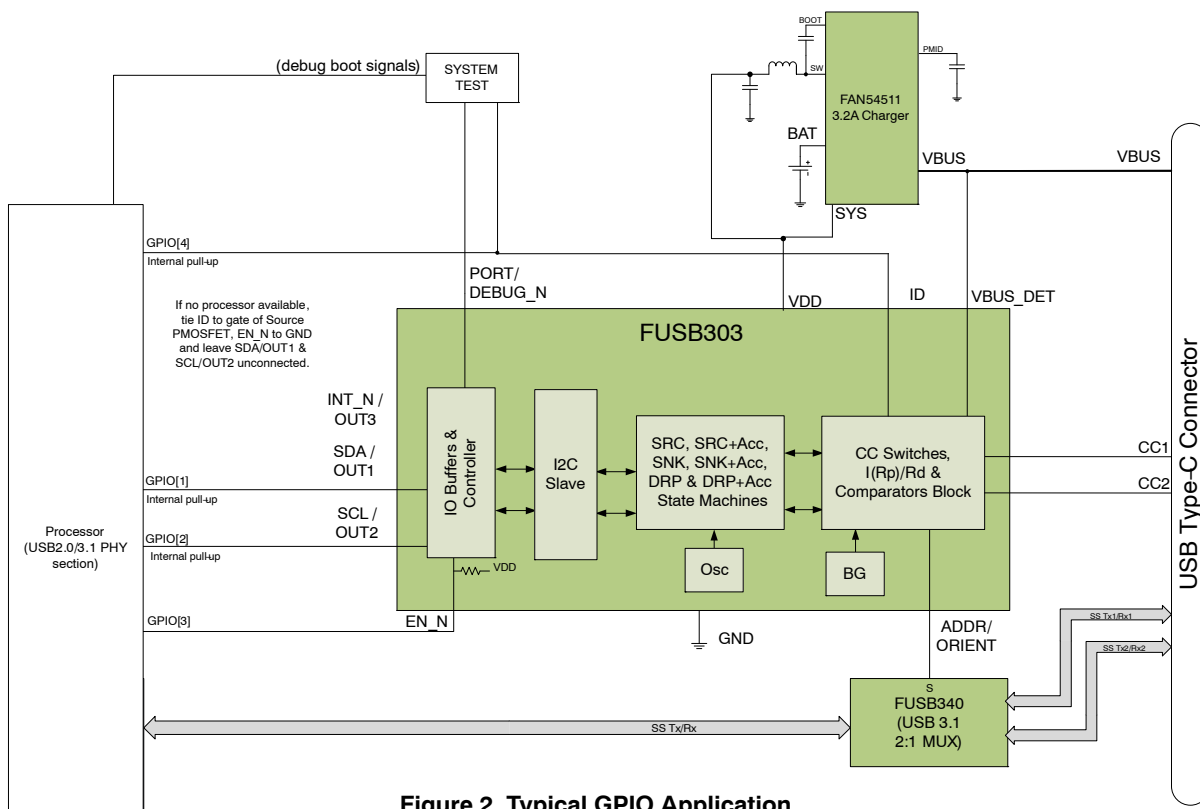


Figure 2. Typical GPIO Application

FUSB303

ORDERING INFORMATION TABLE

Table 1. AVAILABLE PART NUMBERS

| Part Number | Top Mark | Operating Temperature Range | Package | Packing Method† |
|-------------|----------|-----------------------------|---|-----------------|
| FUSB303TMX | UD | -40 to 85°C | 12-Lead Ultra-thin Molded Leadless Package (QFN) 1.6 mm x 1.6 mm x 0.375 mm | Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

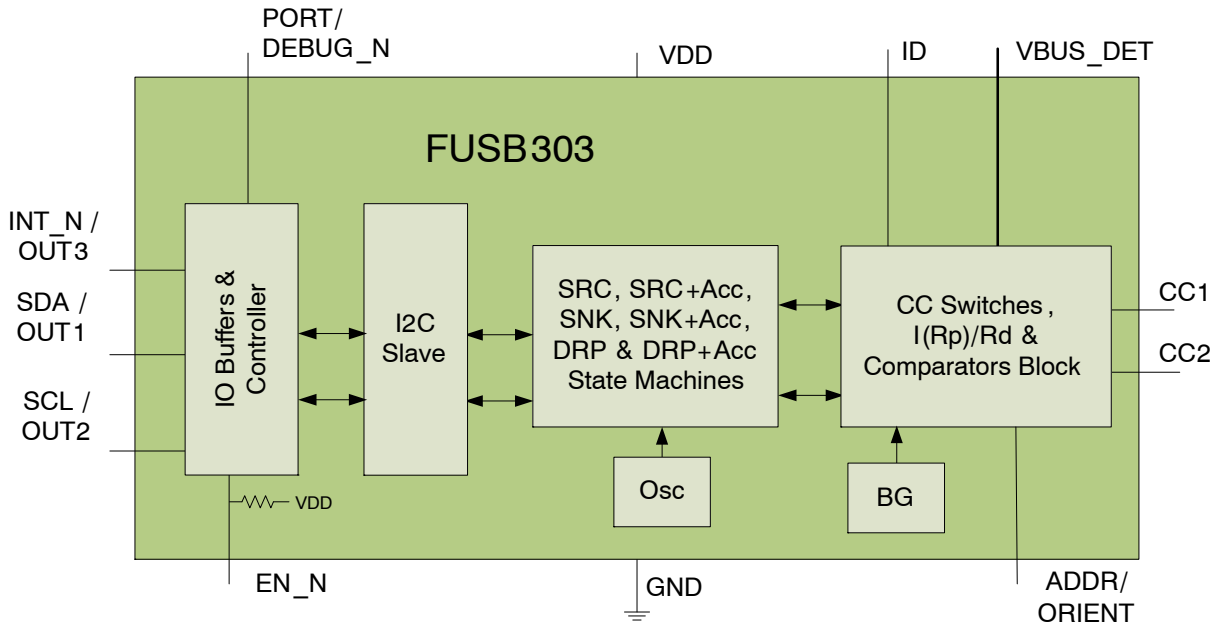


Figure 3. FUSB303 Block Diagram

FUSB303

PIN CONFIGURATION

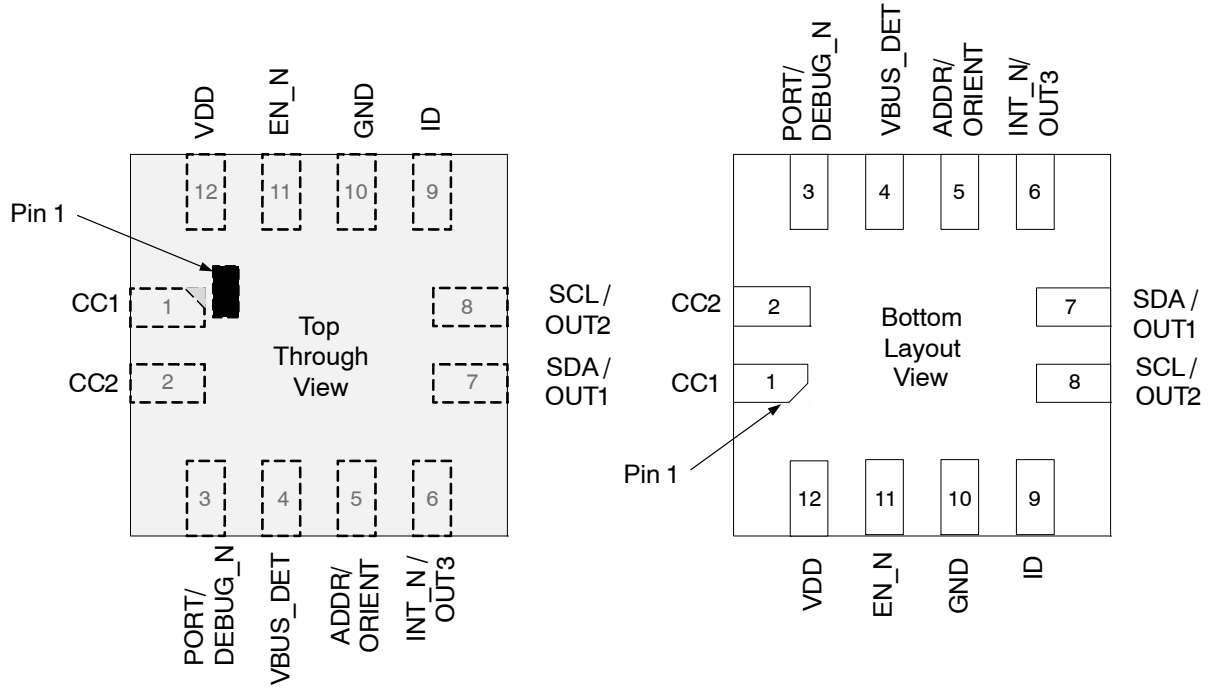


Figure 4. FUSB303 Pin Assignment (Top Through and Bottom Views)

FUSB303

PIN DESCRIPTIONS

Table 2. PIN DESCRIPTIONS

| Pin # | Name | Type | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|--------------|-----------------------------|---|-----------------------------|------------|------------|---------------|--------|------------|---------|--------------------|--------|------------|------------|---------------------------|--------|---------|------------|-------------------------|--------|---------|---------|-----------------------|-----|----------|----------|-----------------------------|-----|---------|----------|---------------------------|-----|---------|---------|-------------------------|-----|----------|---------|-----------------------|
| USB TYPE-C CONNECTOR INTERFACE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1, 2 | CC1, CC2 | I/O | Type-C Configuration Channel pins used for USB-C receptacles | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | VBUS_DET | Input | VBUS input pin for attach and detach detection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| POWER AND GROUND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | GND | Ground | Ground | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | VDD | Power | Input Supply Voltage | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I²C SIGNAL INTERFACE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | INT_N/OUT3 | Open-Drain Output | INT_N/OUT3 is a dual function pin. When in I ² C mode (see ADDR/ORIENT pin), it is the active LOW open drain interrupt output used to prompt the processor to read the I ² C register bits. When the device is in GPIO mode (see ADDR/ORIENT pin), this pin is OUT3, an open drain output LOW = Audio Accessory detected HIGH-Z = Audio Accessory not detected | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | SDA/OUT1 | Open Drain I/O | <p>SDA/OUT1 and SCL/OUT2 are dual function pins. When in I²C mode (see ADDR/ORIENT pin), SDA/OUT1 is the SDA data signal and SCL/OUT2 is the SCL clock signal of the I²C interface. When the device is in GPIO mode (see ADDR/ORIENT pin), these pins are OUT1 and OUT2 inputs (I) or outputs (O) are shown below:</p> <table border="1"> <thead> <tr> <th>ID pin</th> <th>OUT1 (I/O)</th> <th>OUT2 (I/O)</th> <th>Functionality</th> </tr> </thead> <tbody> <tr> <td>HIGH-Z</td> <td>HIGH-Z (O)</td> <td>LOW (O)</td> <td>No Device Attached</td> </tr> <tr> <td>HIGH-Z</td> <td>HIGH-Z (O)</td> <td>HIGH-Z (O)</td> <td>Sink with Default Current</td> </tr> <tr> <td>HIGH-Z</td> <td>LOW (O)</td> <td>HIGH-Z (O)</td> <td>Sink with 1.5 A Current</td> </tr> <tr> <td>HIGH-Z</td> <td>LOW (O)</td> <td>LOW (O)</td> <td>Sink with 3 A Current</td> </tr> <tr> <td>LOW</td> <td>HIGH (I)</td> <td>HIGH (I)</td> <td>Source with Default Current</td> </tr> <tr> <td>LOW</td> <td>LOW (I)</td> <td>HIGH (I)</td> <td>Source with 1.5 A Current</td> </tr> <tr> <td>LOW</td> <td>LOW (I)</td> <td>LOW (I)</td> <td>Source with 3 A Current</td> </tr> <tr> <td>LOW</td> <td>HIGH (I)</td> <td>LOW (I)</td> <td>Reserved (Do Not Use)</td> </tr> </tbody> </table> | ID pin | OUT1 (I/O) | OUT2 (I/O) | Functionality | HIGH-Z | HIGH-Z (O) | LOW (O) | No Device Attached | HIGH-Z | HIGH-Z (O) | HIGH-Z (O) | Sink with Default Current | HIGH-Z | LOW (O) | HIGH-Z (O) | Sink with 1.5 A Current | HIGH-Z | LOW (O) | LOW (O) | Sink with 3 A Current | LOW | HIGH (I) | HIGH (I) | Source with Default Current | LOW | LOW (I) | HIGH (I) | Source with 1.5 A Current | LOW | LOW (I) | LOW (I) | Source with 3 A Current | LOW | HIGH (I) | LOW (I) | Reserved (Do Not Use) |
| ID pin | OUT1 (I/O) | OUT2 (I/O) | | Functionality | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HIGH-Z | HIGH-Z (O) | LOW (O) | | No Device Attached | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HIGH-Z | HIGH-Z (O) | HIGH-Z (O) | | Sink with Default Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HIGH-Z | LOW (O) | HIGH-Z (O) | | Sink with 1.5 A Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| HIGH-Z | LOW (O) | LOW (O) | | Sink with 3 A Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LOW | HIGH (I) | HIGH (I) | | Source with Default Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LOW | LOW (I) | HIGH (I) | | Source with 1.5 A Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LOW | LOW (I) | LOW (I) | Source with 3 A Current | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LOW | HIGH (I) | LOW (I) | Reserved (Do Not Use) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | SCL/OUT2 | Open Drain I/O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GPIO PIN INTERFACE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | PORT/DEBUG_N | Input then Push/Pull Output | PORT/DEBUG_N is a dual function pin: 3 state input to set the port role. On the falling edge of EN_N and when VDD is active or during power up when EN_N is LOW, the state of this pin is sampled. This pin is also sampled on a SW_RES soft reset via I ² C. HIGH = FUSB303 as a Source Only port Float = FUSB303 as a Dual Role Port (DRP) LOW = FUSB303 as a Sink Only port Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current. Subsequently, this pin is the DEBUG_N push-pull output LOW = Debug Accessory detected HIGH = Debug Accessory not detected | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | ADDR/ORIENT | Input then Push/Pull Output | ADDR/ORIENT is a dual function pin: 3 state input to set to I ² C mode and the I ² C address or for GPIO mode. On the falling edge of EN_N and when VDD is active or during power up when EN_N is LOW, the state of this pin is sampled. This pin is also sampled on a SW_RES soft reset via I ² C. HIGH = I ² C mode with address 62h Float = GPIO mode LOW = I ² C mode with address 42h Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current. Subsequently, this pin is the ORIENT push-pull output LOW = CC is CC1 or A5 of the USB-C receptacle HIGH = CC is CC2 or B5 of the USB-C receptacle | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | ID | Open-Drain Output | Open drain output that indicate FUSB303's detection state as a Source or Sink LOW = FUSB303 attached as a Source HIGH-Z = FUSB303 attached as a Sink | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | EN_N | Input | Active LOW device enable input (has internal pull up resistor) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

FUSB303

Table 3. ORIENT PIN VERSUS ORIENT [1:0] REGISTER BITS MAPPING

| CC1 (A5) | CC2 (B5) | STATUS. ORIENT[1] Bit | STATUS. ORIENT[0] Bit | ADDR/ORIENT Pin Output |
|------------------------------------|----------------------|--------------------------|--------------------------|---------------------------|
| FUSB303 CONNECTED AS A SINK | | | | |
| SNK. Open | SNK. Open | 0 | 0 | LOW |
| SNK. Open | SNK. Rp | 1 | 0 | HIGH |
| SNK. Rp | SNK. Open | 0 | 1 | LOW |
| SNK. Rp (Note 2) | SNK. Rp | 0 | 1 | LOW |
| SNK. Rp | SNK. Rp (Note 2) | 1 | 0 | HIGH |
| FUSB303 CONNECTED AS SOURCE | | | | |
| SRC. Open | SRC. Open | 0 | 0 | LOW |
| SRC. Open or SRC. Ra | SRC. Rd | 1 | 0 | HIGH |
| SRC. Rd | SRC. Open or SRC. Ra | 0 | 1 | LOW |
| SRC. Rd (Note 1) | SRC. Rd | 0 | 1 | LOW |
| SRC. Rd | SRC. Rd (Note 1) | 1 | 0 | HIGH |

1. Orientation decoded on this pin after a Sink Debug Test System (DTS) attached to FUSB303.
2. Orientation decoded on this pin after a Source Debug Test System (DTS) attached to FUSB303.

High Voltage Tolerance on CCx and VBUS pins

The FUSB303 has additional protection for the type C connector pins where it can tolerate up to 28V on VBUS, CC1 and CC2 to protect against any misbehaving Type C device connect to the FUSB303. If VBUS tolerance is needed higher than 28V, a 900kΩ resistor can be used externally along with a Transient Voltage Suppressor (TVS) to achieve almost any higher voltage tolerance dictated by the TVS chosen.

Dead Battery

If power is not applied to FUSB303 and it is attached to a Source device, then the Source would pull up the CC line connected through the cable. The FUSB303 in response will turn on the pull-down that will bring the CC voltage to a range that the Source can detect an attached device and turn on VBUS.

GPIO Mode, Debug and Audio Accessories

When VDD is active and on the trailing edge of EN_N, the FUSB303 will sample PORT/DEBUG_N to determine if the FUSB303 operates as a Source (HIGH), Sink (LOW) or DRP (floating). Subsequently the PORT/DEBUG_N will be set LOW when a Debug Test System is detected.

If the FUSB303 is configured as a Sink (PORT/DEBUG_N= LOW upon enable), the FUSB303 will detect a Debug Test System if Rp is detected on both CC1 and CC2. Devices that support orientation detection will also have ADDR/ORIENT set based on the levels detected for CC1 and CC2. ID will be set HIGH-Z.

If the device is configured as a Source (PORT/DEBUG_N= HIGH upon enable), the FUSB303 will detect a Debug Test System if Rd is detected on both CC1 and CC2. Devices that support orientation detection

will also have ADDR/ORIENT set based on the levels detected for CC1 and CC2. ID will be set LOW.

The FUSB303 also supports DRP toggling for detecting debug test systems. When PORT/DEBUG_N= float upon enable, the FUSB303 can detect both Source and Sink debug test systems depending on how it resolves its role as a Source or Sink. Then it acts either as a Source or Sink as described above.

The FUSB303 will report Debug Test System detection via the Type I²C register as well. The detection is the same as described above except Source, Sink and DRP roles are configured via the Portrole register. This Portrole register setting has higher priority over the PORT/DEBUG_N pin state for Source/Sink/DRP port role.

The FUSB303 will set INT_N/OUT3 = LOW in GPIO mode when an Audio Accessory is detected. The FUSB303 will report Audio Accessory detection via the Type I²C register as well when Audio Accessory detection is configured via the Portrole register.

FORCE.SNK and FORCE.SRC Functionality

In some cases, a device may need to force its role to a Sink or a Source especially if two DRP devices are connected together and they have connected in the wrong device role. In that case, the FUSB303 has incorporated a function that allows it to be forced into either Sink or Source. However, if it cannot complete this role change, the FUSB303 will resume its previous role and flag success or failure with I_FRC_SUCC and I_FRC_FAIL interrupts respectively.

Remedial Actions

In some cases, a device may start to detect a Source or Sink but get caught in a loop trying to resolve the detected device. In that case the FUSB303 provides functionality to resolve

FUSB303

to a stable attached state. This functionality can be turned on and off via the REMEDY_EN and DCABLE_EN bits. Multiple cases are tried and some of the register settings will be changed to try to achieve stable attach. The I_REMEDY interrupt will allow the processor to know that this functionality has been triggered.

AUTOSNK Mode

When the FUSB303 is powered directly from VBAT the AUTO_SNK_EN mode can be used to prevent the application from attaching as a Source when the battery is weak or disconnect and attach as a Sink. With AUTO_SNK_EN enabled the port will attempt to configure

as a Sink when attached to another DRP. If connected to another Sink, the port will detach. The threshold at which AUTOSNK can be triggered can be programmed via the AUTO_SNK_TH bits. The I_AUTOSNK interrupt is triggered whenever this functionality is invoked.

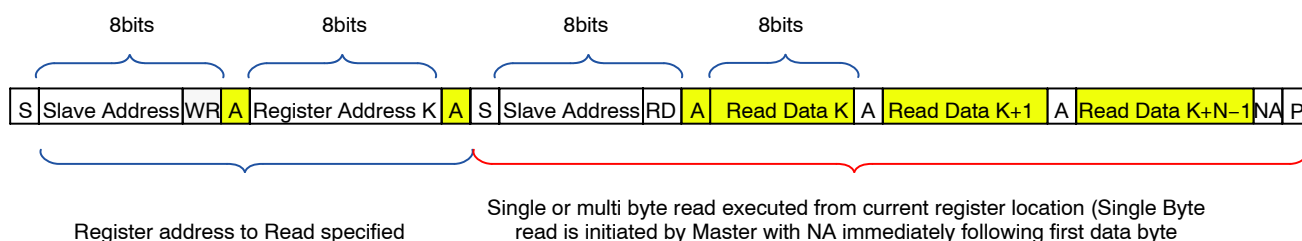
Power Up, Initialization and Reset, Interrupt Operation, I²C Interface

The FUSB303 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 6 requirements. This block is designed for fast mode. Examples of an I²C write and read sequence are shown Figure 5 and Figure 6 respectively.



NOTE: Single byte write is initiated by Master with P immediately following the first data byte and slave A

Figure 5. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed



| | | | | | | | |
|---|----------------------|----------|-----------------------|-----------|----------------------------|-----------|----------------|
|  | From Master to Slave | S | Start Condition | NA | NOT Acknowledge (SDA high) | RD | Read = 1 |
|  | From Slave to Master | A | Acknowledge (SDA Low) | WR | Write=0 | P | Stop Condition |

Figure 6. I²C Write Example

When power is first applied, the FUSB303 will power up in the configuration set by the PORT/DEBUG_N input with Audio Accessory Support enabled and all interrupts masked. If the ADDR/ORIENT input is HIGH or LOW (I²C mode) the local processor can then re-configure the FUSB303 to the desired mode and clear the global interrupt mask bit, INT_MASK using the I²C interface. The INT_N/OUT3 pin is an active LOW, open drain output. This pin indicates to the host processor that an interrupt has occurred in the FUSB303 which needs attention. The INT_N/OUT3 pin is in a high impedance state by default after power-up or device reset, and the global interrupt mask (INT_MASK in Control register) is set. After INT_MASK bit is cleared by the local processor, the INT_N/OUT3 pin stays high impedance in preparation of future interrupts.

When an interruptible event occurs, INT_N/OUT3 is driven LOW and is in a high impedance state again when the processor clears the interrupt by writing a one in the position of the interrupt bit that was set. Subsequent to the initial power up or reset; if the processor writes a "1" to global interrupt mask bit when the system is already powered up, the INT_N/OUT3 pin stays in a high impedance state and ignores all interrupts until the global interrupt mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the global interrupt mask bit is set, the INT_N/OUT3 pin goes LOW when the global interrupt mask is cleared.

Interrupt bits hold their value and to clear a specific interrupt, a "1" needs to be written to that interrupt bit.

FUSB303

I²C Address

The ADDR/ORIENT bit HIGH or LOW is indicated in bit 5 of the slave address shown in Table 4.

Table 4. FUSB303 I²C SLAVE ADDRESS

| Name | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------|-------|-------|-------------------|-------|-------|-------|-------|-------|
| Slave Address | 8 | 0 | 1 | ADDR/ORIENT state | 0 | 0 | 0 | 1 | R/W |

Table 5. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|----------------------|--|--|---------|------|------|
| V _{DD} | Supply Voltage from V _{DD} | | -0.5 | 6.0 | V |
| V _{CON} | ID, VBUS_DET, CC1 and CC2 voltage | | -0.5 | 28.0 | V |
| V _{IO} | PORT/DEBUG_N, ADDR/ORIENT, INT_N/OUT3, SDA/OUT1, SCL/OUT2 pins voltage | | -0.5 | 6.0 | V |
| V _{IO} | EN_N | | -0.5 | 2.0 | V |
| T _{STORAGE} | Storage Temperature Range | | -65 | +150 | C |
| T _J | Maximum Junction Temperature | | | +150 | C |
| T _L | Lead Temperature (Soldering, 10 seconds) | | | +260 | C |
| ESD | IEC 61000-4-2 System ESD with external TVS | Connector Pins (VBUS, CC1 & CC2) | Air Gap | 15 | kV |
| | | | Contact | 8 | |
| | Human Body Model, JEDEC JESD22-A114 | Connector Pins (VBUS_DET, CC1 and CC2) | | 4 | kV |
| | | Others | | 2 | |
| | Charged Device Model, JEDEC LECD22-C101 | All Pins | 1 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 6. RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|-----------------------|------|-----|-----|------|
| V _{BUS} | VBUS_DET Voltage | 4.0 | 5.0 | 22 | V |
| V _{DD} | Supply Voltage | 2.85 | 3.3 | 5.5 | V |
| T _A | Operating Temperature | -40 | | +85 | C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

FUSB303

Table 7. DC AND TRANSIENT CHARACTERISTICS (Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.3\text{ V}$ unless otherwise specified.)

| Symbol | Parameter | $T_A = -40\text{ to }+85^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$ | | | Unit |
|-----------------------------------|--|---|------------|------|------------------|
| | | Min | Typ | Max | |
| TYPE C SPECIFIC PARAMETERS | | | | | |
| I_{80_CCX} | Source 80 μA CC Current (Default) HOST_CUR1 = 0, HOST_CUR0 = 1 or via GPIO mode | 64 | 80 | 96 | μA |
| I_{180_CCX} | Source 180 μA CC Current (1.5 A) HOST_CUR1 = 1, HOST_CUR0 = 0 or via GPIO mode | 166 | 180 | 194 | μA |
| I_{330_CCX} | Source 330 μA CC Current (3 A) HOST_CUR1 = 1, HOST_CUR0 = 1 or via GPIO mode (Note 3) | 304 | 330 | 356 | μA |
| V_{SNKDB} | Sink Pull-Down Voltage in Dead Battery Under all Pull-up Source Loads | | | 2.18 | V |
| R_d | Sink Pull-Down Resistance when VDD is within Operating Range | 4.6 | 5.1 | 5.6 | $\text{k}\Omega$ |
| z_{OPEN} | CC Resistance for Disabled State | 126 | | | $\text{k}\Omega$ |
| $v_{Ra-SRCdef}$ | Ra Detection Threshold for CC Pin for Source for Default Current on VBUS (HOST_CUR1/0 = 01) or via GPIO mode | 0.15 | 0.20 | 0.25 | V |
| $v_{Ra-SRC1.5A}$ | Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS (HOST_CUR1/0 = 10) or via GPIO mode | 0.35 | 0.40 | 0.45 | V |
| $v_{Ra-SRC3A}$ | Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS (HOST_CUR1/0 = 11) or via GPIO mode | 0.75 | 0.80 | 0.85 | V |
| $v_{Rd-SRCdef}$ | Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01) or via GPIO mode | 1.50 | 1.60 | 1.65 | V |
| $v_{Rd-SRC1.5A}$ | Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10) or via GPIO mode | 1.50 | 1.60 | 1.65 | V |
| $v_{Rd-SRC3A}$ | Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11) or via GPIO mode (Note 3) | 2.45 | 2.60 | 2.75 | V |
| v_{Ra-SNK} | Ra Detection Threshold for CC Pin for Sink | 0.15 | 0.20 | 0.25 | V |
| v_{Rd-def} | Rd Default Current Detection Threshold for Sink | 0.61 | 0.66 | 0.70 | V |
| $v_{Rd-1.5A}$ | Rd 1.5 A Current Detection Threshold for Sink | 1.16 | 1.23 | 1.31 | V |
| $v_{Rd-3.0A}$ | Rd 3 A Current Detection Threshold for Sink | 2.04 | 2.11 | 2.18 | V |
| $v_{VBUSthr}$ | VBUS_DET Threshold when VBUSOK is deasserted | 2.9 | 3.3 | 3.67 | V |
| $t_{VBUSdeb}$ | VBUS_DET debounce time before VBUSOK is deasserted only (see t_{Deb} below for VBUSOK being asserted) | 10 | | 20 | ms |
| v_{VBthLH} | VBUS_DET Threshold when VBUSOK is asserted | 3.67 | 4.07 | 4.48 | V |
| t_{Deb} | VBUS_DET debounce time before VBUSOK is asserted | 250 | | 500 | μs |
| $v_{VSAFEthr}$ | vSafe0V VBUS_DET Threshold | | | 0.8 | V |
| $v_{VSAFEthrHys}$ | VSAFE0V VBUS_DET Threshold hysteresis | | 50 | | mV |
| $r_{VBUSleak}$ | Leakage between VBUS and GND when VBUS not sourced | 72.4 | | | $\text{k}\Omega$ |
| $r_{VBUSdschg}$ | Effective resistance from VBUS and GND when VBUS is being discharged from vSafe5V $V_{DD} (V) = 2.85\text{ to }5.5$ | | | 2 | $\text{k}\Omega$ |
| r_{Pullup} | Pull up resistor to VDD value on EN_N pin $V_{DD} (V) = 2.85\text{ to }5.5$ | | 6 | | $\text{M}\Omega$ |
| $v_{AUTOSNKthr}$ | Weak Battery VDD Threshold | -3% | AUTOSNK_TH | +3% | V |
| R_a | Resistor for discharging VCONN $V_{DD} (V) = 2.85\text{ to }5.5$ | | 1 | | $\text{k}\Omega$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. $V_{DD} = 3\text{ V}$ when 3 A current advertised.

FUSB303

Table 8. CURRENT CONSUMPTION

| Symbol | Parameter | VDD (V) | Conditions | TA = -40 to +85°C TJ = -40 to +125°C | | | Unit |
|----------------------|--|--------------|---|---|-----|-----|------|
| | | | | Min | Typ | Max | |
| I _{disable} | Disabled Current | 2.85 to 4.35 | Disabled State EN N = HIGH or not connected | | | 5 | μA |
| I _{stby} | Unattached Sink (3.3 V I ² C mode without AUTOSNK or accessories) | 2.85 to 4.35 | Nothing attached | | 5 | 10 | μA |
| | Unattached DRP or Source (3.3 V I ² C mode without AUTOSNK or accessories) | | Nothing attached, Internally Toggling | | 10 | 15 | μA |
| I _{attach} | Attached Source or Sink (3.3 V I ² C mode without AUTOSNK or accessories. Not including I _{xxx_CCX} current) | 2.85 to 4.35 | Attached as a Sink or Source | | 10 | 15 | μA |

Table 9. TIMING PARAMETERS

| Symbol | Parameter | TA = -40 to +85°C TJ = -40 to +125°C | | | Unit |
|----------------------------|--|---|--------|------|------|
| | | Min | Typ | Max | |
| t _{CCDebounce} | Debounce Time for CC Attach Detection (TCCDEB[2:0] = 011) | -33% | TCCDEB | +33% | ms |
| t _{PDebounce} | Time a Sink port shall wait before it can determine it is detached | 10 | 15 | 20 | ms |
| t _{TryCCDebounce} | Time a port shall wait before it can determine it is re-attached during the try-wait process | 10 | | 20 | ms |
| t _{RpValueChange} | Time a Sink port shall wait before it can determine there has been a change in R _p | 10 | | 20 | ms |
| t _{SRCDisconnect} | Time a Source shall detect the SRC.Open state | 10 | | 20 | ms |
| t _{ErrorRecovery} | Time staying in the ErrorRecovery State if sent there via the ERROR_REC bit or by a change of port roles | 25 | 50 | 100 | ms |
| t _{DRPTry} | Time staying in the Try.SRC/SNK prior to transition to TryWait.SRC/SNK State | 75 | | 150 | ms |
| t _{TryTimeout} | Time to discharge VBUS before giving up for cases where VBUS is always on. | 550 | | 1100 | ms |
| t _{DRP} | Sum of t _{DRPTogSNK} and t _{DRPTogSRC} | -33% | T_DRP | +33% | ms |
| t _{DRPTransition} | Time DRP shall complete transitions between Source and Sink roles | 0 | | 1 | ms |
| t _{DRPTogSNK} | For DRP Operation, Time Spent in Unattached.SNK before going to Unattached.SRC State | DRPTOGGLE = 00 (Note 4) | 70 | | % |
| | | DRPTOGGLE = 01 | 60 | | % |
| | | DRPTOGGLE = 10 | 50 | | % |
| | | DRPTOGGLE = 11 | 40 | | % |
| t _{DRPTogSRC} | For DRP Operation, Time Spent in Unattached.SRC before going to Unattached.SNK State | DRPTOGGLE = 00 (Note 4) | 30 | | % |
| | | DRPTOGGLE = 01 | 40 | | % |
| | | DRPTOGGLE = 10 | 50 | | % |
| | | DRPTOGGLE = 11 | 60 | | % |
| t _{EN} | Time from EN_N LOW and VDD active to I ² C access available | 2.85 to 5.5 | | 100 | ms |

FUSB303

Table 9. TIMING PARAMETERS (continued)

| Symbol | Parameter | | T _A = -40 to +85°C T _J = -40 to +125°C | | | Unit |
|----------|--|-------------|---|-----|-----|------|
| | | | Min | Typ | Max | Unit |
| tRESET | Soft Reset Duration | 2.85 to 5.5 | | | 100 | ms |
| tAUTOSNK | Debounce time to detect Weak Battery VDD Threshold to trigger I_AUTOSNK if AUTOSNK mode enabled for both entering AUTOSNK and exiting AUTOSNK V _{DD} (V) = 2.85 to 5.5 | | 10 | 15 | 20 | ms |

4. Default Value when Configured in GPIO Mode (ADDR/ORIENT = Float)

Table 10. IO SPECIFICATIONS

| Symbol | Parameter | V _{DD} (V) | Conditions | T _A = -40 to +85°C T _J = -40 to +125°C | | | Unit |
|--------|-----------|---------------------|------------|---|-----|-----|------|
| | | | | Min | Typ | Max | |

OPEN DRAIN OUTPUT PINS (ID, INT_N/OUT3)

| | | | | | | | |
|-------------------|--------------------|-------------|------------------------|--|--|-----|---|
| V _{OLID} | Output Low Voltage | 2.85 to 5.5 | I _{OL} = 4 mA | | | 0.4 | V |
|-------------------|--------------------|-------------|------------------------|--|--|-----|---|

INPUT PIN (EN_N)

| | | | | | | | |
|--------------------|-------------------------------|-------------|---------------------|-----|--|-----|----|
| V _{IEN} | Low-Level Input Voltage | 2.85 to 5.5 | | | | 0.4 | V |
| V _{IHEN} | High-Level Input Voltage | 2.85 to 5.5 | | 1.2 | | | V |
| I _{CCTEN} | VDD Current when EN_N is HIGH | 2.85 to 5.5 | Worst Input Voltage | | | 2 | μA |

3-STATE INPUT AND PUSH/PULL OUTPUT PINS (PORT/DEBUG_N, ADDR/ORIENT)

| | | | | | | | |
|---------------------|--|-------------|-------------------------|--------------------|--|--------------------|----|
| V _{ILADDR} | Low-Level Input Voltage | 2.85 to 5.5 | | | | 0.2V _{DD} | V |
| V _{IMADDR} | Middle-Level Input Voltage | 2.85 to 5.5 | | 0.4V _{DD} | | 0.6V _{DD} | V |
| V _{IHADDR} | High-Level Input Voltage | 2.85 to 5.5 | | 0.8V _{DD} | | | V |
| Z _{float} | Impedance to VDD or GND detected as a FLOAT including when VDD = 0 | 2.85 to 5.5 | | 1 | | 4 | MΩ |
| V _{OLOUT} | Low-Level Input Voltage | 2.85 to 5.5 | I _{OL} = 1 mA | | | 0.2V _{DD} | V |
| V _{OHO} | High-Level Input Voltage | 2.85 to 5.5 | I _{OL} = -1 mA | 0.8V _{DD} | | | V |

I²C INTERFACE PINS – FAST MODE SDA/OUT1, SCL/OUT2

| | | | | | | | |
|---------------------|--|-------------|----------------------------|-----|---|-----|----|
| V _{ILI2C} | Low-Level Input Voltage | 2.85 to 5.5 | | | | 0.4 | V |
| V _{IHI2C} | High-Level Input Voltage | 2.85 to 5.5 | | 1.2 | | | V |
| V _{HYS} | Hysteresis of Schmitt Trigger Inputs | 2.85 to 5.5 | | 0.2 | | | V |
| I _{i2C} | Input Current of SDA/OUT1 and SCL/OUT2 Pins, | 2.85 to 5.5 | Input Voltage 0 V to 3.6 V | | | 2 | μA |
| I _{CCTI2C} | VDD Current when SDA/OUT1 or SCL/OUT2 is HIGH | 2.85 to 5.5 | Worst Input Voltage | | | 2 | μA |
| V _{OLSDA} | Low-Level Output Voltage at 2 mA Sink Current (Open-Drain) | 2.85 to 5.5 | I _{OL} = 2 mA | | | 0.3 | V |
| I _{OLSDA} | Low-Level Output Current (Open-Drain) | 3.0 to 5.5 | V _{OLSDA} = 0.4 V | 20 | | | mA |
| C _I | Capacitance for Each I/O Pin | 2.85 to 5.5 | | | 5 | | pF |

Table 11. FAST MODE I²C TIMING SPECIFICATIONS (see Figure 7)

| Symbol | Parameter | Fast Mode | | |
|---------------------|---|-----------------------------|-----|------|
| | | Min | Max | Unit |
| f _{SCL} | SCL/OUT2 Clock Frequency | | 400 | kHz |
| t _{HD;STA} | Hold Time (Repeated) START Condition | 0.6 | | μs |
| t _{LOW} | Low Period of SCL/OUT2 Clock | 1.3 | | μs |
| t _{HIGH} | High Period of SCL/OUT2 Clock | 0.6 | | μs |
| t _{SU;STA} | Set-up Time for Repeated START Condition | 0.6 | | μs |
| t _{HD;DAT} | Data Hold Time | | 0.9 | μs |
| t _{SU;DAT} | Data Set-up Time (Note 5) | 100 | | ns |
| t _r | Rise Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6) | 20×(V _{DD} /5.5 V) | 250 | ns |
| t _f | Fall Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6) | 20×(V _{DD} /5.5 V) | 250 | ns |
| t _{SU;STO} | Set-up Time for STOP Condition | 0.6 | | μs |
| t _{BUF} | Bus-Free Time between STOP and START Conditions | 1.3 | | μs |
| t _{SP} | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | | 50 | ns |

5. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL/OUT2 signal. If such a device does stretch the LOW period of the SCL/OUT2 signal, it must output the next data bit to the I²C_line t_{r_max} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL/OUT2 line is released.
6. C_b equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

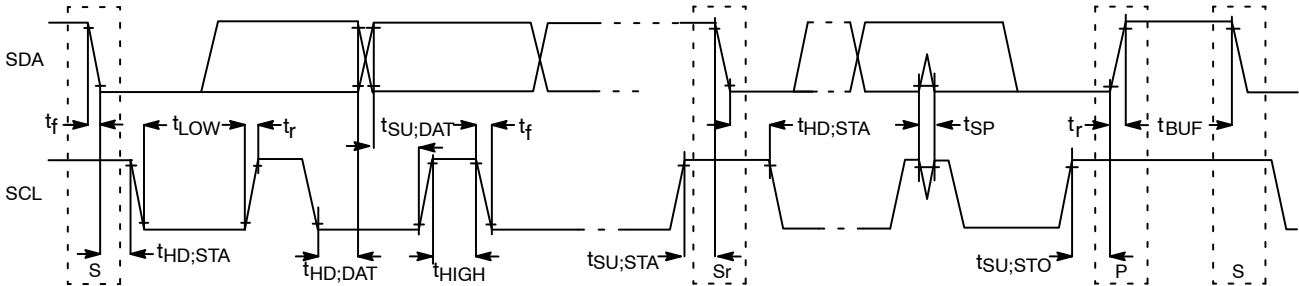


Figure 7. Definition of Timing for Full/Speed Mode Devices on the I²C Bus

FUSB303

REGISTER DEFINITIONS

Table 12. REGISTER MAP

| Address | Register Name | Type | Rst Val | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|---------------|-----------|-----------------|------------------|------------------|----------------|-------------|-------------|---------------|------------|-----------|
| 00h | Reserved | N/A | N/A | Do Not Use | | | | | | | |
| 01h | Device ID | R | 10h | VER_ID[3:0] | | | | REV_ID[3:0] | | | |
| 02h | Device Type | R | 01h | DEVICE_TYPE[7:0] | | | | | | | |
| 03h | Portrole | R/W | 4nh (see below) | | ORIENTDE B | TRY[1:0] | | AUDIOACC | DRP | SNK | SRC |
| 04h | Control | R/W | 4Bh | T_DRP | | DRPTOGGLE[1:0] | | DCABLE_EN | HOST_CUR[1:0] | | INT_MASK |
| 05h | Control1 | R/W | B3h | REMEDY_EN | AUTO_SNK_TH[1:0] | | AUTO_SNK_EN | ENABLE | TCCDEB[2:0] | | |
| 06h-08h | Reserved | N/A | N/A | Do Not Use | | | | | | | |
| 09h | Manual | W/C & R/W | 00h | | | FORCE_S RC | FORCE_S NK | UNATT_S NK | UNATT_S RC | DISABLED | ERROR_REC |
| 0Ah | Reset | W/C | 00h | | | | | | | | SW_RES |
| 0Bh-0Dh | Reserved | N/A | N/A | Do Not Use | | | | | | | |
| 0Eh | Mask | R/W | 00h | | M_ORIENT | M_FAULT | M_VBUS_CHG | M_AUTO_SNK | M_BC_LVL | M_DETACH | M_ATTACH |
| 0Fh | Mask1 | R/W | 00h | | M_REM_VBOFF | M_REM_VBON | | M_REM_FAIL | M_FRC_FAIL | M_FRC_SUCC | M_REMEDY |
| 10h | Reserved | N/A | N/A | Do Not Use | | | | | | | |
| 11h | Status | R | 40h | AUTOSNK | VSAFE0V | ORIENT[1:0] | | VBUSOK | BC_LVL[1:0] | | ATTACH |
| 12h | Status1 | R | 00h | | | | | | | FAULT | REMEDY |
| 13h | Type | R | 00h | | DEBUGSRC | DEBUGSNK | SINK | SOURCE | ACTIVECAPABLE | AUDIOVBUS | AUDIO |
| 14h | Interrupt | R/W1C | 00h | | I_ORIENT | I_FAULT | I_VBUS_CHG | I_AUTOSNK | I_BC_LVL | I_DETACH | I_ATTACH |
| 15h | Interrupt1 | R/W1C | 00h | | I_REM_VBOFF | I_REM_VBON | | I_REM_FAIL | I_FRC_FAIL | I_FRC_SUCC | I_REMEDY |
| 16h-1Fh | Reserved | N/A | N/A | Do Not Use | | | | | | | |

7. Do not use registers that are blank

8. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers

Table 13. DEVICE ID (Address: 01h, Reset Value: 0001_0000b, Type: Read Only)

| Bit # | Name | Size (Bits) | Description |
|-------|--------|-------------|---|
| 7:4 | VER_ID | 4 | Device version ID by Trim, etc. A_[REV_ID]: 0001 (FUSB303 A) |
| 3:0 | REV_ID | 4 | Revision History of each version [VER_ID]_revA: 0000 |

Table 14. DEVICE TYPE (Address: 02h, Type: Read Only)

| Bit # | Name | Size (Bits) | Description |
|-------|------------------|-------------|--------------|
| 7:0 | DEVICE_TYPE[7:0] | 8 | 01h: FUSB303 |

FUSB303

Table 15. PORTROLE (See Note 9)

(Address: 03h, Reset Value: 0100_1nnb (Reset value for bits nnn will be set by the state of the PORT/DEBUG_N pin either during power up when EN_N is LOW or when Vdd is valid and EN_N goes HIGH to LOW) or when SW_RES is set HIGH. In dead battery mode, nnn = 010 or configured as SNK) Type: Read/Write)

| Bit # | Name | Size (Bits) | Description |
|-------|-----------|-------------|--|
| 7 | Reserved | 1 | Do Not Use |
| 6 | ORIENTDEB | 1 | 1: When a Debug Accessory is found, continue to orientation detection if CC is on CC1 or CC2 (result is in Status.Orient[1:0]) |
| 5:4 | TRY[1:0] | 2 | 00: Disable (normal DRP detection for DRPs) 01: Enable Try.SNK state machine detection for DRP only 10: Enable Try.SRC state machine detection for DRP only 11: Disable (cannot have Try.SNK and Try.SRC active together) |
| 3 | AUDIOACC | 1 | 1: Enable Audio Accessory Support (Debug Accessory support is always enabled) |
| 2 | DRP | 1 | 1: Configure device as a Dual Role Port (see reset value text above) |
| 1 | SNK | 1 | 1: Configure device as a Sink (see reset value text above) |
| 0 | SRC | 1 | 1: Configure device as a Source (see reset value text above) |

9. If DRP bit, SNK bit and SRC bit are all set to 1, then the priority of which Portrole the FUSB303 assumes is first priority is DRP, second priority is SNK and last priority is SRC. See Manual register note below for priority between Manual register bits and Portrole register.

Table 16. CONTROL

Address: 04h, Reset Value: 0100_1011b, Type: Read/Write

| Bit # | Name | Size (Bits) | Description |
|-------|----------------|-------------|---|
| 7:6 | T_DRP[:0] | 2 | Sets the total period of the DRP toggle cycle (i.e. Unattached.SNK period + Unattached.SRC period): 00: 60 ms 01: 70 ms 10: 80 ms 11: 90 ms |
| 5:4 | DRPTOGGLE[1:0] | 2 | Selects different timing for Dual Role Port Toggle between Unattached.SNK State and Unattached.SRC State. 00: 60% in Unattached.SNK and 40% in Unattached.SRC 01: 50% in Unattached.SNK and 50% in Unattached.SRC 10: 40% in Unattached.SNK and 60% in Unattached.SRC 11: 30% in Unattached.SNK and 70% in Unattached.SRC |
| 3 | DCABLE_EN | 1 | 1: Enable Dangling Cable internal methods to achieve a stable attach |
| 2:1 | HOST_CUR[1:0] | 2 | Controls the pull-up current when device enabled as a Source 00: Reserved. Do not use. 01: 80 μ A – Default USB Power 10: 180 μ A – Medium Current Mode: 1.5 A 11: 330 μ A – High Current Mode: 3 A |
| 0 | INT_MASK | 1 | 1: Global interrupt mask to mask all interrupts |

FUSB303

Table 17. CONTROL1

(Address: 05h, Reset Value: 1011_0011b, Type: Read/Write)

| Bit # | Name | Size (Bits) | Description |
|-------|----------------------|-------------|---|
| 7 | REMEDY_EN | 1 | 1: Enable the Remedy detection to employ internal methods to achieve stable attach |
| 6:5 | AUTO_SNK_TH [1:0] | 2 | Sets the weak battery VDD threshold voltage when AUTO_SNK_EN is enabled. 00: 3.0 V 01: 3.1 V 10: 3.2 V 11: 3.3 V |
| 4 | AUTO_SNK_EN | 1 | 1: Enable automatic Sink port role based on weak battery VDD threshold in bits AUTO_SNK_TH in Control register below |
| 3 | ENABLE | 1 | 1: Enable the FUSB303 if the external EN_N pin is LOW in I ² C mode (that is, not in GPIO mode) |
| 2:0 | TCCDEB[2:0] | 3 | Controls debounce time for attaching a device 000: 120 ms 001: 130 ms 010: 140 ms 011: 150 ms 100: 160 ms 101: 170 ms 110: 180 ms 111: Reserved |

Table 18. Manual (Note 10)

(Address: 09h, Reset Value: 0000_0000b, Type: Read/Write (see bits below: W/C = Write one self clearing, R/W = Read/Write and N/A = Not Applicable)

| Bit # | Name | R/W/C | Size (Bits) | Description |
|-------|-----------------------|-------|-------------|---|
| 7:6 | Reserved | N/A | 2 | Do Not Use |
| 5 | FORCE_SRC | W/C | 1 | 1: Forces the FUSB303 to behave as a Source |
| 4 | FORCE_SNK | W/C | 1 | 1: Forces the FUSB303 to behave as a Sink |
| 3 | UNATT_SNK | W/C | 1 | 1: Put device in Unattached.SNK State as defined in the Type C spec |
| 2 | UNATT_SRC | W/C | 1 | 1: Put device in Unattached.SRC state as defined in the Type C spec |
| 1 | DISABLED (Note 11) | R/W | 1 | 1: Put device in Disabled state as defined in the Type C spec |
| 0 | ERROR_REC | W/C | 1 | 1: Put device in ErrorRecovery state as defined in the Type C spec |

10. If more than one bit is set to 1b simultaneously then an order of priority will be used. First priority is DISABLED, second is ERROR_REC, third is FORCE_SRC, fourth is FORCE_SNK, fifth is UNATT_SRC, last is UNATT_SNK. The highest priority bit will take precedence and all other bits will be cleared automatically.

11. The DISABLED bit must be manually cleared. Also DISABLED bit has a higher priority over Portrole register since the DISABLED bit has to be cleared in order to execute the new Portrole register settings. However, all other Manual register bits don't have a lot of meaning if the Portrole register is changed and so Portrole register setting should have higher priority than all bits except for DISABLED bit.

Table 19. RESET

(Address: 0Ah, Reset Value: 0000_0000b, Type: Write/Clear)

| Bit # | Name | Size (Bits) | Description |
|-------|----------|-------------|---|
| 7:1 | Reserved | 7 | Do Not Use |
| 0 | SW_RES | 1 | 1: Reset the FUSB303 and I ² C Registers |

FUSB303

Table 20. MASK

(Address: 0Eh, Reset Value: 0000_0000b, Type: Read/Write)

| Bit # | Name | Size (Bits) | Description |
|-------|------------|-------------|--|
| 7 | Reserved | 1 | Do Not Use |
| 6 | M_ORIENT | 1 | 1: Mask the I_ORIENT interrupt bit from asserting INT_N pin |
| 5 | M_FAULT | 1 | 1: Mask the I_FAULT interrupt bit from asserting INT_N pin |
| 4 | M_VBUS_CHG | 1 | 1: Mask the I_VBUS interrupt bit from asserting INT_N pin |
| 3 | M_AUTOSNK | 1 | 1: Mask the I_AUTOSNK interrupt bit from asserting INT_N pin |
| 2 | M_BC_LVL | 1 | 1: Mask the I_BC_LVL interrupt bit from asserting INT_N pin |
| 1 | M_DETACH | 1 | 1: Mask the I_DETACH interrupt bit from asserting INT_N pin |
| 0 | M_ATTACH | 1 | 1: Mask the I_ATTACH interrupt bit from asserting INT_N pin |

12. Masking the interrupt just does not cause INT_N to be asserted. The interrupt bit will still be asserted in the Interrupt register and so that an all zeroes Interrupt register value is not needed for INT_N to be deasserted.

Table 21. MASK1

(Address: 0Fh, Reset Value: 0000_0000b, Type: Read/Write)

| Bit # | Name | Size (Bits) | Description |
|-------|-------------|-------------|--|
| 7 | Reserved | 1 | Do Not Use |
| 6 | M_REM_VBOFF | 1 | 1: Mask the I_REM_VBOFF interrupt bit from asserting INT_N pin |
| 5 | M_REM_VBON | 1 | 1: Mask the I_REM_VBON interrupt bit from asserting INT_N pin |
| 4 | Reserved | 1 | Do Not Use |
| 3 | M_REM_FAIL | 1 | 1: Mask the I_REM_FAIL interrupt bit from asserting INT_N pin |
| 2 | M_FRC_FAIL | 1 | 1: Mask the I_FRC_FAIL interrupt bit from asserting INT_N pin |
| 1 | M_FRC_SUCC | 1 | 1: Mask the I_FRC_SUCC interrupt bit from asserting INT_N pin |
| 0 | M_REMEDY | 1 | 1: Mask the I_REMEDY interrupt bit from asserting INT_N pin |

13. Masking the interrupt just does not cause INT_N to be asserted. The interrupt bit will still be asserted in the Interrupt register and so that an all zeroes Interrupt register value is not needed for INT_N to be deasserted.

Table 22. STATUS

(Address: 11h, Reset Value: 0000_0000b, Type: Read Only)

| Bit # | Name | Size (Bits) | Description |
|-------|-------------|-------------|--|
| 7 | AUTOSNK | 1 | 1: AUTOSNK mode is activated since the VDD voltage is lower than AUTO_SNK_TH voltage |
| 6 | VSAFE0V | 1 | 1: Status to indicate VBUS_DET is below vSafe0V max of 0.8 Vpin |
| 5:4 | ORIENT[1:0] | 2 | Status to indicate which CCx pins has the cable CC connection 00: No or unresolved connection detected 01: Cable CC is connected through the CC1 (A5) pin 10: Cable CC is connected through the CC2 (B5) pin 11: A fault has occurred during the detection |
| 3 | VBUSOK | 1 | 1: Status to indicate VBUS_DET is in the valid VBUS 5V range |
| 2:1 | BC_LVL[1:0] | 2 | Thresholds that allow detection of current advertisement on CC line 00: (Ra or unattached) Sink or unattached Source 01: Rd threshold for Sink default current advertisement 10: Rd threshold for Sink 1.5 A current advertisement 11: Rd threshold for Sink 3 A current advertisement |
| 0 | ATTACH | 1 | 1: Attached to a device or accessory of a type shown in the Type register |

FUSB303

Table 23. STATUS1

(Address: 12h, Reset Value: 0000_0000b, Type: Read Only)

| Bit # | Name | Size (Bits) | Description |
|-------|----------|-------------|---|
| 7:2 | Reserved | 6 | Do Not Use |
| 1 | FAULT | 1 | 1: Status to indicate that as a Sink, CC has exceed the normal vRd voltage range |
| 0 | REMEDY | 1 | 1: Status to indicate that FUSB303 is employing internal methods to achieve a stable attach |

Table 24. TYPE

(Address: 13h, Reset Value: 0000_0000b, Type: Read Only)

| Bit # | Name | Size (Bits) | Description |
|-------|-------------|-------------|--|
| 7 | Reserved | 1 | Do Not Use |
| 6 | DEBUGSRC | 1 | 1: FUSB303 is attached as a Source Debug Accessory ([Unoriented/Oriented]DebugAccessory.SRC) |
| 5 | DEBUGSNK | 1 | 1: FUSB303 is attached as a Sink Debug Accessory (DebugAccessory.SNK) |
| 4 | SINK | 1 | 1: FUSB303 is attached as a Sink (Attached.SNK) |
| 3 | SOURCE | 1 | 1: FUSB303 is attached as a Source (Attached.SRC) |
| 2 | ACTIVECABLE | 1 | 1: FUSB303 is attached to an Active Cable (Ra detected) |
| 1 | AUDIOVBUS | 1 | 1: Indicates an Audio Accessory with VBUS has been detected (AudioAccessory with VBUS) |
| 0 | AUDIO | 1 | 1: Indicates an Audio Accessory without VBUS has been detected (AudioAccessory without VBUS) |

Table 25. INTERRUPT

(Address: 14h, Reset Value: 0000_0000b, Type: Read/Write 1 to Clear)

| Bit # | Name | Size (Bits) | Description |
|-------|------------|-------------|--|
| 7 | Reserved | 1 | Do Not Use |
| 6 | I_ORIENT | 1 | 1: Interrupt flagged whenever ORIENT changes from 0,0 to 0,1 or 1,0 but not 1,1. Interrupt not flagged when ORIENT is cleared. |
| 5 | I_FAULT | 1 | 1: Interrupt flagged when CC1 or CC2 voltage exceeds normal Rd range when FUSB303 has Rd termination on CC1 and/or CC2 |
| 4 | I_VBUS_CHG | 1 | 1: Interrupt flagged when VBUS has crossed vVBUSthr or vVBthLH thresholds |
| 3 | I_AUTOSNK | 1 | 1: Interrupt flagged when AUTOSNK mode has been activated or deactivated |
| 2 | I_BC_LVL | 1 | 1: Interrupt flagged when a change in BC_LVL[1:0] advertised current level has occurred |
| 1 | I_DETACH | 1 | 1: Interrupt flagged when a device or accessory has been detached |
| 0 | I_ATTACH | 1 | 1: Interrupt flagged when a device or accessory of type indicated in the Type register has been attached |

FUSB303

Table 26. INTERRUPT1

(Address: 15h, Reset Value: 0000_0000b, Type: Read/Write 1 to Clear)

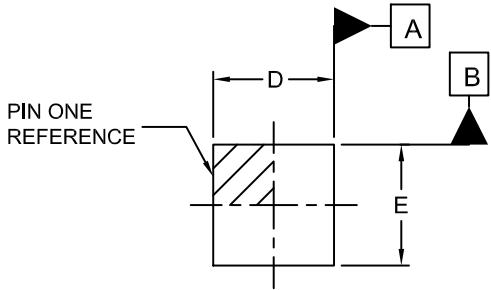
| Bit # | Name | Size (Bits) | Description |
|-------|-------------|-------------|---|
| 7 | Reserved | 1 | Do Not Use |
| 6 | I_REM_VBOFF | 1 | 1: Interrupt to request VBUS be turned off and discharged while executing internal methods to achieve stable attach |
| 5 | I_REM_VBON | 1 | 1: Interrupt to request VBUS be turned on while executing internal methods to achieve stable attach |
| 4 | Reserved | 1 | Do Not Use |
| 3 | I_REM_FAIL | 1 | 1: Interrupt to indicate that internal methods to achieve stable attach have failed. |
| 2 | I_FRC_FAIL | 1 | 1: Interrupt to indicate that FORCE_SRC or FORCE_SNK has failed to execute either because it was being forced into a state it was already in or for other reasons |
| 1 | I_FRC_SUCC | 1 | 1: Interrupt to indicate that FORCE_SRC or FORCE_SNK has successfully being executed. |
| 0 | I_REMEDY | 1 | 1: Interrupt to indicate that detection issues caused FUSB303 to employ internal methods to achieve stable attach |

All brand names and product names appearing in this document are registered trademarks or trademarks of their respective holders.

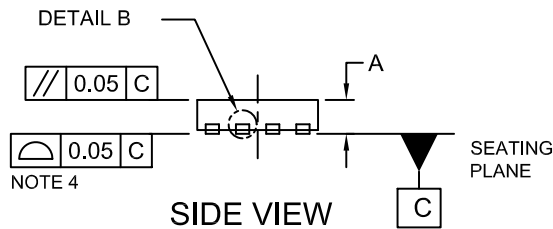


X2QFN12 1.6x1.6, 0.4P
CASE 722AG
ISSUE A

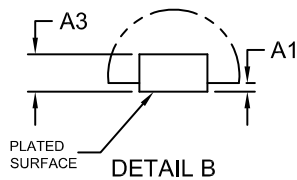
DATE 26 SEP 2017



TOP VIEW



SIDE VIEW

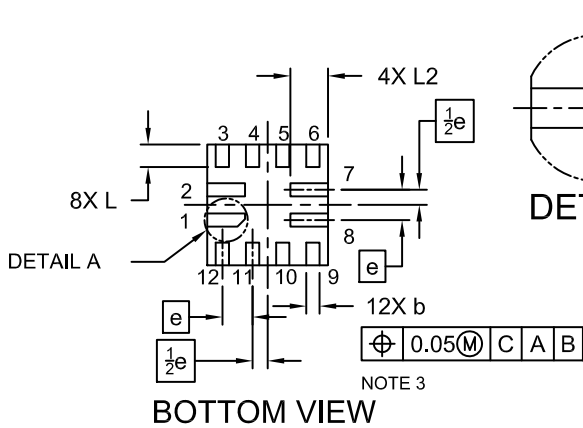


DETAIL B

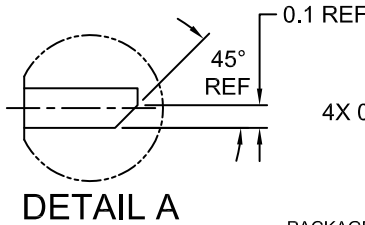
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

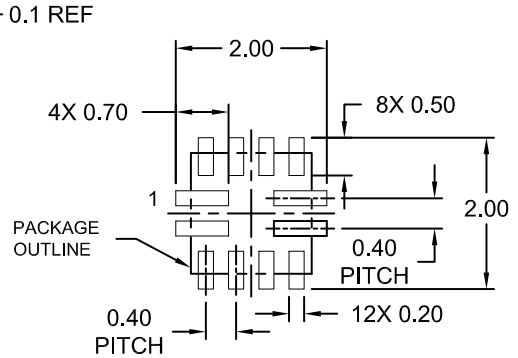
| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| A1 | -- | -- | 0.05 |
| A3 | 0.127 REF | | |
| b | 0.15 | 0.175 | 0.20 |
| D | 1.55 | 1.60 | 1.65 |
| E | 1.55 | 1.60 | 1.65 |
| e | 0.40 BSC | | |
| L | 0.25 | 0.30 | 0.35 |
| L2 | 0.45 | 0.50 | 0.55 |



BOTTOM VIEW



DETAIL A



RECOMMENDED MOUNTING FOOTPRINT

| | | |
|-------------------------|------------------------------|--|
| DOCUMENT NUMBER: | 98AON13772G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | X2QFN12 1.6x1.6, 0.4P | PAGE 1 OF 1 |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

