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MM74HC245A Octal 3-STATE Transceiver

General Description

The MM74HC245A 3-STATE bidirectional buffer utilizes advanced silicon-gate CMOS technology, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device has an active LOW enable input \overline{G} and a direction control input, DIR. When DIR is HIGH, data flows from the A inputs to the B outputs. When DIR is LOW, data flows from the B inputs to the A outputs. The MM74HC245A transfers true data from one bus to the other.

This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

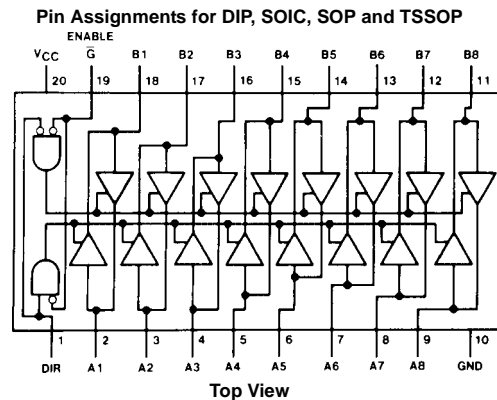
- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μ A maximum (74 HC)
- 3-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)
- Same as the 645

Ordering Code:

Order Number	Package Number	Package Description
MM74HC245AWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC245ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC245AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC245AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

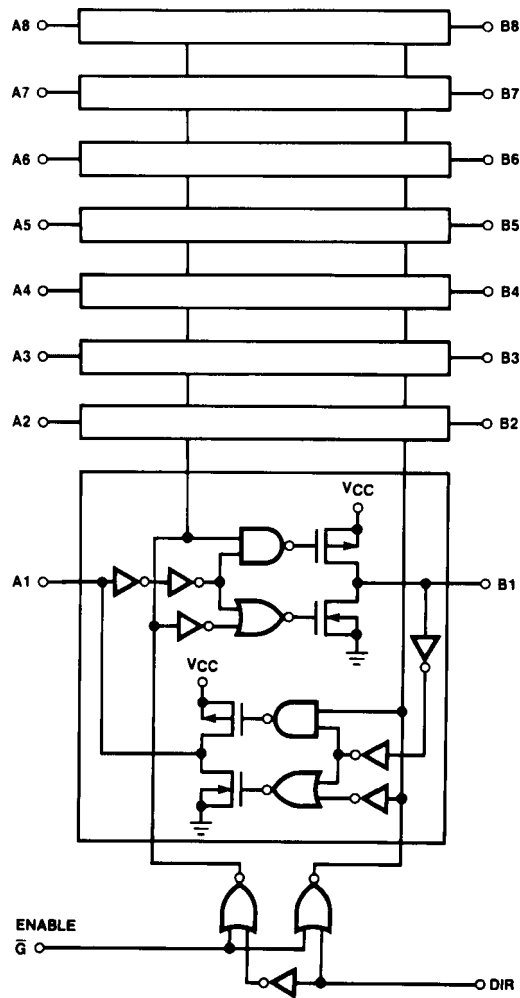


Truth Table

Control Inputs		Operation
\overline{G}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Logic Diagram



AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay	$C_L = 45 pF$	12	17	ns
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	24	35	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 5 pF$	18	25	ns

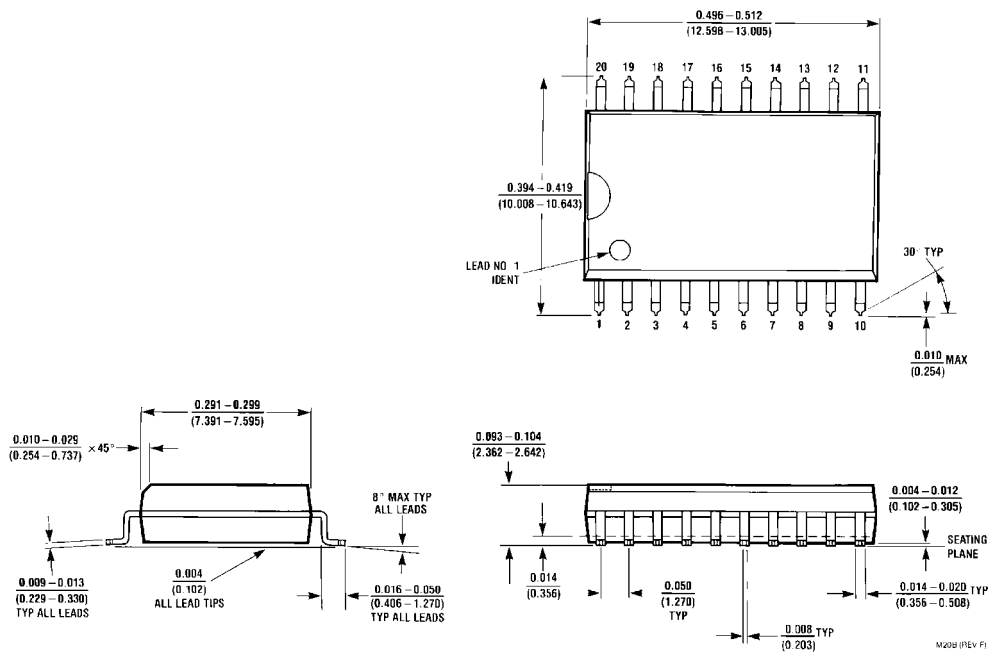
AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50 pF$, $t_r = t_f = 6ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$		$T_A = -55$ to $125^\circ C$		Units				
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits					
t_{PHL} , t_{PLH}	Maximum Propagation Delay	$C_L = 50 pF$	2.0V	31	90	113	135	ns						
		$C_L = 150 pF$	2.0V	41	96	116	128	ns						
		$C_L = 50 pF$	4.5V	13	18	23	27	ns						
		$C_L = 150 pF$	4.5V	17	22	28	33	ns						
		$C_L = 50 pF$	6.0V	11	15	19	23	ns						
		$C_L = 150 pF$	6.0V	14	19	23	28	ns						
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1 k\Omega$	2.0V	71	190	240	285	ns						
		$C_L = 50 pF$												
		$C_L = 150 pF$							2.0V	81	240	300	360	ns
		$C_L = 50 pF$							4.5V	26	38	48	57	ns
		$C_L = 150 pF$							4.5V	31	48	60	72	ns
		$C_L = 50 pF$							6.0V	21	32	41	48	ns
$C_L = 150 pF$	6.0V	25	41	51	61	ns								
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1 k\Omega$	2.0V	39	135	169	203	ns						
		$C_L = 50 pF$	4.5V	20	27	34	41	ns						
			6.0V	18	23	29	34	ns						
t_{TLH} , t_{THL}	Output Rise and Fall Time	$C_L = 50 pF$	2.0V	20	60	75	90	ns						
			4.5V	6	12	15	18	ns						
			6.0V	5	10	13	15	ns						
C_{PD}	Power Dissipation Capacitance (Note 5)	$\bar{G} = V_{IL}$ $\bar{G} = V_{IH}$		50				pF						
				5				pF						
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF						
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF						

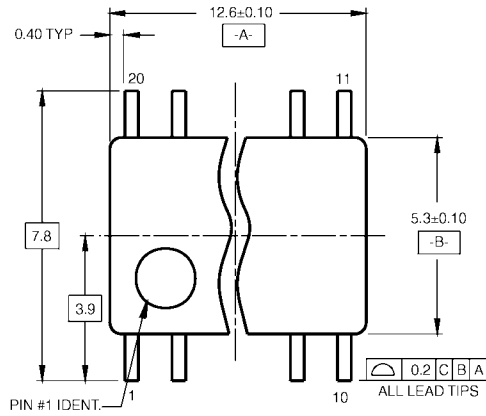
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

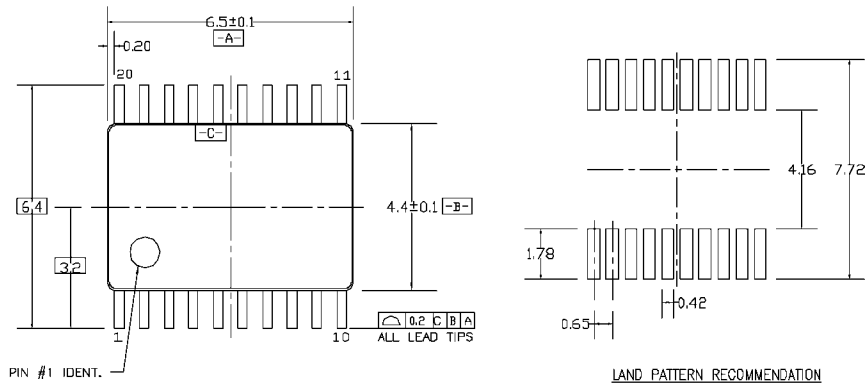
NOTES:

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M20DRevB1

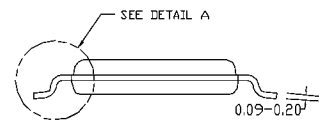
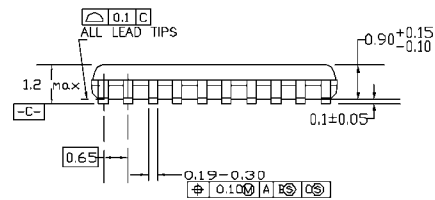
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

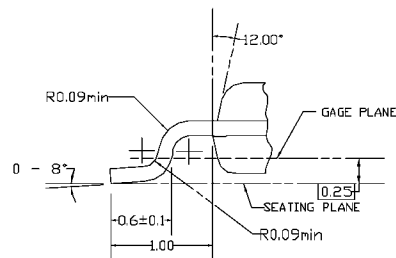


PIN #1 IDENT.

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DETAIL A

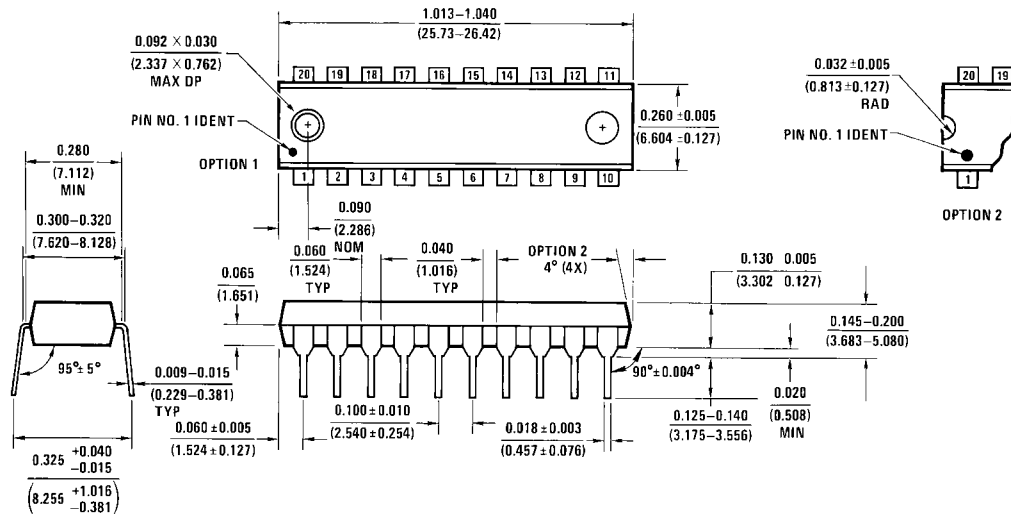
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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