

# MC74LCXU04

## Low-Voltage CMOS Unbuffered Hex Inverter

### With 5 V-Tolerant Inputs

The MC74LCXU04 is a high performance unbuffered hex inverter operating from a 2.3 to 3.6 V supply. (High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance.) A  $V_I$  specification of 5.5 V allows MC74LCXU04 inputs to be safely driven from 5 V devices.

#### Features

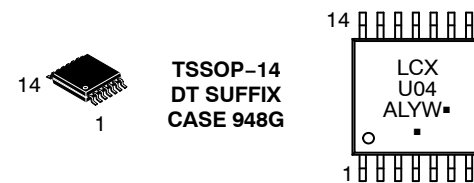
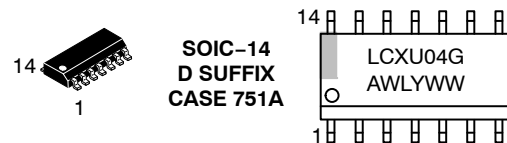
- Designed for 2.3 to 3.6 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVC MOS Compatible
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - ◆ Human Body Model >2000 V
  - ◆ Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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#### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74LCXU04

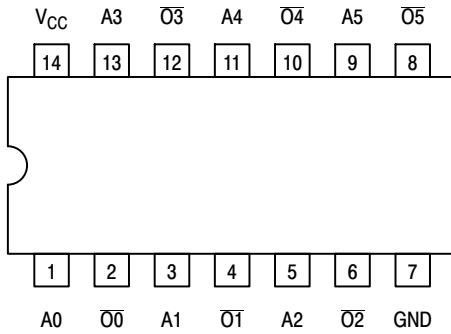


Figure 1. Pinout: 14-Lead (Top View)

## PIN NAMES

Pins	Function
An	Data Inputs
$\bar{O}_n$	Outputs

## TRUTH TABLE

An	$\bar{O}_n$
L	H
H	L

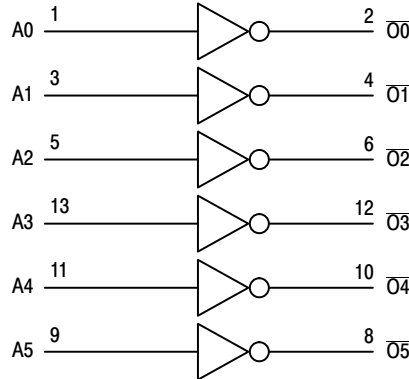


Figure 2. Logic Diagram

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State. (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		$^{\circ}C$
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.

# MC74LCXU04

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V <sub>CC</sub>	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State)	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current V <sub>CC</sub> = 3.0 V – 3.6 V V <sub>CC</sub> = 2.7 V – 3.0 V V <sub>CC</sub> = 2.3 V – 2.7 V			-18 -12 -8	mA
I <sub>OL</sub>	LOW Level Output Current V <sub>CC</sub> = 3.0 V – 3.6 V V <sub>CC</sub> = 2.7 V – 3.0 V V <sub>CC</sub> = 2.3 V – 2.7 V			+16 +12 +8	mA
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Units
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	V <sub>CC</sub> = 2.3 V	1.7		V
		V <sub>CC</sub> = 2.7 V	2.1		
		V <sub>CC</sub> = 3.0 V	2.2		
		V <sub>CC</sub> = 3.6 V	2.7		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	V <sub>CC</sub> = 2.3 V		0.55	V
		V <sub>CC</sub> = 2.7 V		0.55	
		V <sub>CC</sub> = 3.0 V		0.55	
		V <sub>CC</sub> = 3.6 V		0.55	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.5	
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>CC</sub> = 0, V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V		10	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		±5	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

# MC74LCXU04

## AC CHARACTERISTICS ( $t_{\text{R}} = t_{\text{F}} = 2.5 \text{ ns}$ ; $R_{\text{L}} = 500 \Omega$ ) (Note 3)

Symbol	Parameter	Waveform	Limits						Units
			$T_{\text{A}} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$						
			$V_{\text{CC}} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{\text{CC}} = 2.7 \text{ V}$		$V_{\text{CC}} = 2.5 \text{ V} \pm 0.2 \text{ V}$		
			$C_{\text{L}} = 50 \text{ pF}$		$C_{\text{L}} = 50 \text{ pF}$		$C_{\text{L}} = 30 \text{ pF}$		
			Min	Max	Min	Max	Min	Max	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Input to Output	1	1.0 1.0	3.6 3.6	1.0 1.0	4.5 4.5	1.0 1.0	4.3 4.3	ns
$t_{\text{OSHL}}$ $t_{\text{OSLH}}$	Output-to-Output Skew (Note 4)			1.0 1.0					ns

3. These AC parameters are preliminary and may be modified.

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_{\text{A}} = +25^{\circ}\text{C}$			Units
			Min	Typ	Max	
$V_{\text{OLP}}$	Dynamic LOW Peak Voltage (Note 5)	$V_{\text{CC}} = 3.3 \text{ V}, C_{\text{L}} = 50 \text{ pF}, V_{\text{IH}} = 3.3 \text{ V}, V_{\text{IL}} = 0 \text{ V}$ $V_{\text{CC}} = 2.5 \text{ V}, C_{\text{L}} = 30 \text{ pF}, V_{\text{IH}} = 2.5 \text{ V}, V_{\text{IL}} = 0 \text{ V}$		0.8 0.6		V
$V_{\text{OLV}}$	Dynamic LOW Valley Voltage (Note 5)	$V_{\text{CC}} = 3.3 \text{ V}, C_{\text{L}} = 50 \text{ pF}, V_{\text{IH}} = 3.3 \text{ V}, V_{\text{IL}} = 0 \text{ V}$ $V_{\text{CC}} = 2.5 \text{ V}, C_{\text{L}} = 30 \text{ pF}, V_{\text{IH}} = 2.5 \text{ V}, V_{\text{IL}} = 0 \text{ V}$		-0.8 -0.6		V

5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

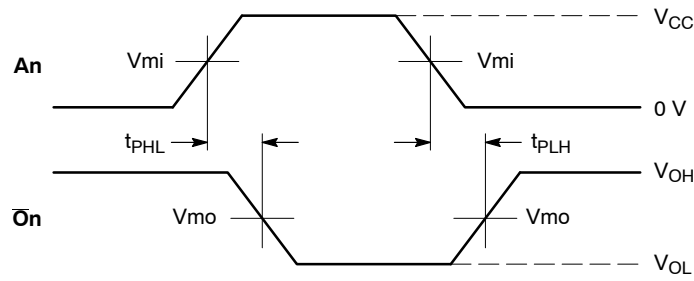
Symbol	Parameter	Condition	Typical	Units
$C_{\text{IN}}$	Input Capacitance	$V_{\text{CC}} = 3.3 \text{ V}, V_{\text{I}} = 0 \text{ V or } V_{\text{CC}}$	7	pF
$C_{\text{OUT}}$	Output Capacitance	$V_{\text{CC}} = 3.3 \text{ V}, V_{\text{I}} = 0 \text{ V or } V_{\text{CC}}$	8	pF
$C_{\text{PD}}$	Power Dissipation Capacitance	10 MHz, $V_{\text{CC}} = 3.3 \text{ V}, V_{\text{I}} = 0 \text{ V or } V_{\text{CC}}$	25	pF

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74LCXU04DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCXU04DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCXU04DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LCXU04DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC74LCXU04

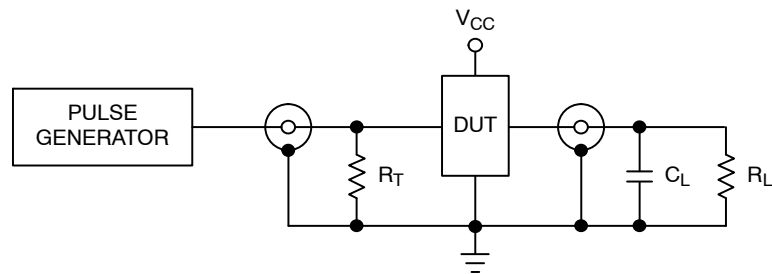


## PROPAGATION DELAYS

$t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Symbol	$V_{CC}$		
	$3.3 \text{ V} \pm 0.3 \text{ V}$	$2.7 \text{ V}$	$2.5 \text{ V} \pm 0.2 \text{ V}$
Vmi	1.5 V	1.5 V	$V_{CC}/2$
Vmo	1.5 V	1.5 V	$V_{CC}/2$

Figure 3. AC Waveforms



$C_L = 50 \text{ pF}$  at  $V_{CC} = 3.3 \pm 0.3 \text{ V}$  or equivalent (includes jig and probe capacitance)

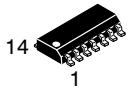
$C_L = 30 \text{ pF}$  at  $V_{CC} = 2.5 \pm 0.2 \text{ V}$  or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

Figure 4. Test Circuit

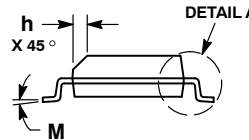
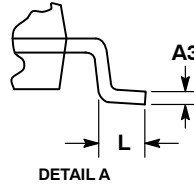
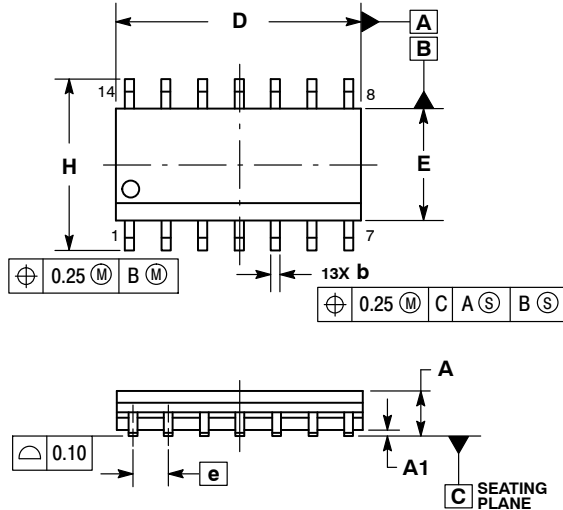
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

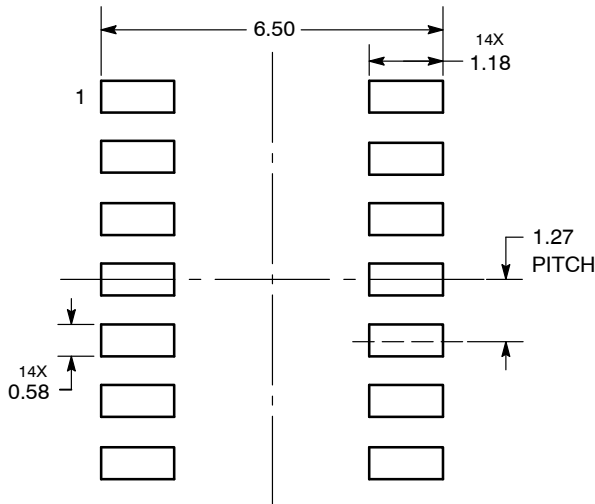


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°		7°	

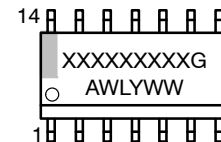
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
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 12. ANODE  
 13. ANODE  
 14. ANODE

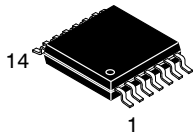
STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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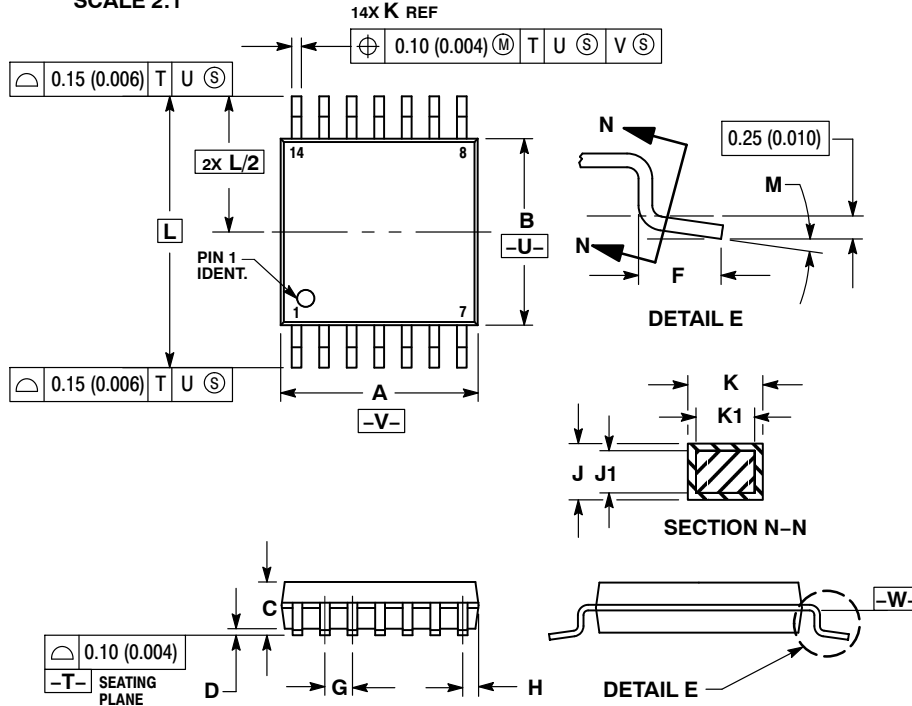
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

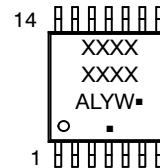
SCALE 2:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

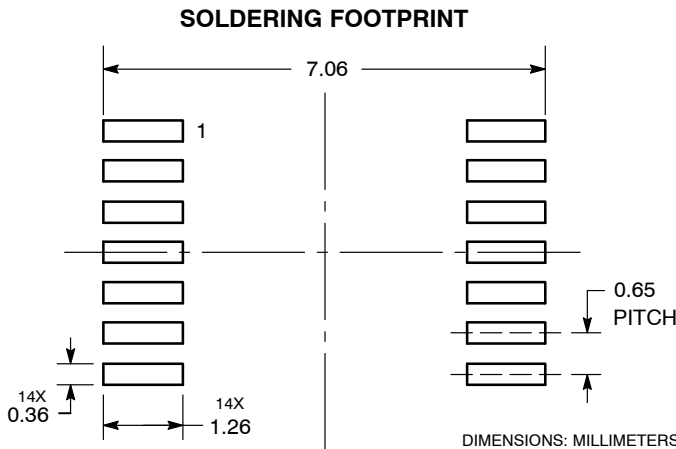
### GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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<b>DESCRIPTION:</b>	<b>TSSOP-14 WB</b>	<b>PAGE 1 OF 1</b>

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