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1 Kb 1-Wire EPROM Add-Only Memory

N21C21A

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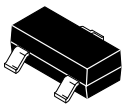
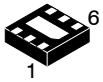


SOT−23
SN SUFFIX
CASE 527AG



UDFN6
MU SUFFIX
CASE 517AP

Description

The N21C21A is a 1K−bit serial EPROM containing a factory−programmed, unique 48−bit identification number, 8−bit CRC generation, and the 8−bit family code (09h). A 64−bit status register controls write protection and page redirection.

The N21C21A 1−wire interface requires only a single connection and a ground return. The DATA pin is also the sole power source for the N21C21A.

The small surface−mount package options saves printed−circuit−board space, while the low cost makes it ideal for applications such as battery pack configuration parameters, record maintenance, asset tracking, product−revision status, and access−code security.

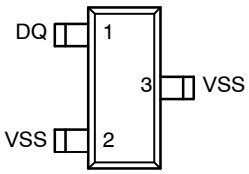
Features

- 1024 Bits of One−Time Programmable (OTP) EPROM For Storage Of User−Programmable Configuration Data
- Factory−Programmed Unique 64−Bit Identification Number
- Single−Wire Interface to Reduce Circuit Board Routing
- Synchronous Communication Reduces Host Interrupt Overhead
- No Standby Power Required
- 8 byte RAM Buffer (Scratch Pad)
- Available in a 3−Pin SOT−23
- This is a Pb−Free Device

Applications

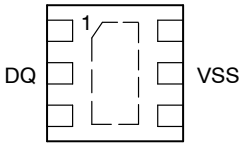
- Security Encoding
- Inventory Tracking
- Product−Revision Maintenance
- Battery−Pack Identification

PIN DESCRIPTIONS



SOT23 (Top View)

Pin Number	Pin Description
1	DQ − DATA Serial I/O
2	VSS
3	VSS



UDFN6 (Top View)

Pin Number	Pin Description
1	Do not connect (NC)
2	DQ − DATA Serial I/O
3	Do not connect (NC)
4	Do not connect (NC)
5	VSS
6	Do not connect (NC)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Units
DC voltage applied to data, V_{PU}	−0.3		12.5	V
Low−level output current, I_{OL}			40	mA
Operating free−air temperature, T_A	−20		70	°C
Communication free−air temperature, $T_{A(Comm)}$	−40		85	°C
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}	−55		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. D.C. OPERATING CHARACTERISTICS (T_A = −40°C to +85°C, VPU = 2.65 V to 5.5 V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{PU}	Pull−up Voltage		2.65		5.5	V
I_{DATA}	Supply current	V_{PU} = 5.5 V			20	μA
V_{OL}	Low−level output voltage	Logic 0, V_{PU} = 5.5 V, I_{OL} = 4 mA, DQ pin			0.4	V
		Logic 0, V_{PU} = 2.65 V, I_{OL} = 2 mA			0.4	
V_{OH}	High−level output voltage	Logic 1		V_{PU}	5.5	
I_{OL}	Low−level output current (sink)	V_{OL} = 0.4 V, DQ pin			4	mA
V_{IL}	Low−level input voltage	Logic 0			0.8	V
V_{IH}	High−level input voltage	Logic 1	2.2			V
V_{PP}	Programming voltage		11.5		12	V
R_{PU}	Serial communication interface pull−up resistance			5		kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Tested initially and after a design or process change that affects this parameter

Table 3. A.C. CHARACTERISTICS (T_A = −40°C to +85°C, VPU = 2.65 V to 5.5 V)

Symbol	Parameter	Min	Max	Unit
t_c	Bit cycle time	60	120	μs
t_{WSTRB}	Write start cycle	1	15	μs
t_{WDSU}	Write data setup	t_{WSTRB}	15	μs
t_{WDH}	Write data hold	60	t_c	μs
t_{rec}	Recovery time	1		μs
		5		
t_{RSTRB}	Read start cycle	1	13	μs
t_{ODD}	Output data delay	t_{RSTRB}	13	μs
t_{ODHO}	Output data hold	17	60	μs
t_{RST}	Reset time	480		μs
t_{PPD}	Presence pulse delay	15	60	μs
t_{PP}	Presence pulse	60	240	μs
t_{EPROG}	EPROM programming time	2500		μs
t_{EDN}	EDN programming time		5000	μs
t_{PSU}	Program setup time	5		μs
t_{PREC}	Program recovery time	5		μs
t_{PRE}	Program rising−edge time		5	μs
t_{PFE}	Program falling−edge time		5	μs
t_{RSTREC}		480		μs

Table 4. PIN CAPACITANCE

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
$C_{IN/OUT}$	DATA Pin Capacitance	T_A = 25°C		800	pF

Detailed Description

Overview

The Functional Block Diagram shows the relationships among the major control and memory sections of the N21C21A. The N21C21A has three main data components: a 64−bit factory−programmed ROM, including 8−bit family code, 48−bit identification number and 8−bit CRC value, 1024−bit EPROM, and EPROM STATUS bytes. Power for read and write operations is derived from the DATA pin. An internal capacitor stores energy while the signal line is high and releases energy during the low times of the DATA pin, until the pin returns high to replenish the charge on the capacitor. A special manufacturer's PROGRAM PROFILE BYTE can be read to determine the programming profile required to program the part.

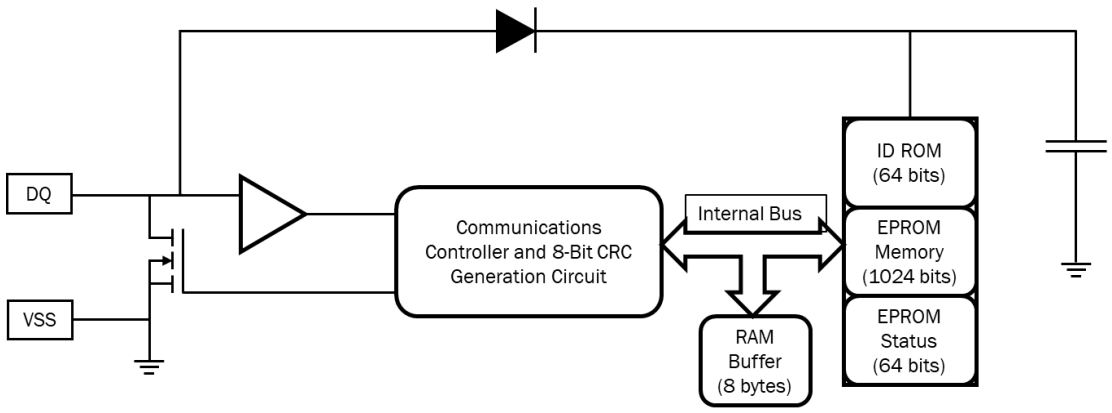


Figure 1. Functional Block Diagram

Feature Description

1024−Bit EPROM

Table 5 is a memory map of the 1024−bit EPROM section of the N21C21A, configured as four pages of 32 bytes each. The 8−byte RAM buffers are additional registers used when programming the memory. Data are first written to the RAM buffer and then verified by reading an 8−bit CRC from the N21C21A that confirms proper receipt of the data. If the buffer contents are correct, a programming command is issued and an 8−byte segment of data is written into the selected address in memory. This process ensures data integrity when programming the memory. The details for reading and programming the 1024−bit EPROM portion of the N21C21A are in the Memory/Status Function Commands section of this data sheet.

Table 5. 1024−Bit EPROM DATA MEMORY MAP

ADDRESS(HEX)	PAGE
0060−007F	Page 3
0040−005F	Page 2
0020−003F	Page 1
0000−001F	Page 0

EPROM Status Memory

In addition to the programmable 1024−bits of memory are 64 bits of status information contained in the EPROM STATUS memory. The STATUS memory is accessible with separate commands. The STATUS bits are EPROM and are read or programmed to indicate various conditions to the software interrogating the N21C21A. The first byte of the STATUS memory contains the write protect page bits, that inhibit programming of the corresponding page in the 1024−bit main memory area if the appropriate write−protection bit is programmed. Once a bit has been programmed in the write protect page byte, the entire 32−byte page that corresponds to that bit can no longer be altered but may still be read. The write protect bits may be cleared by using the WRITE STATUS command.

The next four bytes of the EPROM STATUS memory contain the page address redirection bytes. Bits in the EPROM status bytes can indicate to the host what page is substituted for the page by the appropriate redirection byte. The hardware of the N21C21A makes no decisions based on the contents of the page address redirection bytes. This feature allows the user's software to make a data patch to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the page address redirection bytes. The ones complement of the new page address is written into the page address redirection byte that corresponds to the original (replaced) page. If a page address redirection byte has an FFh value, the data in the main memory that corresponds to that page are valid. If a page address redirection byte has some other hex value, the data in the page corresponding to that redirection byte are invalid, and the valid data can now be found at the ones complement of the page address indicated by the hexadecimal value stored in the associated page address redirection byte. A value of FDh in the redirection byte for page 1, for example, indicates that the updated data are now in page 2. The details for reading and programming the EPROM status memory portion of the N21C21A are given in the Memory/Status Function Commands section.

Table 6. EPROM STATUS BYTES

ADDRESS (HEX)	PAGE
00h	Write protection bits BIT0 − write protect page 0 BIT1 − write protect page 1 BIT2 − write protect page 2 BIT3 − write protect page 3 BIT4 to 7−bitmap of used pages
01h	Redirection byte for page 0
02h	Redirection byte for page 1
03h	Redirection byte for page 2
04h	Redirection byte for page 3
05h	Reserved
06h	Reserved
07h	Factory programmed 00h

Error Checking

To validate the data transmitted from the N21C21A, the host generates a CRC value from the data as they are received. This generated value is compared to the CRC value transmitted by the N21C21A. If the two CRC values match, the transmission is error−free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. Details are found in the CRC Generation section of this data sheet.

Customizing the N21C21A

The 64−bit ID identifies each N21C21A. The 48−bit serial number is unique and programmed by the factory. The default 8−bit family code is 09h; however, a different value can be reserved on an individual customer basis. Contact your ON Semiconductor for more information.

Bus Termination

Because the drive output of the N21C21A is an open−drain, N−channel MOSFET, the host must provide a source current or a 5−kΩ external pullup, as shown in the typical application circuit.

Device Functional Modes

The device is in active mode during communication or while the DQ is kept at valid Vpu voltages.

Programming

Serial Communication

A host reads, programs, or checks the status of the N21C21A through the command structure of the DQ interface.

Initialization

Initialization consists of two pulses, the RESET and the PRESENCE pulses. The host generates the RESET pulse, while the N21C21A responds with the PRESENCE pulse. The host resets the N21C21A by driving the DATA bus low for at least 480 μs. For more details, see the *RESET and PRESENCE PULSE* section.

ROM Commands

READ ROM Command

The READ ROM command sequence is the fastest sequence that allows the host to read the 8−bit family code and 48−bit identification number. The READ ROM sequence starts with the host generating the RESET pulse of at least 480 μs. The N21C21A responds with a PRESENCE pulse. Next, the host continues by issuing the READ ROM command, 33h, and then reads the ROM and CRC byte using the READ signaling (see the READ and WRITE signals section) during the data frame.

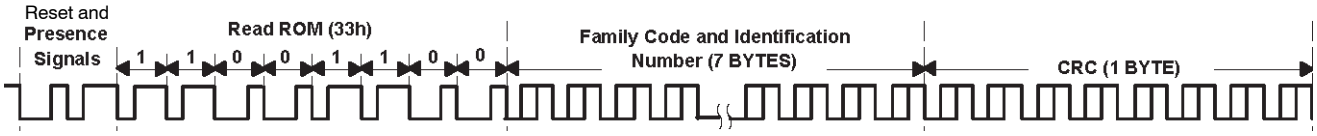


Figure 2. READ ROM Sequence

SKIP ROM Command

The SKIP ROM command, CCh, allows the host to access the memory/status functions. The SKIP ROM command is directly followed by a memory/status functions command.

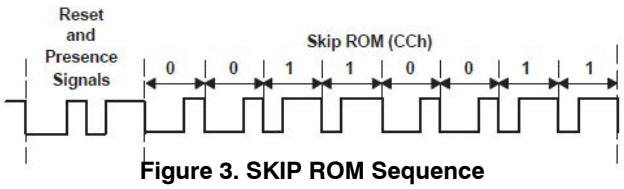


Figure 3. SKIP ROM Sequence

Six memory/status function commands allow read and modification of the 1024−bit EPROM data memory or the 64−bit EPROM status memory. There are two types of READ MEMORY command, plus the WRITE MEMORY, READ STATUS, and WRITE STATUS commands. Additionally, the part responds to a PROGRAM PROFILE byte command. The N21C21A responds to memory/status function commands only after a part is issued a SKIP ROM command.

READ MEMORY Commands

Two READ MEMORY commands are available on the N21C21A. Both commands are used to read data from the 1024−bit EPROM data field. They are the READ MEMORY/Page CRC and the READ MEMORY/Field CRC commands. The READ MEMORY/Page CRC generates CRC at the end any 32−byte page boundary whereas the READ MEMORY/Field CRC generates CRC when the end of the 1024−bit data memory is reached.

READ MEMORY/Page CRC

To read memory and generate the CRC at the 32−byte page boundaries of the N21C21A, the SKIP ROM command is followed by the READ MEMORY/Generate CRC command, C3h, followed by the address low byte and then the address high byte.

An 8−bit CRC of the command byte and address bytes is computed by the N21C21A and read back by the host to confirm that the correct command word and starting address were received. If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the N21C21A starting at the initial address and continuing until the end of a 32−byte page is reached. At that point, the host sends eight additional read time slots and receive an 8−bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8−bit CRC has been received, data is again read from the 1024−bit EPROM data field starting at the next page. This sequence continues until the final page and its accompanying CRC are read by the host. Thus each page of data can be considered to be 33 bytes long, the 32 bytes of user−programmed EPROM data and an 8−bit CRC that gets generated automatically at the end of each page.

Table 7. READ MEMORY/PAGE CRC

Initialization and SKIP ROM Command Sequence	READ MEMORY/ Generate CRC Command	Address Low Byte	Address High Byte	Read and Verify CRC	EPROM Memory and CRC Byte Generated at 32−Byte Page Boundaries
	C3h	A0 A7	A8 A15		

NOTE: Individual bytes of address and data are transmitted LSB first.

READ MEMORY/Field CRC

To read memory without CRC generation on 32−byte page boundaries, the SKIP ROM command is followed by the READ MEMORY command, F0h, followed by the address low byte and then the address high byte.

An 8−bit CRC of the command byte and address bytes is computed by the N21C21A and read back by the host to confirm that the correct command word and starting address were received. If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the N21C21A starting at the initial address and continuing until the end of the 1024−bit data field is reached or until a reset pulse is issued. If reading occurs through the end of memory space, the host may issue eight additional read time slots and the N21C21A responds with an 8−bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the host, any subsequent read time slots appear as logical 1s until a reset pulse is issued. Any reads ended by a reset pulse prior to reaching the end of memory does not have the 8−bit CRC available.

Table 8. READ MEMORY/FIELD CRC

Initialization and SKIP ROM Command Sequence	READ MEMORY Command	Address Low Byte	Address High Byte	Read and Verify CRC	Read EPROM Memory Until End of EPROM Memory	Read and Verify CRC
	F0h	A0 A7	A8 A15			

WRITE MEMORY Command

The WRITE MEMORY command is used to program the 1024−bit EPROM memory field. The 1024−bit memory field is programmed in 8−byte segments. Data is first written into an 8−byte RAM buffer one byte at a time. The contents of the RAM buffer is then ANDed with the contents of the EPROM memory field when the programming command is issued.

Figure 4 illustrates the sequence of events for programming the EPROM memory field. After issuing a SKIP ROM command, the host issues the WRITE MEMORY command, 0Fh, followed by the low byte and then the high byte of the starting address. The N21C21A calculates and transmits an 8−bit CRC based on the WRITE command and address.

If at any time during the WRITE MEMORY process, the CRC read by the host is incorrect, a reset pulse must be issued, and the entire sequence must be repeated.

After the N21C21A transmits the CRC, the host then transmits 8 bytes of data to the N21C21A. Another 8−bit CRC is calculated and transmitted based on the 8 bytes of data. If this CRC agrees with the CRC calculated by the host, the host transmits the program command 5Ah and then applies the programming voltage for at least 2500 μs or t_{EPROG}. The contents of the RAM buffer is then logically ANDed with the contents of the 8−byte EPROM offset by the starting address.

The starting address can be any integer multiple of eight between 0000 and 007F (hex) such as 0000, 0008, and 0010 (hex).

The WRITE DATA MEMORY command sequence can be terminated at any point by issuing a reset pulse except during the program pulse period t_{PROG}.

For both of these cases, the decision to continue programming is made entirely by the host, because the N21C21A is not able to determine if the 8−bit CRC calculated by the host agrees with the 8−bit CRC calculated by the N21C21A.

Prior to programming, bits in the 1024−bit EPROM data field appear as logical 1s.

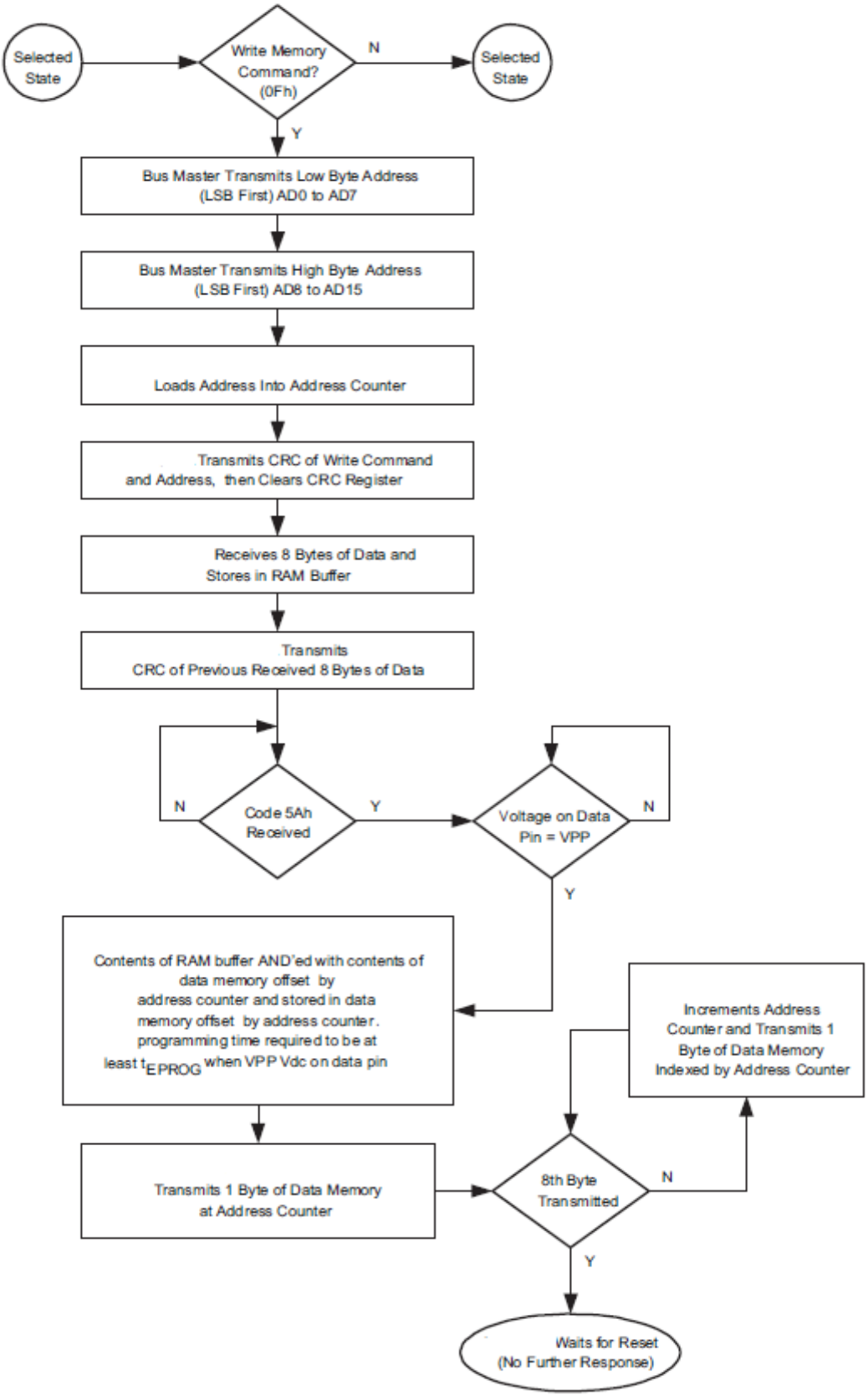


Figure 4. WRITE MEMORY Command Flow

READ STATUS Command

The READ STATUS command is used to read data from the EPROM status data field. After issuing a SKIP ROM command, the host issues the READ STATUS command, AAh, followed by the address low byte and then the address high byte.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the N21C21A starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point, the host receives an 8−bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final factory−programmed byte that contains the 00h value.

This feature is provided because the EPROM status information may change over time making it impossible to program the data once and include an accompanying CRC that is always valid. Therefore, the READ status command supplies an 8−bit CRC that is based on (and always is consistent with) the current data stored in the EPROM status data field.

After the 8−bit CRC is read, the host receives logical 1s from the N21C21A until a reset pulse is issued. The

READ STATUS command sequence can be ended at any point by issuing a reset pulse.

Table 9. READ STATUS COMMAND

Initialization and SKIP ROM Command Sequence	READ STATUS Command	Address Low Byte	Address High Byte	Read and Verify CRC	Read STATUS Memory Until End of STATUS Memory	Read and Verify CRC
	AAh	A0 A7	A8 A15			

WRITE STATUS Command

The WRITE STATUS command is used to program the EPROM Status data field after the N21C21A has been issued SKIP ROM command.

The flow chart in Figure 5 illustrates that the host issues the WRITE STATUS command, 55h, followed by the address low byte and then the address high byte the followed by the byte of data to be programmed.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the program command (5Ah) is issued. After the program command is issued, then the programming voltage, V_{PP} is applied to the DATA pin for period t_{PROG}. Prior to programming, the first seven bytes of the EPROM STATUS data field appear as logical 1s. For each bit in the data byte provided by the host that is set to a logical 0, the corresponding bit in the selected byte of the EPROM STATUS data field is programmed to a logical 0 after the programming pulse has been applied at the byte location. The eighth byte of the EPROM STATUS byte data field is factory−programmed to contain 00h.

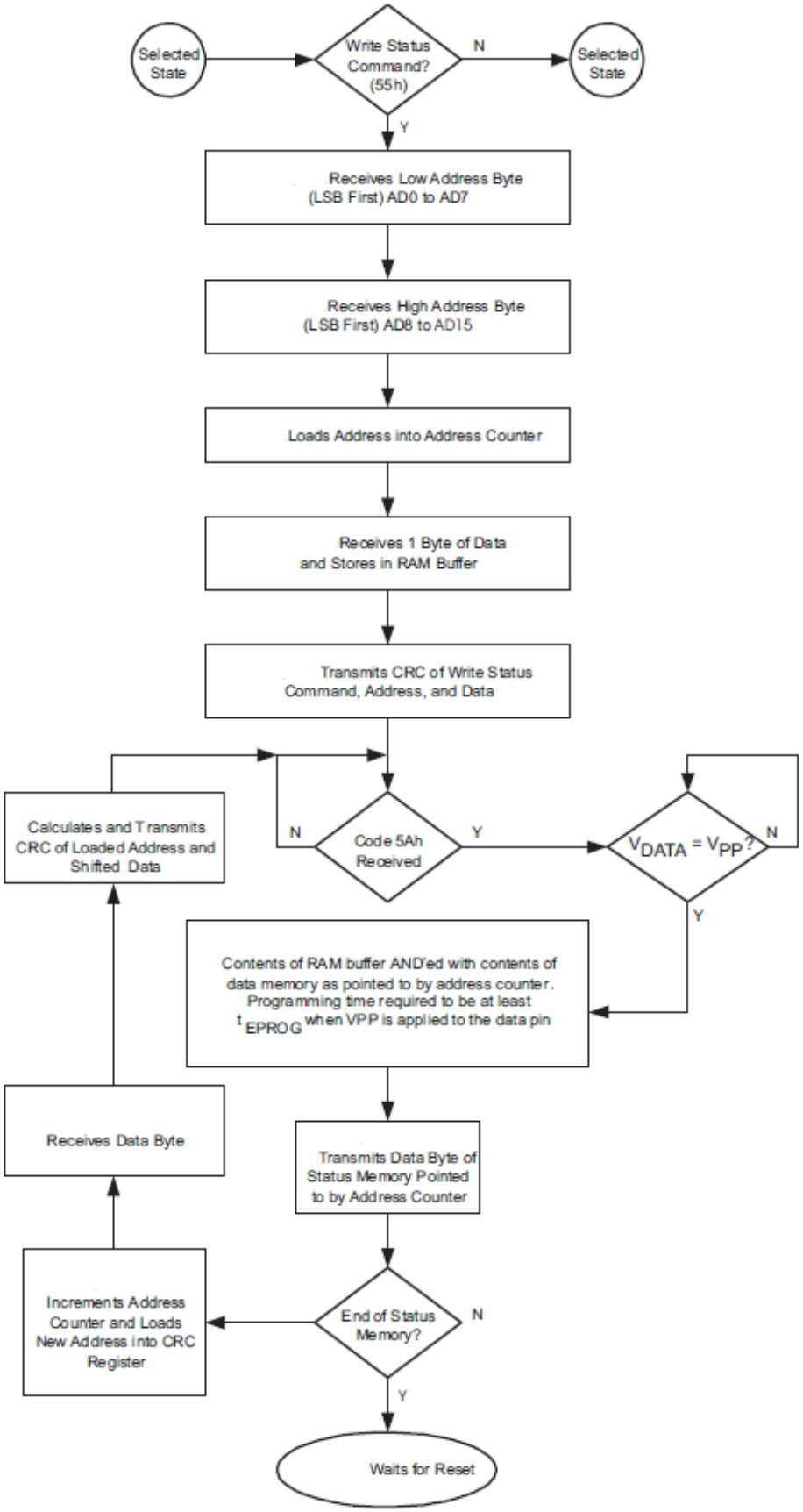


Figure 5. WRITE STATUS Command Flow

After the programming pulse is applied and the data line returns to V_{PU}, the host issues eight read time slots to verify that the appropriate bits have been programmed. The N21C21A responds with the data from the selected EPROM STATUS address sent least significant bit first. This response should be checked to verify the programmed byte. If the programmed byte is incorrect, then the host must reset the device and begin the write sequence again. If the N21C21A EPROM data byte programming was successful, the N21C21A automatically increments its address counter to select the next byte in the STATUS MEMORY data field. The least significant byte of the new two−byte address is also loaded into the 8−bit CRC generator as a starting value. The host issues the next byte of data using eight write time slots.

As the N21C21A receives this byte of data into the RAM buffer, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8−bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the host reads this 8−bit CRC from the N21C21A with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the host issues a programming pulse and the selected byte in memory is programmed.

For both of these cases, the decision to continue programming the EPROM Status registers is made entirely by the host, because the N21C21A is not able to determine if the 8−bit CRC calculated by the host agrees with the 8−bit CRC calculated by the N21C21A. If an incorrect CRC is ignored and a program pulse is applied by the host, incorrect programming could occur within the N21C21A. Also note that the N21C21A always increments its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the host, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the WRITE STATUS command, incorrect programming could occur within the N21C21A. The WRITE STATUS command sequence can be ended at any point by issuing a reset pulse.

Table 10. COMMAND CODE SUMMARY

COMMAND (HEX)	DESCRIPTION	CATEGORY
33h	Read Serialization ROM and CRC	ROM Commands Available in Command Level I
CCh	Skip Serialization ROM	
F0h	Read Memory/Field CRC	Memory Function Commands Available in Command Level II
AAh	Read EPROM Status	
C3h	Read Memory/Page CRC	
0Fh	Write Memory	
99h	Programming Profile	
55h	Write EPROM Status	
5Ah	Program Control	Program Command Available Only in WRITE MEMORY and WRITE STATUS Modes

PROGRAM PROFILE Byte

The PROGRAM PROFILE byte is read to determine the WRITE MEMORY programming sequence required by a specific manufacturer. After issuing a ROM command, the host issues the PROGRAM PROFILE BYTE command, 99h. Figure 6 shows the N21C21A responds with 55h. This informs the host that the WRITE MEMORY programming sequence is the one described in the WRITE MEMORY Command section of this data sheet.

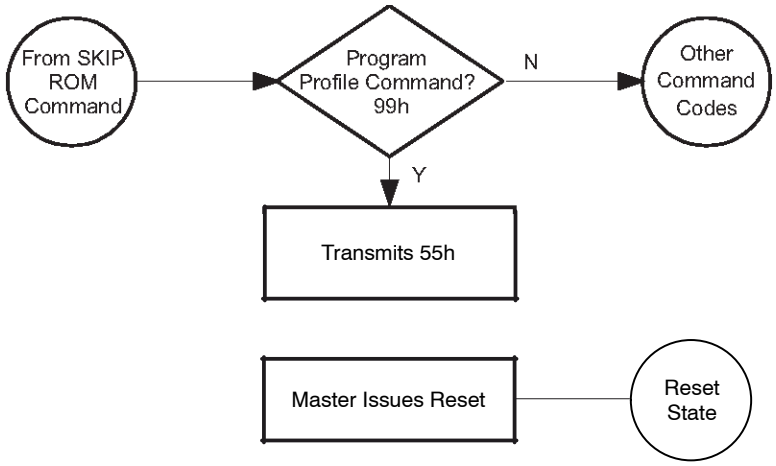


Figure 6. PROGRAM PROFILE Command Flow

DQ Signaling

All DQ signaling begins with initializing the device, followed by the host driving the bus low to write a 1 or 0, or to begin the start frame for a bit read. Figure 7 shows the initialization timing, whereas Figure 8 and Figure 9 show that the host initiates each bit by driving the DATA bus low for the start period, t_{WSTRB} / t_{RSTRB}. After the bit is initiated, either the host continues controlling the bus during a WRITE, or the N21C21A responds during a READ.

RESET and PRESENCE PULSE

If the DATA bus is driven low for more than 120 μs, the N21C21A may be reset. Figure 8 shows that if the DATA bus is driven low for more than 480 μs, the N21C21A resets and indicates that it is ready by responding with a PRESENCE PULSE.

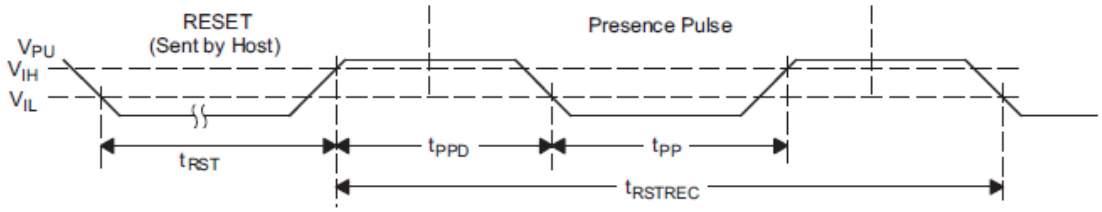


Figure 7. Reset Timing Diagram

WRITE Bit

The WRITE bit timing diagram in Figure 8 shows that the host initiates the transmission by issuing the twsTRB portion of the bit and then either driving the DATA bus low for a WRITE 0, or releasing the DATA bus for a WRITE 1.

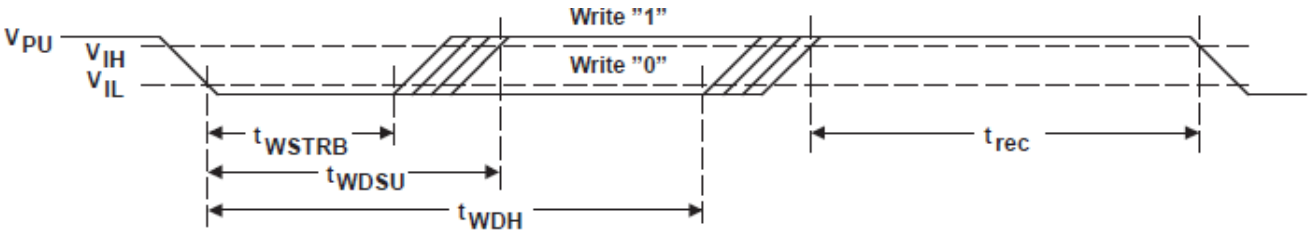


Figure 8. WRITE Bit Timing Diagram

READ Bit

The READ bit timing diagram in Figure 9 shows that the host initiates the transmission of the bit by issuing the tRsTRB portion of the bit. The N21C21A then responds by either driving the DATA bus low to transmit a READ 0 or releasing the DATA bus to transmit a READ 1.

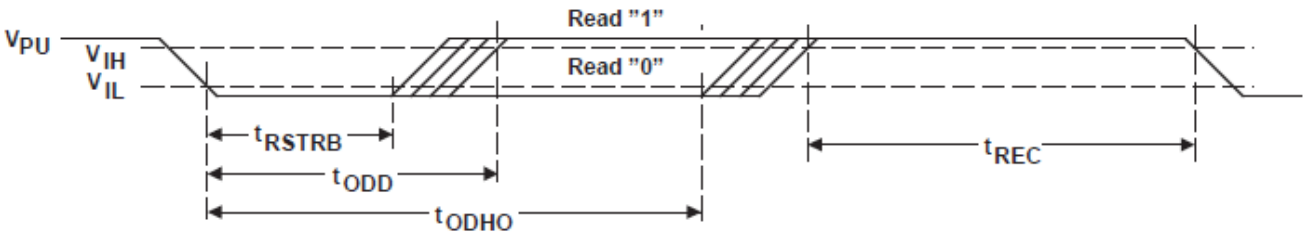


Figure 9. READ Bit Timing Diagram

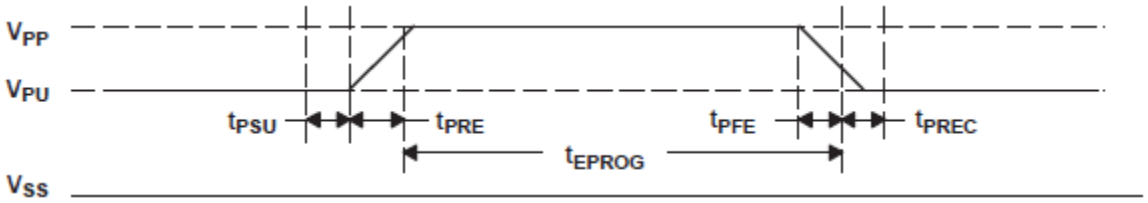


Figure 10. PROGRAM PULSE Timing Diagram

IDLE

If the bus is high, the bus is in the IDLE state. Bus transactions can be suspended by leaving the DATA bus in IDLE. Bus transactions can resume at any time from the IDLE state.

CRC Generation

The N21C21A has an 8−bit CRC stored in the most significant byte of the 64−bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64−bit ROM and compare it to the value stored within the N21C21A to determine if the ROM data has been received error−free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

Under certain conditions, the N21C21A also generates an 8−bit CRC value using the same polynomial function just shown and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the N21C21A. The N21C21A computes an 8−bit CRC for the command, address, and data bytes received for the WRITE MEMORY and the WRITE STATUS commands and then outputs this value to the bus master to confirm proper transfer. Similarly, the N21C21A computes an 8−bit CRC for the command and address bytes received from the bus master for the READ MEMORY, READ STATUS, and READ DATA/ GENERATE 8−BIT CRC commands to confirm that these bytes have been received correctly. The CRC generator on the N21C21A is also used to provide verification of error−free data transfer as each page of data from the 1024−bit EPROM is sent to the bus master during a READ DATA/GENERATE 8−BIT CRC command, and for the eight bytes of information in the status memory field.

In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function previously given and compare the calculated value to either the 8−bit CRC value stored in the 64−bit ROM portion of the N21C21A (for ROM reads) or the 8−bit CRC value computed within the N21C21A. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. No circuitry on the N21C21A prevents a command sequence from proceeding if the CRC stored in or calculated by the N21C21A does not match the value generated by the bus master. Proper use of the CRC can result in a communication channel with a high level of integrity.

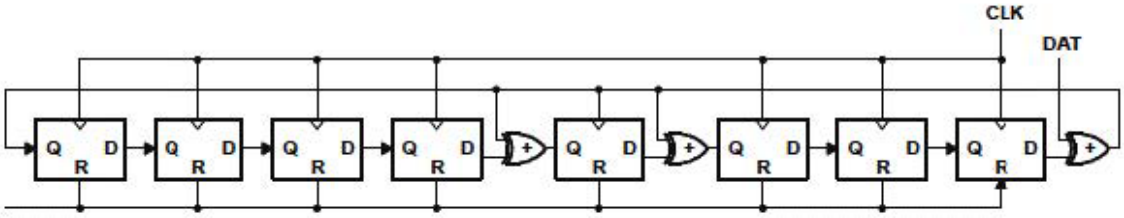


Figure 11. 8−Bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$)

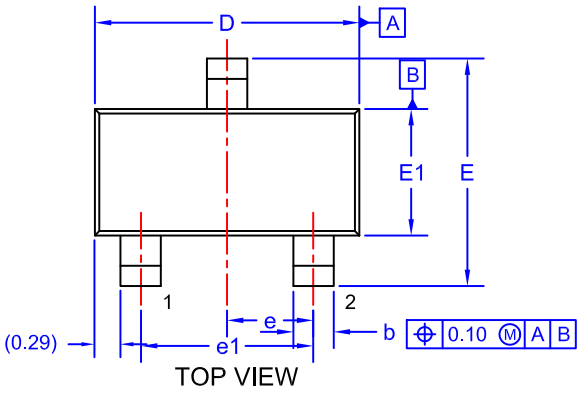
ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
N21C21ASNDT3G	C21	SOT-23−3	−40°C to +85°C	Ni PdAu	3000 / Tape & Reel
N21C21AMU6DT3G*	WA	UDFN6	−40°C to +85°C	Ni PdAu	3000 / Tape & Reel

2. All packages are RoHS−compliant (Lead−free, Halogen−free)
*Product under development
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

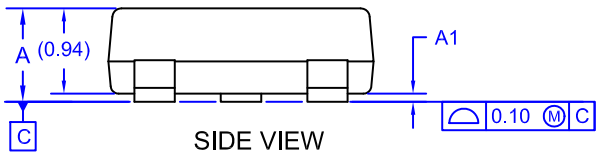
SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

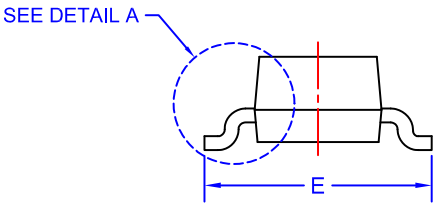


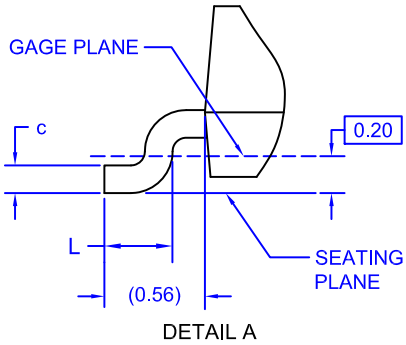
NOTES: UNLESS OTHERWISE SPECIFIED

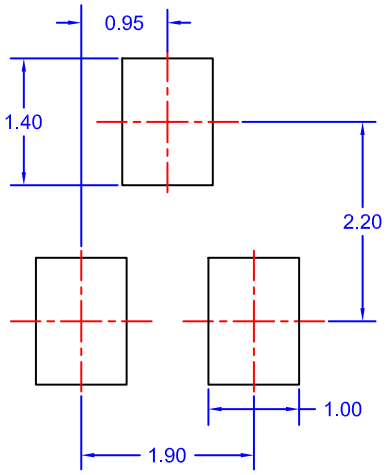
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43







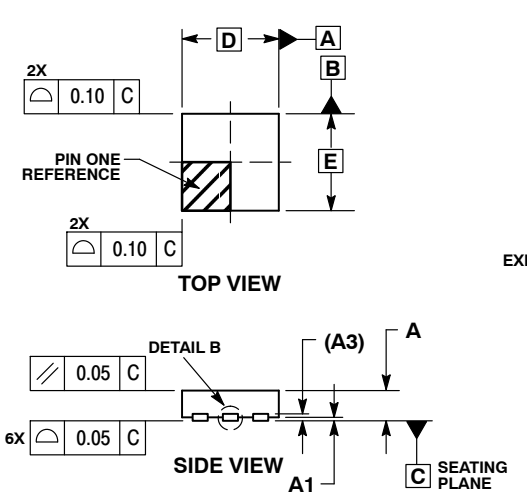


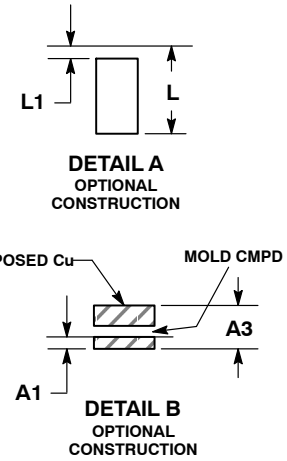
LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

PACKAGE DIMENSIONS

UDFN6 1.6x1.6, 0.5P
CASE 517AP
ISSUE O

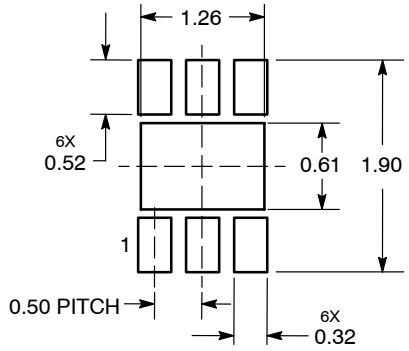




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D2	1.10	1.30
E2	0.45	0.65
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Phone: 011 421 33 790 2910

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Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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