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CMOS LSI

On-Screen Display LSI for Camcorder

Overview

The LC74772V is a CMOS LSI that implements on-screen display for camcorders. It displays characters and patterns in a camcorder viewfinder under microprocessor control. The LC74772V displays a 12×18 dot font with 256 characters.

Functions

- Screen format: 12 lines × 24 characters (up to 288 characters)
- Number of characters displayed: Up to 288 characters
- Character format: 12 (horizontal) × 18 (vertical) dots
- Number of characters in font: 256 characters
- Character sizes: Normal and double, specified in line units
- Display start position
 - Horizontal: 64 positions
- Vertical: 64 positions
- Character reverse video function: Individual characters can be displayed in reverse video.
- Types of blinking: Two types with periods of 1.0 and 0.5 seconds, specifiable on a per character basis.

(Blinking has a 60% display on duty.)

(Four divisors: 1/25, 1/30, 1/50, 1/60)

- Outputs: R, G, B plus 2 output systems
 - Or: 4 output systems (character data and blanking data: 4 outputs each)
- External control input: 8-bit serial data input format.

Specifications

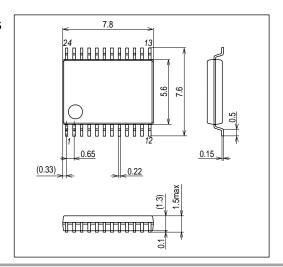
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Supply voltage	V _{DD}	VDD	Vss – 0.3 to Vss + 7.0	V
Input voltage	Vin	All input pins	Vss - 0.3 to Vpp + 0.3	V
Output voltage	Vouт	CKOUT, CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK	Vss - 0.3 to Vpp + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	300	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Package Dimensions

unit: mm SSOP24(275mil)



Allowable Operating Ranges at $Ta = -30 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	Conditions		Unit			
Farameter	Symbol		min	typ	max	I OTHE	
Supply voltage	V _{DD}	V _{DD}	2.7	5.0	5.5	V	
Input high-level voltage	V _{IH}		0.8 V _{DD}		V _{DD} + 0.3	V	
Input low-level voltage	V _{IL}	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	V _{SS} - 0.3		0.2 V _{DD}	V	
Oscillator frequency	Fosc	OSC _{IN} , OSC _{OUT} (LC oscillator)	6	(8)	10	MHz	

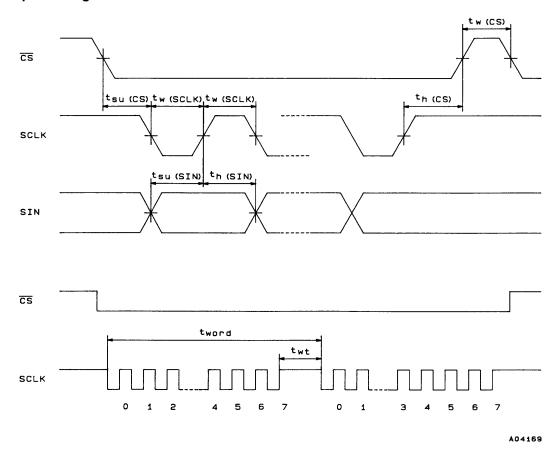
Electrical Characteristics at Ta = -30 to $+70^{\circ}C$, unless otherwise specified $V_{DD} = 5~V$

Parameter	Symbol	Symbol Conditions		Ratings				
Farameter	Symbol	Conditions	min	typ	max	Unit		
Output high-level voltage	V _{OH}	CK _{OUT} , CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: $V_{DD} = 5.5$ to 4.5 V ($V_{DD} = 4.4$ to 2.7 V), $I_{OH} = -1.0$ mA (-0.5 mA)	0.9 V _{DD}			V		
Output low-level voltage	V _{OL}	CK_{OUT} , CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: $V_{DD} = 5.5$ to 4.5 V ($V_{DD} = 4.4$ to 2.7 V), $I_{OL} = 1.0$ mA (0.5 mA)			0.1 V _{DD}	V		
Input current	I _{IH}	$\frac{\text{CTRL1, TEST_{IN}, \overline{CS}, SCLK, SIN, OUT_{MOD}, \overline{HSYNC},}}{\text{VSYNC: V_{IN} = V_{DD}}}$			1	μΑ		
	I _{IL}	CTRL1, TEST _{IN} , HSYNC, VSYNC: V _{IN} = V _{SS}	-1	·	·	μΑ		
Operating current drain	I _{DD}	V _{DD} pin; all outputs open, LC oscillator: 8 MHz			10	mA		

Timing Characteristics at $Ta = -30~to~+70^{\circ}C,~V_{DD} = 5 \pm 0.5~V$

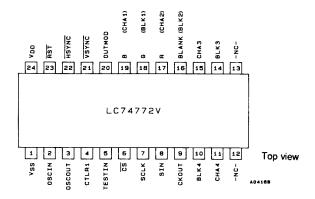
Parameter	Sumbol	Symbol Conditions		Ratings				
Farameter	Symbol		min	typ	max	Unit		
Minimum input pulse width	t _{W (SCLK)}	SCLK	200			ns		
wiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	t _{W (CS)}	CS (the period that CS is high)	1			μs		
Data setup time	t _{SU (CS)}	CS	200			ns		
Data setup time	t _{SU (SIN)}	SIN	200			ns		
Data hold time	t _{h (CS)}	CS	2			μs		
Data fiold time	t _{h (SIN)}	SIN	200			ns		
One-word write time	t _{word}	The time to write 8 bits of data	4.2			μs		
One-word write tille	t _{wt}	The RAM data write time	1			μs		

Serial Data Input Timing



Pin Assignment

The signal names in parentheses indicate the output pin functions when 4-system output mode is used.

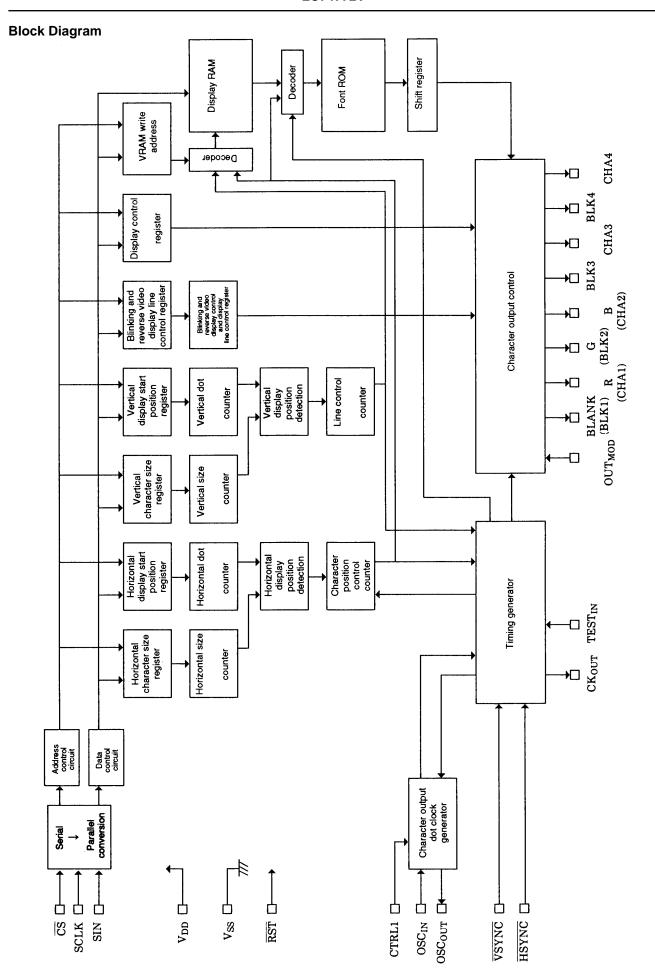


Pin Functions

PinNo.	Symbol	Function	Description
1	V _{SS}	Ground	Ground connection
2	OSC _{IN}	LC oscillator	Connections for the coil and capacitor that form the oscillator that generates the character
3	OSC _{OUT}	LO OSCINATOI	output horizontal dot clock.
4	CTRL1	Clock input control	Control input that switches between LC oscillator mode and clock input mode Low: LC oscillator mode, high: clock input mode
5	TEST _{IN}	Test control input	Test mode control input (The IC operates in test mode when this input is high.)
6	CS	Enable input	Serial data input enable input Low: active (This input has hysteresis characteristics.)
7	SCLK	Clock input	Serial data input clock input (This input has hysteresis characteristics.)
8	SIN	Data input	Serial data input (This input has hysteresis characteristics.)
9	CK _{OUT}	Clock output	LC oscillator clock monitor output This signal is output when RST is low.
10	BLK4	Blanking signal output	Blanking signal output (system 2) Functions as the system 4 blanking data signal output in 4-system mode.
11	CHA4	Character data output	Character data signal output (system 2) Functions as the system 4 character data signal output in 4-system mode.
12	NC	Unused	Must be left open or tied to ground in normal operation.
13	NC	Unused	Must be left open or tied to ground in normal operation.
14	BLK3	Blanking signal output	Blanking signal output (system 1) Functions as the system 3 blanking data signal output in 4-system mode.
15	CHA3	Character data output	Character data signal output (system 1) Functions as the system 3 character data signal output in 4-system mode.
16	BLANK	Blanking signal output	Blanking signal output (blanking signal for RGB output) Functions as the system 2 blanking data signal output in 4-system mode.
17	R	Character data output	Character data (R) signal output Functions as the system 2 character data signal output in 4-system mode.
18	G	Character data output	Character data (G) signal output Functions as the system 1 blanking data signal output in 4-system mode.
19	В	Character data output	Character data (B) signal output Functions as the system 1 character data signal output in 4-system mode.
20	OUT _{MOD}	Output control input	Control input that switches between RGB output and 4-system output Low: RGB output, high 4-system output
21	VSYNC	Vertical synchronizing signal input	Vertical synchronizing signal input (This input has hysteresis characteristics.)
22	HSYNC	Horizontal synchronizing	Horizontal synchronizing signal input (This input has hysteresis characteristics.) signal input
23	RST	Reset input	System reset signal input (This input has hysteresis characteristics.)
24	V _{DD}	Power supply	Power supply connection (+5 V)

Note: 1. Built-in pull-up resistors can be specified for inclusion in the \overline{CS} (pin 6), SCLK (pin 7), SIN (pin 8), and \overline{RST} (pin 23) pins as mask options.

2. In clock input mode (when CTRL1 is high), the function that holds the OSC_{IN} (pin 2) pin high during an oscillator reset is stopped.



Display Control Commands

The display control commands have an 8-bit serial input format. Data is input LSB first.

Display Control Command Table

				First	byte	byte Second byte										
Command		Command code				Data			Data							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND 0 System setup 1	0	0	0	0	RST SYS	RAM CLR	OSC STP	TST MOD	_	<u> </u>	<u> </u>	<u> </u>	_	<u> </u>	<u> </u>	_
COMMAND 1 System setup 2	0	0	0	1			CLK MOD1		_	_	<u> </u>	<u> </u>	_	<u> </u>	<u> </u>	<u> </u>
COMMAND 2 Input control setup	0	0	1	0			DATA FMT		_	_	<u> </u>	<u> </u>	_	<u> </u>	<u> </u>	<u> </u>
COMMAND 3 General-purpose port control	0	0	1	1	PORT SET	OUT P11	OUT P10	OUT P9	_	-	<u> </u>	-	-	<u> </u>	-	-
COMMAND 4 Display operation control: reverse video and blinking	0	1 1	0	0	RVS ON	BLK	BLK	BLK 0	_	<u> </u>	<u> </u>	i ! ! —	_	: : : :	: : : :	: : : :
COMMAND 5 Display control: on/off settings for each output	0	1 1	0	1	DSP 4	DSP 3	DSP	DSP 1	_	<u> </u>	 —	- -	_	 	<u> </u>	<u> </u>
COMMAND 6 Output control: systems 3 and 4	0	1 1	1	0	DSPF SL34		¦ DSP ¦ GSG	DSP BSG	_	<u> </u>	<u> </u>	<u> </u>	_	<u> </u>	<u> </u>	<u> </u>
COMMAND 8 Display control: border	1	0	0	0	0	BKC R	BKC G	BKC B	BKO4 F1	BKO4 F0	BKO3 F1	BKO3 F0	BKO2 F1	BKO2 F0	BKO1 F1	BKO1 F0
COMMAND 9 Display start position	1	0	0	1	VP5	VP4	VP3	VP2	VP1	VP0	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND 10 Display line control	1	0	1	0	LNF SZ	LNF OT4	LNF OT3	LN SEL	0	0	LIN 126	LIN 115	LIN 104	LIN 93	LIN 82	LIN 71
COMMAND 11 RAM write address	1	0	1	1	VADR 3	VADR 2	VADR 1	VADR 0	0	0	0	HADR 4	HADR 3	HADR 2	HADR 1	HADR 0
COMMAND 14 Display RAM setup data	1	1	1	BLK	RV	R	G	В	C7	C6	C5	C4	СЗ	C2	C1	C0
	1										2					

- ① Command code: (These 4 bits in the first byte identify the command.)

 Command 14 is recognized by the upper 3 bits.
- 2 Command data: (These bits specify the data for each command.)
 - For commands 0 through 7, 8 bits of data are read in.
 - For commands 8 through 14, 16 bits of data are read in.
 - If the command 2 data-1 bit (DATAFMT) was set to 1, after the first byte of a command 14 is read in, the system goes to continuous transfer mode for reading in a series of following bytes.

Note: 1. If the \overline{CS} pin is set high, the command state is set to the command 0 (system control setup) state.

2. If a system reset is executed from the RST pin or by a command reset, the command register is set tot 0.

① COMMAND 0 (System control setup 1)

First byte

DAG 1 DA7	5		Register content														
DA0 to DA7	Register name	State	Function	Note													
7	_	0															
6	_	0	Command 0 identification code														
5	_	0	Command o identification code														
4	_	0															
3	RST		Normal operation	If $\overline{\text{CS}}$ is low, the reset is executed, but if													
3	SYS	1	System reset	CS is high this command will be excluded.													
2	RAM	0	Normal operation	The VRAM clear operation is not executed when the oscillator													
2	CLR	1	Normal operation VRAM clear (All data is set to FE (hexadecimal))	is stopped.													
4	osc	osc	osc	osc	OSC	osc	osc	osc	osc	osc	osc	osc	OSC	osc	0	The LC oscillator operating state is maintained.	Valid when the display is off. VRAM write is not possible when the oscillator is
'	STP	1	The LC oscillator is stopped.	stopped.													
0	TST	0	Normal operation	Illegal setting.													
0	MOD	1	Test mode	This bit must always be set to 0.													

Note: This register is set to 0 on a reset (either by the RST pin or by a command reset).

Notes on command settings

- RSTSYS: A command reset is executed immediately after the data is read.
 The reset is cleared by returning the CS pin to high to reset this register. The reset is also cleared if this command is executed consecutively or if this register is set to 0.
- RAMCLR: The RAM can only be erased when display is off. This operation is not executed during display. This
 operation cannot be executed if the LC oscillator is stopped. Only use this command when the LC oscillator is
 operating.
 - This command bit is automatically cleared when the RAM erase operation completes.
 - Once the RAM erase command has been read in, the following time is required to complete the operation.
 Tclear = 5 [μs] + 4/f_{OSC} (LC-oscillator) × 288
- 3. OSCSTP: The LC oscillator stop command stops the LC oscillator connected to pins 2 and 3 (OSC $_{IN}$ and OSC $_{OUT}$). The oscillator stop command is only executed when display is off. It is not executed if display is in progress.
 - In external clock input mode, this command stops the acquisition of that clock signal.
- 4. TSTMOD: The test mode command is executed if the TEST_{IN} pin (pin 5) is high. This command should not be used by applications in normal operation.

② COMMAND 1 (System control setup 2)

First byte

DAG 1 DA 7	D			Re	egister content	N.				
DA0 to DA7	Register name	State			Function	Note				
7	_	0								
6	_	0	Command	1 identified	tion and					
5	_	0	Command	i identifica	alion code					
4	_	1]							
3	0	HSYNC (pi signal inpu	,	ions as the horizontal synchronizing	The VSYNC pin (pin 21) must be tied to ground or V _{DD} in composite					
3	MOD	1	HSYNC (pi signal inpu	,	ions as the composite synchronizing	synchronizing signal input mode.				
2	CLK	0	The systen	n clock has	a positive polarity.	This sets the clock polarity for system operation when pin 2 is used as a clock				
2	POLT	1	The systen	n clock has	a negative polarity.	input.				
1	CLK	CLK	1 CLK	0	MOD1	MOD0	Operation	1		
	MOD1	1	0	0	LC oscillator mode	Valid when the CTRL1 pin (pin 4) is high.				
	CLK MOD0	CLK	CLK		0	1	Clock input (1 dot)	The input clock frequency in clock input mode is either 4fsc or the dot clock		
				CLK	CLK		CLK	0	1	0
0		1	1	1	Clock input (PAL)					

③ COMMAND 2 (Input control)

First byte

DAG - DAZ	5		Register content	N.		
DA0 to DA7	Register name	State	Function	Note		
7	_	0				
6	_	0	Command 2 identification code			
5	_	1	Confinance 2 Identification code			
4	_	0				
3	VSYN	0	The vertical synchronizing signal input polarity is low active.	Sets the pin 21 (VSYNC) signal input		
3	POLT	1	The vertical synchronizing signal input polarity is high active.	polarity.		
2	HSYN	0	The horizontal synchronizing signal input polarity is low active.	Sets the pin 22 (HSYNC) signal input		
2	POLT	1	The horizontal synchronizing signal input polarity is high active.	polarity.		
1	DATA FMT	DATA	DATA	0	Data is transferred in 16-bit units.	Sets the COMMAND 14 data transfer
·		1	Continuous transfers with the upper 8 bits input first and then the lower 8 bits	format.		
0	ATR 0		RV specifies the reverse video display function.	COMMAND-14 Data 11: Valid in RV		
U	FMT	1	RV specifies system 3 output control.	RGB output mode.		

④ COMMAND 3 (General-purpose port control)

First byte

D.1.0.1. D.1.7			Register content		
DA0 to DA7	Register name	State	Function	Note	
7	_	0			
6	_	0	Command 3 identification code		
5	_	1	Command 3 Identification code		
4	_	1			
3	PORT SET	PORT	0	System 4 functions as a normal character and border outputs.	Controls the pin 10 (BLK4) and pin 11
3		1	System 4 functions as general-purpose ports.	(CHA4) outputs.	
2	OUT	OUT	0	The pin 11 output is set to low.	Sets the output when PORTSET is
2	P11	1	The pin 11 output is set to high.	set to 1.	
4	OUT	0	The pin 10 output is set to low.	Sets the output when PORTSET is	
'	P10	1	The pin 10 output is set to high.	set to 1.	
0	OUT P9	0	The pin 9 output is set to low.	Sets the output for pin 9 during normal	
0		1	The pin 9 output is set to high.	operation (other than during a reset).	

⑤ COMMAND 4 (Display control: reverse video and blinking)

First byte

DA04- DA7	Danista a sama			Re	egister content	Nete
DA0 to DA7	Register name	State			Function	Note
7	_	0				
6	_	1	Command	1 identifies	ation code	
5	_	0	Command	4 Identifica	ation code	
4	_	0				
3	RVS	0	_			
3	ON	1	Characters in reverse		the attribute is specified are displayed	
0	BLK	0	_			
2	ON	1	Characters displayed I		the attribute is specified are	
		0				
1	BLK1		BLK1	BLK0	Operation	The blinking period setting
		1	0	0	V × 25 (PAL: 0.5 s)	The duty is 60% for all types.
			0	1	V × 30 (NTSC: 0.5 s)	Character display on: 60% Character display off: 40%
0		0	1	0	V × 50 (PAL: 1.0 s)	V: Vertical period
0	BLK0		1	1	V × 60 (NTSC: 1.0 s)	v. vertical period
		1				

⑥ COMMAND 5 (Display control: on/off settings for each output system)

First byte

DAG (DA7	D		Register content			
DA0 to DA7	Register name	State	Function	Note		
7	_	0				
6	_	1	Command 5 identification code			
5	_	0	Command 5 Identification code			
4	_	1				
3	3 DSP4		System 4 output off	Pin 10 (BLK4) and pin 11 (CHA4) output		
3	D3F4	D3F4	D3F4	1	System 4 output on	control
2	DSP3	DSD3	0	System 3 output off	Pin 14 (BLK3) and pin 15 (CHA3) output	
2		1	System 3 output on	control		
1	DSP2	0	System 2 output off	Pin 16 (BLK2) and pin 17 (CHA2) output control		
,	5012	1	System 2 output on	Invalid in RGB output mode.		
0	DSP1	0	System 1 (RGB) output off	Pin 18 (BLK1) and pin 19 (CHA1) output control		
		1	System 1 (RGB) output on	Functions as the RGB output control in RGB output mode.		

⑦ COMMAND 6 (Output control: systems 3 and 4 output control settings)

First byte

DA04- DA7	Danistan sama			Re	gister conte	Niete	
DA0 to DA7	Register name	State			Func	tion	Note
7	_	0					
6	_	1	Command	C identifica	tion anda		
5	_	1	Command	o identifica	lion code		
4	_	0					
3	DSPF	0	Sets the sy described to		put conditio	ns according to the command	Only system 4 is valid in 4-system output mode. System 4 cannot be set
3	SL34	1	Sets the sy described to		put conditio	when the general-purpose output port usage is specified.	
	DSP	0	DSPRSG	DSPGSG	DSPBSG	Output selection	
2	RSG	1	0	0	0	Signals other than R, G, B are output.	Note: The following registers are set to
			0	0	1	B is output.	1 during a reset. DSPRSG
	DSP	0	0	1	0	G is output.	DSPGSG
1	GSG	1	0	1	1	G and B are output.	DSPBSG
		'	1	0	0	R is output.	As a result, the "All of R, G, B are output" state is selected during a
		0	1	1 0 1 R		R and B are output.	reset.
0	DSP BSG		1 1 0 R and G are output.				
	250	1	1	1	1	All of R, G, B are output.	

First byte

DAO to DAZ	Dogistar nama			Re	gister cont	ent		Note		
DA0 to DA7	Register name	State			Fund	ction		Note		
7	_	1								
6	_	0	Commond	O identifica	tion anda					
5	_	0	Command	8 identifica	tion code					
4	_	0								
3		0	_							
2	BKCR	0	BKCR	BKCG	вксв	Background color	7			
2	BKCK	1	0	0	0	Black				
		'	0	0	1	Blue		Background color setting in RGB output		
		0	0	1	0	Green		mode		
1	BKCG		0	1	1	Cyan		This command is invalid in 4-system output mode.		
		1	1	0	0	Red		 Invalid when pin 20 (OUT_{MOD}) is high. 		
			1	0	1	Magenta		 Valid when pin 20 (OUT_{MOD}) is low. 		
	0 BKCB	0	1	1	0	Yellow				
		1	1	1	1					
		'								

Second byte

DA0 to DA7	Dogistar name			Re	egister content	Note				
DAU IO DA7	Register name	State			Function	Note				
7	BKO4	0	BKO4F1	BKO4F0	Operation function					
/	F1	1	0	0	No background or border					
		_ '	0	1	Font size (black characters)	The system 4 output border setting				
	DI/O	0	1	0	Border					
6	BKO4 F0		1	1	Areas other than the font (all filled)					
		1								
		0								
5	ВКО3	0	BKO3F1	BKO3F0	Operation function					
	F1	1	0	0	No background or border					
			0	1	Font size (black characters)	The system 3 output border setting				
	ВКО3	0	1	0	Border					
4	F0		1	1	Areas other than the font (all filled)					
		1								
3	BKO2 F1	0	BKO2F1	BKO2F0	Operation function	The system 2 output border setting				
		1	0	0	No background or border	This command is invalid in RGB output				
			0	1	Font size (black characters)	mode.				
0	BKO2	0	1	0	Border	 Invalid when pin 20 (OUT_{MOD}) is low. Valid when pin 20 (OUT_{MOD}) is high. 				
2	F0	1	11	1	Areas other than the font (all filled)]				
		<u>'</u>								
	DIVO	0								
1	BKO1 F1		BKO1F1	BKO1F0	Operation function					
		1	0	0	No background or border	The system 1 or RGB output border				
			0	1	Font size	setting				
0	BKO1	0	1	0	Border					
	F0	1	11	1	Areas other than the font (all filled)					
		<u>'</u>								

First byte

DAG 4- DAZ	Danistas sama		Register content	Note
DA0 to DA7	Register name	State	Function	Note
7	_	1		
6	_	0	Command 9 identification code	
5	_	0	Command 9 Identification code	
4	_	1		
3	VP5	0	If VS is the vertical display start position then: $VS = H \times (\sum_{n=0}^{5} 2^n VP_n) + 16H$	
3	VIS	1	n`= 0 Where H is horizontal period pulse period.	
2	VP4	0	HSYNC	
	VI 4	1		
1	VP3	0	vs	
'	VIS	1	VSYNC Character	
0	VP2	0	HS display area	
	V1 Z	1		

Second byte

DAG 1 DA 7	D		Register content	N .
DA0 to DA7	Register name	State	Function	Note
7	VP1	0		
,	VFI	1		
6	VP0	0		
0	VFO	1		
5	HP5	0		
J	111 3	1		
4	HP4	0	If VS is the horizontal display start position then:	
	111 4	1	$HS = Tc \times (\sum_{n=0}^{\infty} 2^{n}HP_{n}) + 12Tc$	
3	HP3	0	n=0	
	111 0	1	Where Tc is a single period of the LC oscillator connected to pins 2 and 3 (OSC _{IN} and OSC _{OUT}), or:	
2	HP2	0	Tc is the period of the input clock (4fsc input) if CTRL1 (pin 4) is	
	111 2	1	high.	
1	HP1	0	NTSC mode: 7.159 MHz = 4fsc × 1/2	
'	'	1	PAL mode: 7.094 MHz = $4 \text{fsc} \times 2/5$	
0	HP0	0		
	0	1		

(10) COMMAND 10 (Display line control)

First byte

DAG 1 DA7	5		Register content	N.		
DA0 to DA7	Register name	State	Function	Note		
7	_	1				
6	_	0	Command 10 identification code			
5	_	1	Command to identification code			
4	_	0				
2	LNF	0	_			
3	SZ	1	Sets the character size.			
2	LNF		_	Invalid in general-purpose port mode.		
2	OT4	1	Sets the system 4 display line.	invalid in general-purpose port mode.		
1	LNF	0	_	Invalid in system 4 output setup mode.		
'	OT3 1		Sets the system 3 display line.	invalid in system 4 output setup mode.		
0	LNF	0	The line specified by the next 6 bits is one of lines 1 to 6.	Controls the line switching specified by		
U	0 SEL		The line specified by the next 6 bits is one of lines 7 to 12.	the six bits in the second byte.		

Second byte

D. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	5		Register content					
DA0 to DA7	Register name	State	Function	Note				
7	_	0	_					
6	_	0	_					
5	LIN	0	Clears the line 6 (12) setting.					
Э	126	1	Sets line 6 (12).					
4	LIN	0	Clears the line 5 (11) setting.					
4	115	1	Sets line 5 (11).	The character size or display line				
3	LIN	0	Clears the line 4 (10) setting.	setting				
3	LIN 104	1	Sets line 4 (10).	0: Character size specification = norma				
2	LIN	0 — 0 — 0 Clears 1 Sets li 0 Clears	Clears the line 3 (9) setting.	Display line specification = off 1: Character size specification = double				
2	93	1	Sets line 3 (9).	size				
1	LIN	0	Clears the line 2 (8) setting.	Display line specification = on				
ı	82	1	Sets line 2 (8).					
0	LIN	0	Clears the line 1 (7) setting.					
U	71	1	Sets line 1 (7).]				

① COMMAND 11 (Display RAM write address setting)

First byte

D404 D45			Register content				
DA0 to DA7	Register name	State	Function	Note			
7	_	1					
6	_	0	Command 11 identification code				
5	_	1	Command 11 Identification code				
4	_	1					
3	VADR	0					
3	3	1					
2	VADR	0					
2	2	1	The range of the display RAM vertical address (line address)				
1	VADR	0	setting is from 0 to B (hexadecimal) (12 lines). Values of C (hexadecimal) or larger are not allowed.				
_ '	1	1	, , ,				
0	o VADR						
U	0	1					

Second byte

DAG 1 DA 7	D		Register content	
DA0 to DA7	Register name	State	Function	Note
7	_	0	_	
6	_	0	_	
5	_	0	_	
4	HADR	0		
4	4	1		
2	3 HADR	0		
3	3	1		
2	HADR	0	The range of the display RAM horizontal address (character address) setting is from 00 to 17 (hexadecimal) (24 characters).	
2	2	1	Values of 18 (hexadecimal) or larger are not allowed.	
4	HADR	0	, ,	
'	1	1		
0	HADR	0		
0	0	1		

② COMMAND 14 (Display RAM setup data)

First byte

DAG / DA7	D : .		Register content	N.
DA0 to DA7	Register name	State	Function	Note
7	_	1		
6	_	1	Command 14 identification code	
5	_	1		
4	BLK	0		
4	BLK	1	Blinking character specification	
3	D\/	RV 0 —		
3	KV	1	Reverse video character specification	
2	R 0		_	
2	K	1	R output specification (system 3 output in 4-system output mode)	
1	6	0	_	
'	1 G		G output specification (system 2 output in 4-system output mode)	
0	В	0	_	
U	В	1	B output specification (system 1 output in 4-system output mode)	

Second byte

DA04- DA7	Danistan		Register content	Nete
DA0 to DA7	Register name	State	Function	Note
7	C7	0		
,	C/	1		
6	C6	0		
0	00	1		
5	C5	0	Character code setting	
J	03	1	There are 256 characters (00 to FF hexadecimal).	
4	C4	0	FE hexadecimal is handled as blank data.	
7	04	1	Nothing is displayed, whatever the other conditions are set to.	
3	C3	0	FF hexadecimal functions as the transfer termination code for	
<u> </u>	00	1	character-code-only continuous transfers.	
2	C2	0	Continuous transfer mode is set up by setting the data 0 bit (DATAFMT) in COMMAND 2 to 1.	
	02	1	(DATAL WIT) III COMMAND 2 to 1.	
1	C1	0		
'	01	1		
0	CO	0		
		1		

Display Screen Organization

The display screen consists of 12 lines of 24 characters each.

Thus the maximum number of characters that can be displayed is 288 characters.

The display memory address consists of a line address (VADR0, VADR1, VADR2, and VADR3 representing values from 0 to B (hexadecimal)), and a column (character position) address (HADR0, HADR1, HADR2, HADR3, and HADR4 representing values from 0 to 17 (hexadecimal)).

Display Screen Organization (Display memory address)

| 00h
00h
00h | 2
01h
00h | 3
02h | 4 | 5 | 6 | 7
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| 00h | | 02h | | | | •
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 | 16
 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| | | 00h | 03h
00h | 04h
00h | 05h
00h | 06h
00h
 | 07h
00h

 | 08h
00h | 09h
00h
 | 0Ah
00h
 | 0Bh
00h
 | 0Ch
 | 0Dh
00h | 0Eh
00h
 | 0Fh
00h
 | 10h
00h | 11h
00h | 12h
00h | 13h
00h | 14h
00h | 15h
00h | 16h
00h | 17h
00h |
| | 01h | 02h | 03h | 04h | 05h | 06h
 | 07h

 | 08h | 09h
 | 0Ah
 | 0Bh
 | 0Ch
 | 0Dh | 0Eh
 | 0Fh
 | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h |
| 01h
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01h | 01h
02h | 01h
03h | 01h
04h | 01h
05h | 01h
06h
 | 01h
07h

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09h
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0Ah
 | 01h
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0Ch
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 | 01h
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 | 0Bh
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 | 0Fh
 | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h
0Bh |
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02h 02h 00h 01h 02h 03h 04h 05h 03h 03h 03h 03h 03h 03h 00h 01h 02h 03h 04h 05h 04h 04h 04h 04h 04h 04h 04h 06h 01h 02h 03h 04h 05h 05h 06h 05h 05h 05h 05h 05h 05h 06h 06h 06h 06h 06h 06h 06h 06h 06h <td>01h 01h 01h 01h 01h 01h 01h 00h 01h 02h 03h 04h 05h 06h 02h 02h 02h 02h 02h 02h 02h 00h 01h 02h 03h 04h 05h 06h 03h 03h 03h 03h 03h 03h 03h 00h 01h 02h 03h 04h 05h 06h 04h 04h 04h 04h 04h 04h 04h 04h 06h 04h 04h 04h 04h 04h 04h 04h 04h 06h 05h 05h 05h 05h 05h 05h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h 06h<td>01h 01h 01h 01h 01h 01h 01h 01h 00h 01h 02h 03h 03h 03h 03h 03h 03h 03h 03h 03h 04h 04h</td><td>01h 01h 08h 02h 03h 04h 04h<td>01h 01h 09h 02h 03h 04h 05h<td>01h 01h 02h 03h 03h<td>01h 01h 02h 03h 03h<td>01h 01h 02h 02h<td>01h 01h 02h 02h<td>01h 01h 02h 02h<td>01h 01h 02h 02h<td>01h 01h 02h 02h<td>01h 01h 11h 02h 02h</td><td>01h 01h 01h 01h 01h 01h 01h 01h 01h 01h</td><td>01h 01h 01h 01h 01h 01h 01h 01h 01h 01h</td><td>01h 01h 01h 01h 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H-address (horizontal address: in hexadecimal)

V-address (vertical address: in hexadecimal)

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