# MC10H601, MC100H601

# 9-Bit ECL to TTL Translator

### Description

The MC10H/100H601 is a 9-bit, dual supply ECL to TTL translator. Devices in the ON Semiconductor 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. For the 3-state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

The 10H version is compatible with MECL 10H<sup>™</sup> ECL logic levels. The 100H version is compatible with 100K levels.

### Features

- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- ECL and TTL 3-State Control Inputs
- Dual Supply
- 4.8 ns Max Delay into 50 pF, 9.6 ns into 200 pF (all Outputs Switching)
- PNP TTL Inputs for Low Loading
- Pb-Free Packages are Available\*



## **ON Semiconductor®**

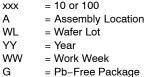
http://onsemi.com



PLCC-28 FN SUFFIX CASE 776

### **MARKING DIAGRAM\***





\*For additional marking information, refer to Application Note AND8002/D.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

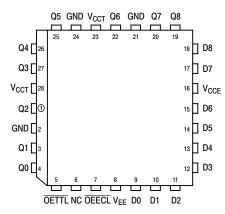


Figure 1. PLCC-28 Pinout (Top View)

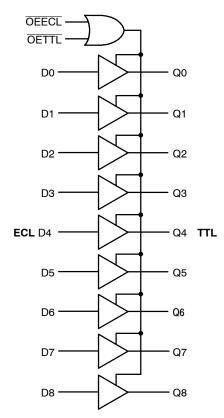


Figure 2. Logic Diagram

Table 1. PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V <sub>CCE</sub>	ECL V <sub>CC</sub> (0 V)
V <sub>CCT</sub>	Supply (+5.0 V)
V <sub>EE</sub>	ECL Supply (-5.2 /-4.5 V)
D0-D8	Data Inputs (ECL)
Q0-Q8	Data Outputs (TTL)
OEECL	3-State Control (ECL)
OETTL	3-State Control (TTL)

Table 2. TRUTH TABLE

OEECL	OETTL	D	Q
L	L	L	L
L	L	н	н
н	Х	х	Z
Х	Н	Х	Z

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		0°C		25°C		85°C		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
I <sub>EE</sub>	Power Supply Current		-51		-51		-51	mA
I <sub>INH</sub> I <sub>INL</sub>	Input HIGH Current Input LOW Current	0.5	255	0.5	175	0.5	175	μΑ μΑ
V <sub>IH</sub> V <sub>IL</sub>	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1060 -1950	-720 -1445	mV

## Table 3. 10H ECL DC CHARACTERISTICS: V<sub>CCT</sub> = 5.0 V $\pm$ 10%; V<sub>EE</sub> = – 5.2 V $\pm$ 5%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

### Table 4. 100H ECL DC CHARACTERISTICS: V<sub>CCT</sub> = 5.0 V $\pm$ 10%; V<sub>EE</sub> = -4.2 V to -5.5 V

			0°C		25°C		85°C	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
I <sub>EE</sub>	Power Supply Current		-51		-51		-53	mA
I <sub>INH</sub> I <sub>INL</sub>	Input HIGH Current Input LOW Current	0.5	255	0.5	175	0.5	175	μΑ μΑ
V <sub>IH</sub> V <sub>IL</sub>	Input HIGH Voltage Input LOW Voltage	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

## Table 5. TTL DC CHARACTERISTICS: V<sub>CCT</sub> = 5.0 V $\pm$ 10%; V<sub>EE</sub> = -5.2 V $\pm$ 5% (10H version);

 $V_{EE} = -4.2 \text{ V to } -5.5 \text{ V}$  (100H version)

			0	°C	25	°C	85	°C	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Unit
I <sub>CCH</sub>	Power Supply Current			110		110		110	mA
I <sub>CCL</sub>				110		110		110	
I <sub>CCZ</sub>	Power Supply Current			105		105		105	
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.7 V V <sub>IN</sub> = 7.0 V		20 100		20 100		20 100	μΑ
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.5 V		-0.6		-0.6		-0.6	mA
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0 V	-100	-225	-100	-225	-100	-225	mA
I <sub>OZH</sub> I <sub>OZL</sub>	Output Disable Current HIGH Output Disable Current LOW	V <sub>OUT</sub> = 2.7 V V <sub>OUT</sub> = 0.5 V	-50	50	-50	50	-50	50	μΑ
V <sub>IHT</sub> V <sub>ILT</sub>	Input HIGH Voltage Input LOW Voltage		2.0	0.8	2.0	0.8	2.0	0.8	V
V <sub>OHT</sub>	Output HIGH Voltage	I <sub>OH</sub> = −3.0 mA I <sub>OH</sub> = −15 mA	2.5 2.0		2.5 2.0		2.5 2.0		V
V <sub>OLT</sub>	Output LOW Voltage	I <sub>OL</sub> = 48 mA		0.55		0.55		0.55	V
V <sub>IK</sub>	Input Clamp Voltage	I <sub>IN</sub> = –18 mA		-1.2		-1.2		-1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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				<b>0</b> °	°C	25	°C	85	°C	
Symbol	Parameter		Condition	Min	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output		C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	ns ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	OEECL	C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF	3.7 5.4	6.5 13	3.7 5.4	6.5 13	3.7 5.4	6.5 13	ns ns
t <sub>PLZ</sub> t <sub>PHZ</sub>		OETTL	C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF	4.3 7.0	7.5 15	4.3 7.0	7.5 15	4.3 7.0	7.5 15	ns ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	OEECL	C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF	3.5 5.0	6.0 12	3.5 5.0	6.0 12	3.5 5.0	6.0 12	ns ns
t <sub>PZL</sub> t <sub>PZH</sub>		OETTL	C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF	4.2 6.0	7.0 14	4.2 6.0	7.0 14	4.2 6.0	7.0 14	ns ns
t <sub>R</sub> t <sub>F</sub>	Output Rise/Fall Time 1.0 V-2.0 V		C <sub>L</sub> = 50 pF C <sub>L</sub> = 200 pF		1.2 3.0		1.2 3.0		1.2 3.0	ns ns

Table 6. AC CHARACTERISTICS:  $V_{CCT} = 5.0 \text{ V} \pm 10\%$ ;  $V_{EE} = -5.2 \text{ V} \pm 5\%$  (10H version);  $V_{EE} = -4.2 \text{ V}$  to -5.5 V (100H version)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

#### **ORDERING INFORMATION**

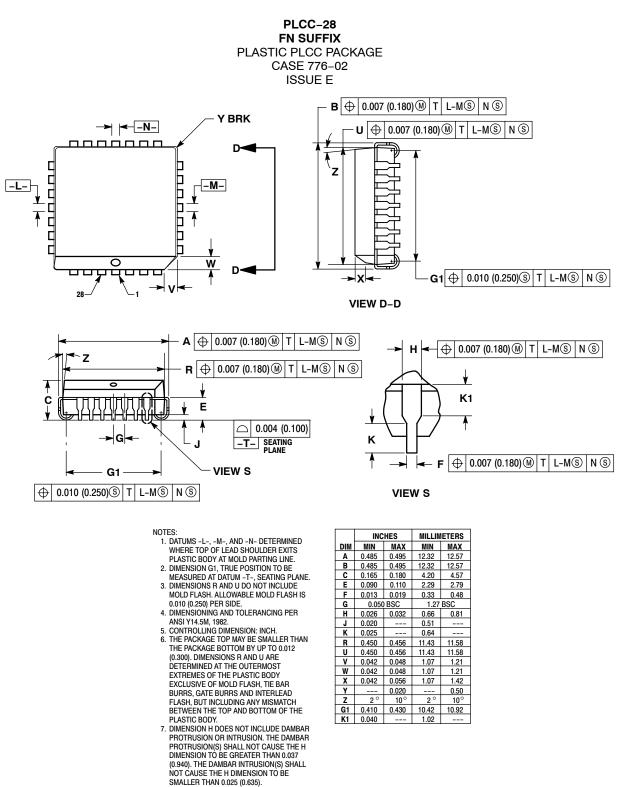
Device	Package	Shipping <sup>†</sup>
MC10H601FN	PLCC-28	37 Units / Rail
MC10H601FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10H601FNR2	PLCC-28	500 / Tape & Reel
MC10H601FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel
MC100H601FN	PLCC-28	37 Units / Rail
MC100H601FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC100H601FNR2	PLCC-28	500 / Tape & Reel
MC100H601FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **Resource Reference of Application Notes**

AN1405/D	-	ECL Clock Distribution Techniques
AN1406/D	-	Designing with PECL (ECL at +5.0 V)
AN1503/D	_	ECLinPS <sup>™</sup> I/O SPiCE Modeling Kit
AN1504/D	_	Metastability and the ECLinPS Family
AN1568/D	_	Interfacing Between LVDS and ECL
AN1672/D	_	The ECL Translator Guide
AND8001/D	-	Odd Number Counters Design
AND8002/D	_	Marking and Date Codes
AND8020/D	_	Termination of ECL Logic Devices
AND8066/D	-	Interfacing with ECLinPS
AND8090/D	_	AC Characteristics of ECL Devices

### PACKAGE DIMENSIONS



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