2N6052

Preferred Device

Darlington Complementary Silicon Power Transistors

This package is designed for general−purpose amplifier and low frequency switching applications.

Features

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector−Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- This is a Pb−Free Device*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous Peak	I_C	12 20	Adc
Base Current	I_B	0.2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.17	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Indicates JEDEC Registered Data.

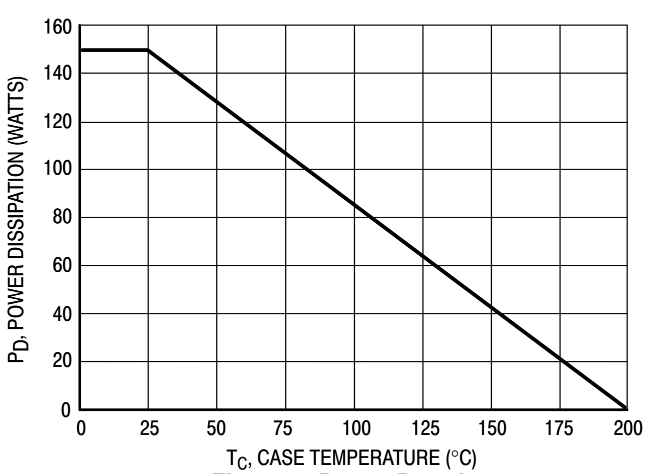
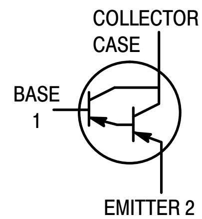


Figure 1. Power Derating

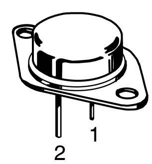
ON Semiconductor®

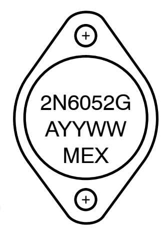
http://onsemi.com

12 AMPERE COMPLEMENTARY SILICON POWER TRANSISTOR 100 VOLTS, 150 WATTS



MARKING DIAGRAM





TO−204AA (TO−3)
CASE 1−07
STYLE 1

2N6052	=	Device Code
G	=	Pb−Free Package
A	=	Location Code
YY	=	Year
WW	=	Work Week
MEX	=	Country of Orgin

ORDERING INFORMATION

Device	Package	Shipping
2N6052G	TO−3 (Pb−Free)	100 Units/Tray

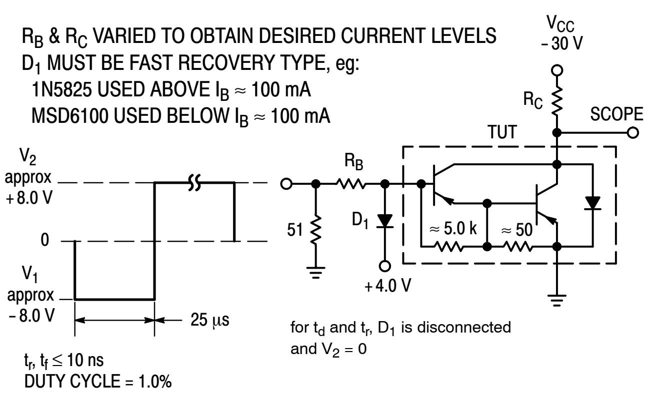
Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 3)	(I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current	(V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
	(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)		–	0.5	
	(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	5.0	
Emitter Cutoff Current	(V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain		h_{FE}			–
	(I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		750	18,000	
	(I_C = 12 Adc, V_{CE} = 3.0 Vdc)		100	–	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
	(I_C = 6.0 Adc, I_B = 24 mAdc)		–	2.0	
	(I_C = 12 Adc, I_B = 120 mAdc)		–	3.0	
Base−Emitter Saturation Voltage	(I_C = 12 Adc, I_B = 120 mAdc)	$V_{BE(sat)}$	–	4.0	Vdc
Base−Emitter On Voltage	(I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small−Signal Short Circuit Forward Current Transfer Ratio	(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	4.0	–	MHz
Output Capacitance	(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	500	pF
Small−Signal Current Gain	(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	–	–

2. Indicates JEDEC Registered Data.
3. Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

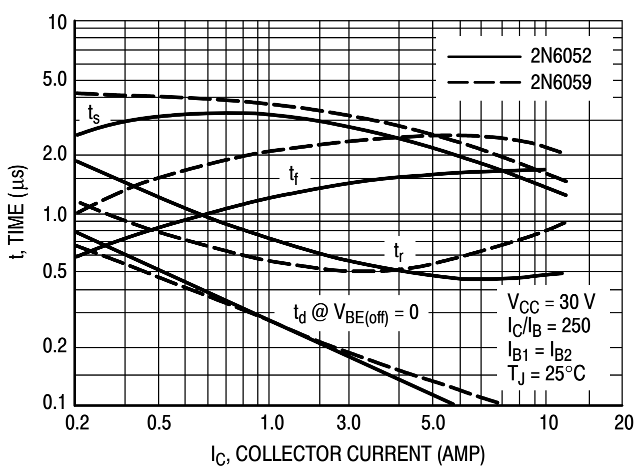


Figure 3. Switching Times

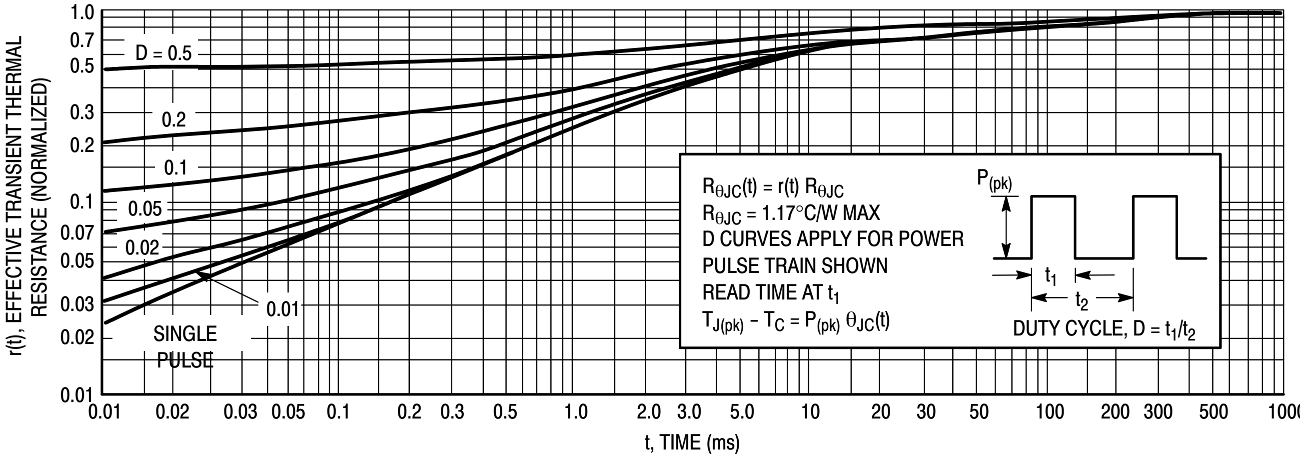


Figure 4. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, and 6 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

ACTIVE−REGION SAFE OPERATING AREA

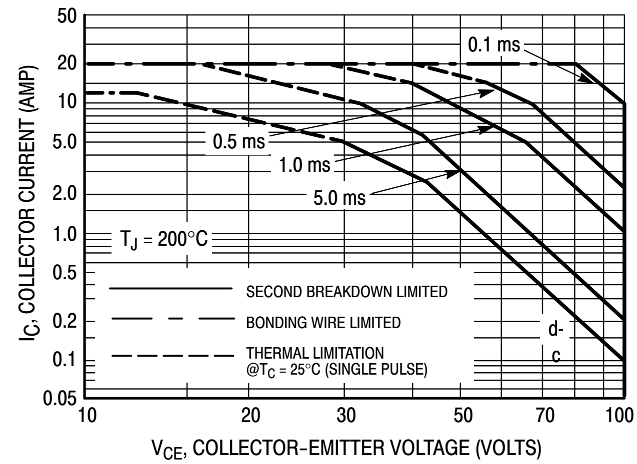


Figure 5.

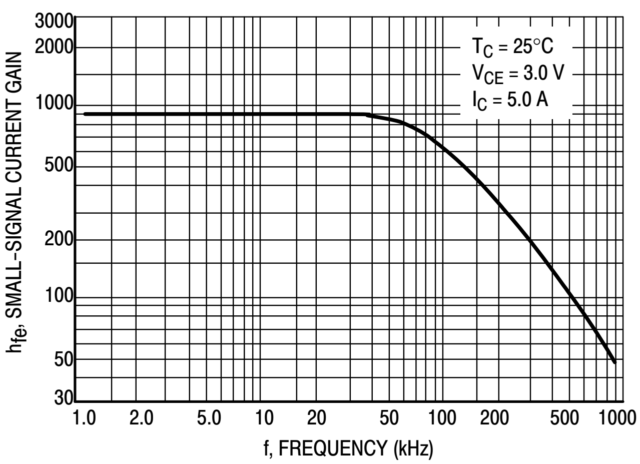


Figure 6. Small−Signal Current Gain

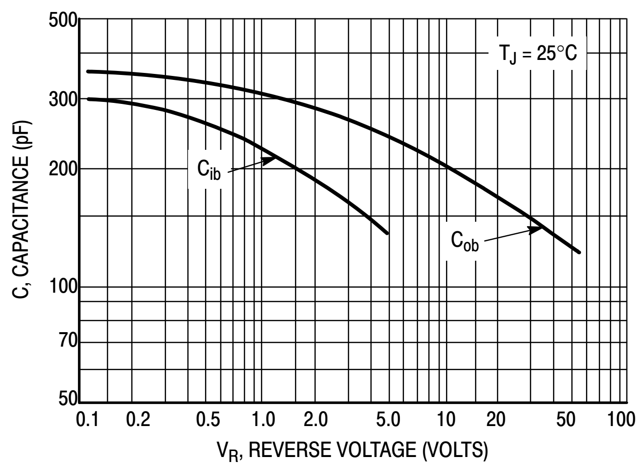


Figure 7. Capacitance

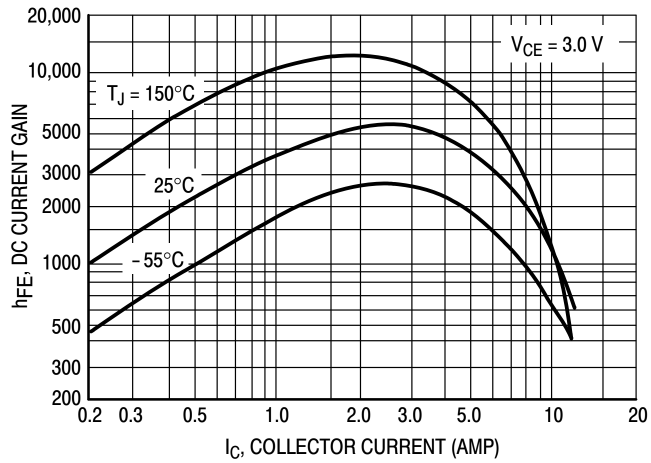


Figure 8. DC Current Gain

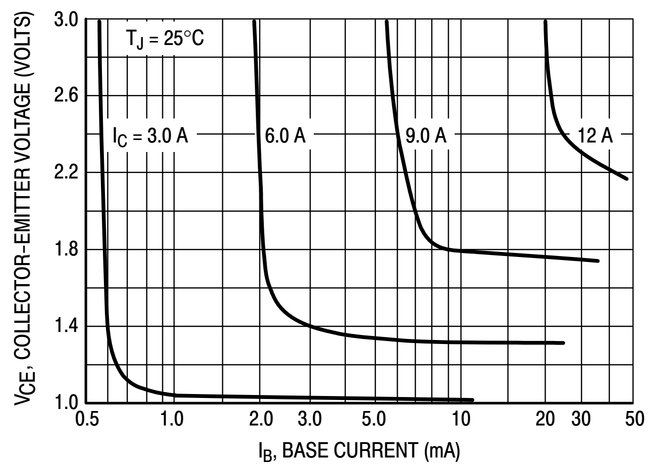


Figure 9. Collector Saturation Region

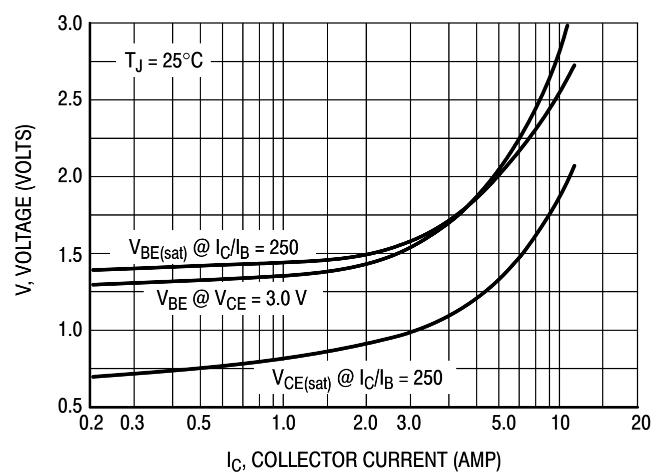
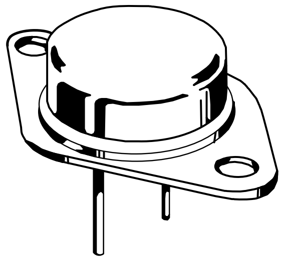


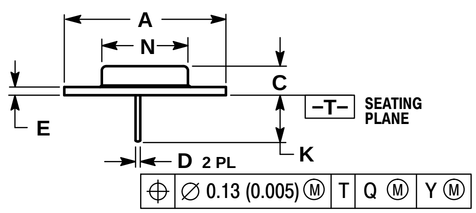
Figure 10. “On” Voltages

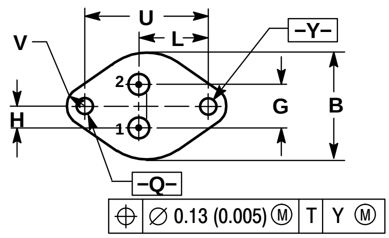
TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



SCALE 1:1





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊