

MCR12LD, MCR12LM, MCR12LN

Preferred Device

Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half-wave, silicon gate-controlled devices are needed.

Features

- Blocking Voltage to 800 Volts
- On-State Current Rating of 12 Amperes RMS at 80°C
- High Surge Current Capability – 100 Amperes
- Rugged, Economical TO-220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- High Immunity to dv/dt – 100 V/μsec Minimum at 125°C
- Pb-Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T _J = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM} , V _{RRM}	400 600 800	V
On-State RMS Current (180° Conduction Angles; T _C = 80°C)	I _{T(RMS)}	12	A
Average On-State Current (180° Conduction Angles; T _C = 80°C)	I _{T(AV)}	7.6	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T _J = 125°C)	I _{TSM}	100	A
Circuit Fusing Consideration (t = 8.3 ms)	I ² t	41	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs, T _C = 80°C)	P _{GM}	5.0	W
Forward Average Gate Power (t = 8.3 ms, T _C = 80°C)	P _{G(AV)}	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T _C = 80°C)	I _{GM}	2.0	A
Operating Junction Temperature Range	T _J	-40 to 125	°C
Storage Temperature Range	T _{stg}	-40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

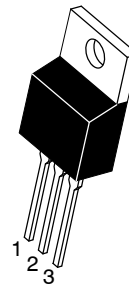
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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SCRs
12 AMPERES RMS
400 thru 800 VOLTS



TO-220AB
CASE 221A-09
STYLE 3

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
x = D, M, or N
G = Pb-Free Package
AKA = Diode Polarity

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
MCR12LD	TO-220AB	50 Units / Rail
MCR12LDG	TO-220AB (Pb-Free)	50 Units / Rail
MCR12LM	TO-220AB	50 Units / Rail
MCR12LMG	TO-220AB (Pb-Free)	50 Units / Rail
MCR12LN	TO-220AB	50 Units / Rail
MCR12LNG	TO-220AB (Pb-Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}C/W$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ($V_D = \text{Rated } V_{DRM}$ and V_{RRM} ; Gate Open)	$T_J = 25^{\circ}C$	I_{DRM}	-	-	0.01	mA
	$T_J = 125^{\circ}C$	I_{RRM}	-	-	2.0	

ON CHARACTERISTICS

Peak Forward On-State Voltage (Note 2) ($I_{TM} = 24 A$)	V_{TM}	-	-	2.2	V
Gate Trigger Current (Continuous dc) ($V_D = 12 V$, $R_L = 100 \Omega$)	I_{GT}	2.0	4.0	8.0	mA
Holding Current ($V_D = 12 V$, Gate Open, Initiating Current = 200 mA)	I_H	4.0	10	20	mA
Latch Current ($V_D = 12 V$, $I_g = 20 mA$)	I_L	6.0	12	30	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 V$, $R_L = 100 \Omega$)	V_{GT}	0.5	0.65	0.8	V

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Waveform, Gate Open, $T_J = 125^{\circ}C$)	dv/dt	100	250	-	$V/\mu s$
Critical Rate of Rise of On-State Current $I_{PK} = 50 A$; $P_w = 40 \mu sec$; $di/dt = 1 A/\mu sec$, $I_{gt} = 50 mA$	di/dt	-	-	50	$A/\mu s$

2. Indicates Pulse Test: Pulse Width $\leq 1.0 ms$, Duty Cycle $\leq 2\%$.

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Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

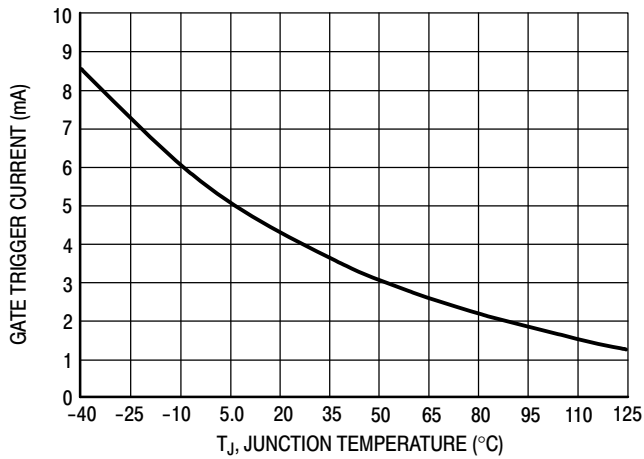
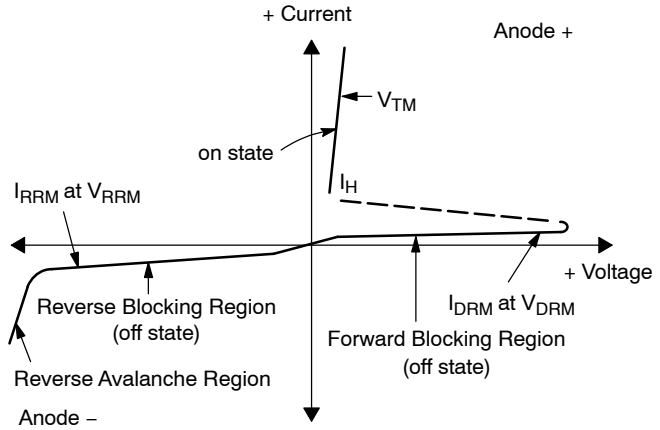


Figure 1. Typical Gate Trigger Current versus Junction Temperature

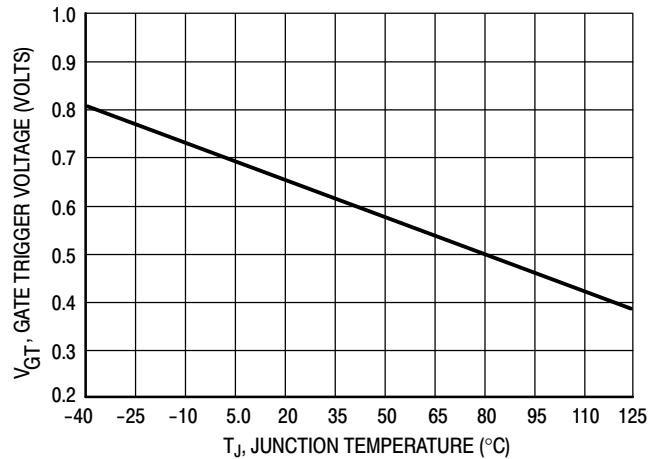


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

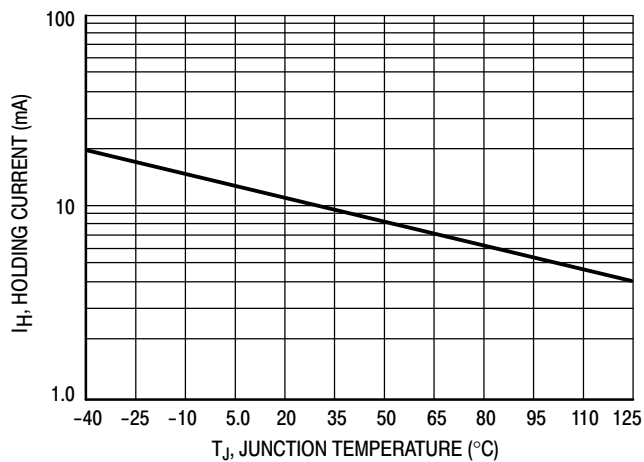


Figure 3. Typical Holding Current versus Junction Temperature

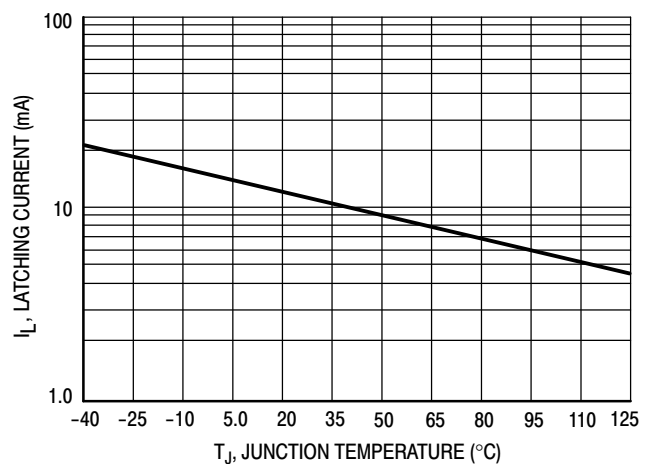


Figure 4. Typical Latching Current versus Junction Temperature

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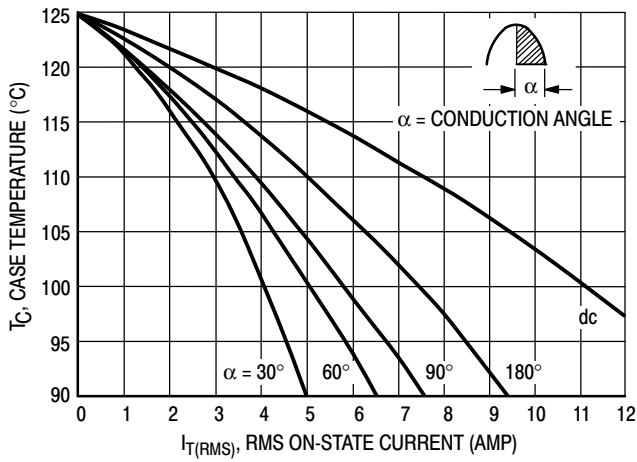


Figure 5. Typical RMS Current Derating

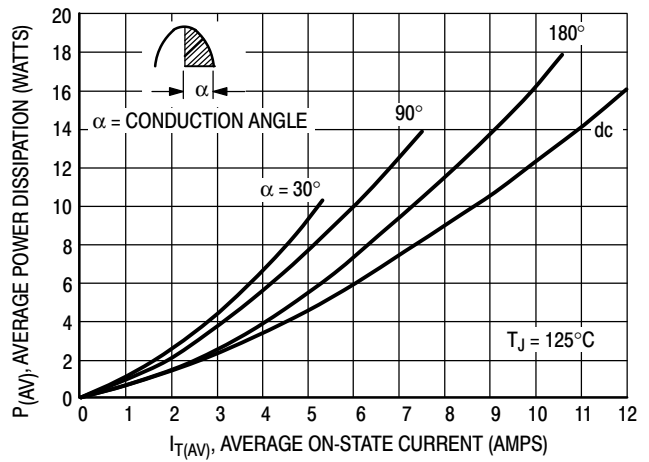


Figure 6. On-State Power Dissipation

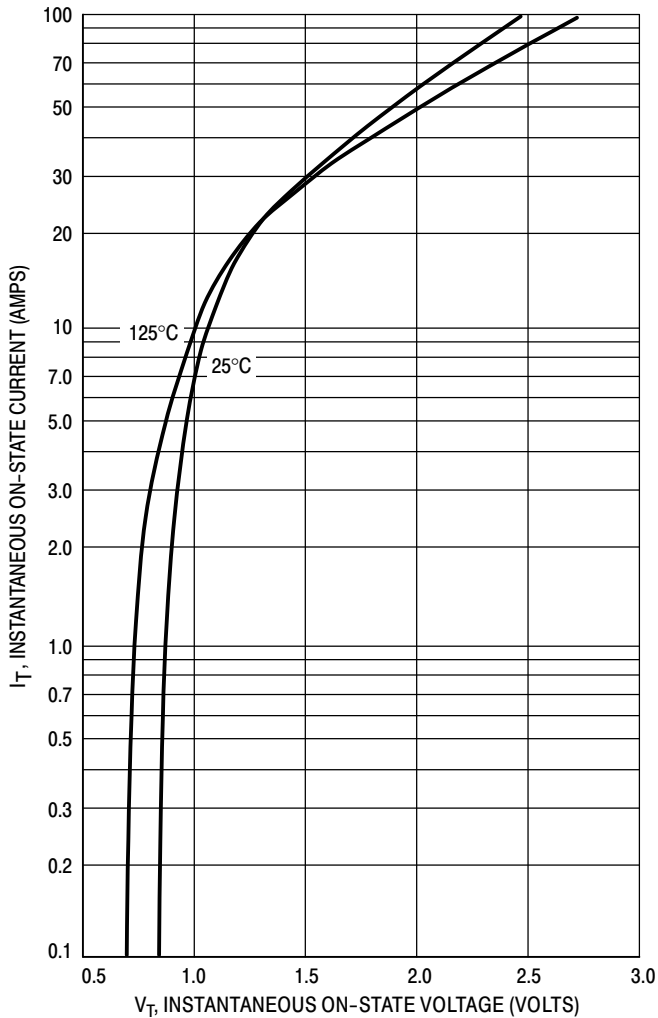


Figure 7. Typical On-State Characteristics

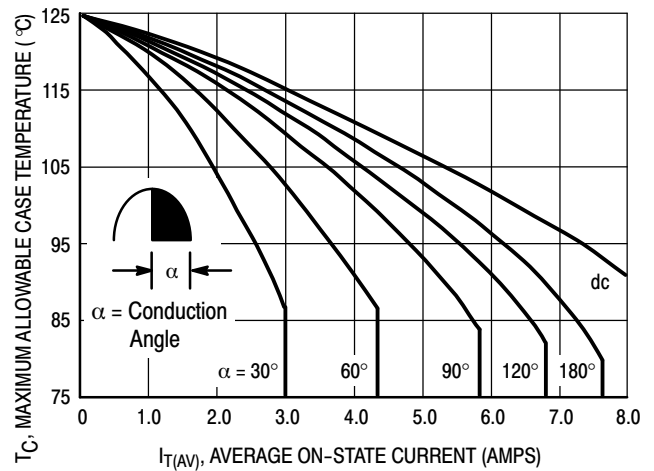
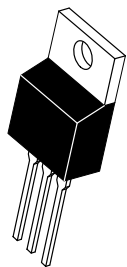


Figure 8. Average Current Derating

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

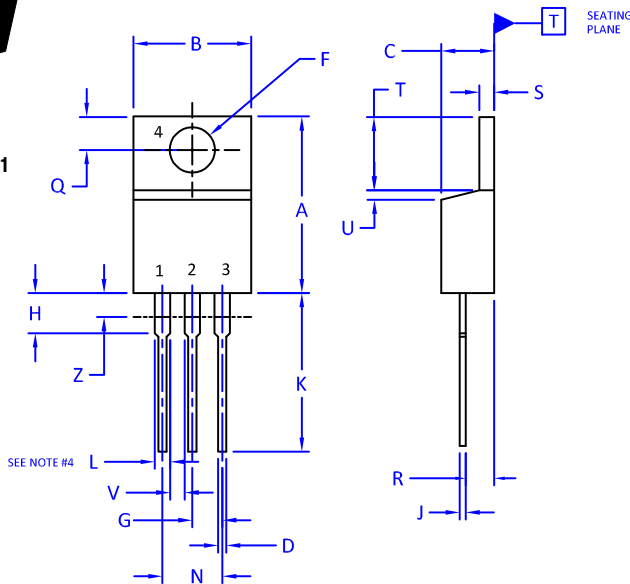
ON Semiconductor®



SCALE 1:1

TO-220 CASE 221A-09 ISSUE AJ

DATE 05 NOV 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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