High Speed 3-Channel Digital Isolator

NCID9301, NCID9311

Description

The NCID9301 and NCID9311 are galvanically isolated high−speed 3−channel digital isolator with output enable. This device supports isolated communications thereby allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages.

It utilizes **onsemi's** patented galvanic off−chip capacitor isolation technology and optimized IC design to achieve high insulation and high noise immunity, characterized by high common mode rejection and power supply rejection specifications. The thick ceramic substrate yields capacitors with ~25 times the thickness of thin film on−chip capacitors and coreless transformers. The result is a combination of the electrical performance benefits that digital isolators offer with the safety reliability of a >0.5 mm insulator barrier similar to what has historically been offered by optocouplers.

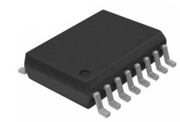
The device is housed in a 16−pin wide body small outline package.

Features

- Off−Chip Capacitive Isolation to Achieve Reliable High Voltage Insulation
  - DTI (Distance Through Insulation): ≥ 0.5 mm
  - Maximum Working Insulation Voltage: 2000 V_{peak}
- Bi−directional Communication
- 100 kV/μs Minimum Common Mode Rejection
- 8 mm Creepage and Clearance Distance to Achieve Reliable High Voltage Insulation
- Specifications Guaranteed Over 2.5 V to 5.5 V Supply Voltage and −40°C to 125°C Extended Temperature Range
- Over Temperature Detection
- Output Enable Function (Primary and Secondary side)
- NCIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable (Pending)
- Safety and Regulatory Approvals
  - UL1577, 5000 V_{RMS} for 1 Minute
  - DIN EN/IEC 60747−17 (Pending)

Typical Applications

- Isolated PWM Control
- Industrial Fieldbus Communications
- Microprocessor System Interface (SPI, I^2C, etc.)
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator



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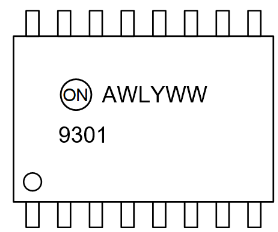
MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot / Assembly Lot
Y	= Year
WW	= Work Week
9301 / 9311	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

January, 2022 − Rev. 0

Publication Order Number:
NCID9301/D

BLOCK DIAGRAM

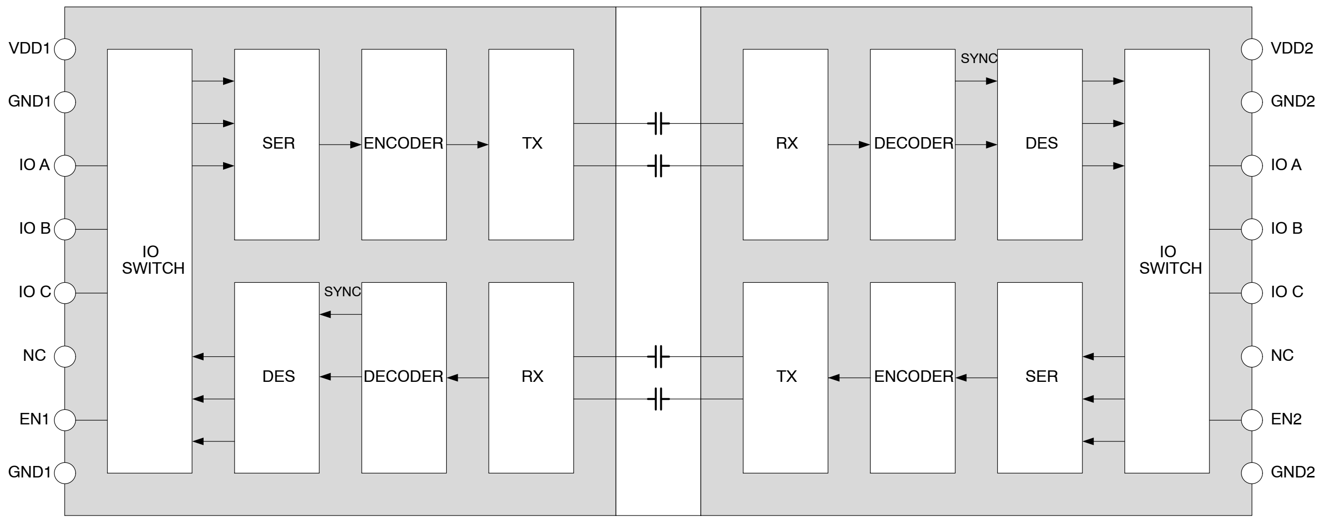


Figure 1. Functional Block Diagram

PIN CONFIGURATION

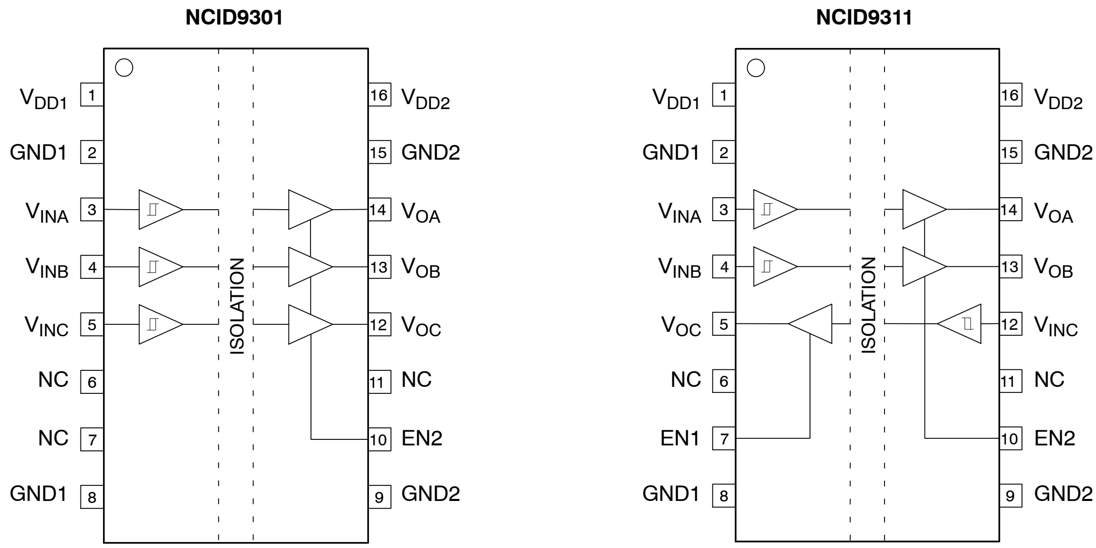


Figure 2. Pin and Channel Configuration

PIN DEFINITIONS

Name	Pin No. NCID9301	Pin No. NCID9311	Description
V_{DD1}	1	1	Power Supply, Side 1
GND1	2	2	Ground Connection for V_{DD1}
V_{INA}	3	3	Input, Channel A
V_{INB}	4	4	Input, Channel B
V_{INC}	5	12	Input, Channel C
NC	6	6	No Connect
EN1	–	7	Output Enable 1
NC	7	–	No Connect
GND1	8	8	Ground Connection for V_{DD1}
GND2	9	9	Ground Connection for V_{DD2}
EN2	10	10	Output Enable 2
NC	11	11	No Connect
V_{OC}	12	5	Output, Channel C
V_{OB}	13	13	Output, Channel B
V_{OA}	14	14	Output, Channel A
GND2	15	15	Ground Connection for V_{DD2}
V_{DD2}	16	16	Power Supply, Side 2

SPECIFICATIONS

TRUTH TABLE (Note 1)

V_{INX}	EN_X	V_{DDI}	V_{DDO}	V_{OX}	Comment
H	H/NC	Power Up	Power Up	H	Normal Operation
L	H/NC	Power Up	Power Up	L	Normal Operation
X	L	Power Up	Power Up	Hi−Z	
X	H/NC	Power Down	Power Up	L	Default low; V_{OX} return to normal operation when V_{DDI} change to Power Up
X	H/NC	Power Up	Power Down	Undetermined (Note 2)	V_{OX} return to normal operation when V_{DDO} change to Power Up

1. VINX = Input signal of a given channel (A, B or C). EN_X = Enable pin for primary or secondary side (1 or 2). V_{OX} = Output signal of a given channel (A, B or C). V_{DDI} = Input−side V_{DD}. V_{DDO} = Output−side V_{DD}. X = Irrelevant. H = High level. L = Low level. NC = No Connection.
2. The outputs are in undetermined state when V_{DDO} < V_{UVLO}.

SAFETY AND INSULATION RATINGS

As per DIN EN/IEC 60747−17, this digital isolator is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.

Symbol	Parameter		Min	Typ	Max	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	–	I–IV	–	
		< 300 V_{RMS}	–	I–IV	–	
		< 450 V_{RMS}	–	I–IV	–	
		< 600 V_{RMS}	–	I–IV	–	
		< 1000 V_{RMS}	–	I–III	–	
	Climatic Classification		–	40/125/21	–	
	Pollution Degree (DIN VDE 0110/1.89)		–	2	–	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	–	–	
V_{PR}	Input−to−Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		3750	–	–	V_{peak}
	Input−to−Output Test Voltage, Method a, $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC		3200	–	–	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage		2000	–	–	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage		8000	–	–	V_{peak}
E_{CR}	External Creepage		8.0	–	–	mm
E_{CL}	External Clearance		8.0	–	–	mm
DTI	Insulation Thickness		0.50	–	–	mm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		150	–	–	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		100	–	–	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		600	–	–	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	–	–	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−55 to +150	°C
T_{OPR}	Operating Temperature	−40 to +125	°C
T_J	Junction Temperature	−40 to +150	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	°C
V_{DD}	Supply Voltage (V_{DDx})	−0.5 to 6	V
V	Voltage (V_{INx}, V_{Ox}, ENx)	−0.5 to 6	V
I_O	Average Output Current	10	mA
PD	Power Dissipation	210	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+125	°C
V_{DD1} V_{DD2}	Supply Voltage (Notes 3, 4)	2.5	5.5	V
V_{INH}	High Level Input Voltage	0.7 × V_{DDI}	V_{DDI}	V
V_{INL}	Low Level Input Voltage	0	0.1 × V_{DDI}	V
V_{UVLO+}	Supply Voltage UVLO Rising Threshold	2.2	–	V
V_{UVLO-}	Supply Voltage UVLO Falling Threshold	2.0	–	V
$UVLO_{HYS}$	Supply Voltage UVLO Hysteresis	0.1	–	V
I_{OH}	High Level Output Current	−2	–	mA
I_{OL}	Low Level Output Current	–	2	mA
DR	Signaling Rate	0	15	Mbps

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. During power up or down, ensure that both the input and output supply voltages reach the proper recommended operating voltages to avoid any momentary instability at the output state.
4. For reliable operation at recommended operating conditions, V_{DD} supply pins require at least a pair of external bypass capacitors, placed within 2 mm from V_{DD} pins 1 and 16 and GND pins 2 and 15. Recommended values are 0.1 μF and 1 μF.

ISOLATION CHARACTERISTICS

Apply over all recommended conditions. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} ≤ 10 μA, 50 Hz (Notes 5, 6, 7)	5000	–	–	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 5)	–	10^{11}	–	
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, Frequency = 1.0 MHz (Note 5)	–	1	–	pF

5. Device is considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
6. 5,000 V_{RMS} for 1−minute duration is equivalent to 6,000 V_{RMS} for 1−second duration.
7. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN EN/IEC 60747−17 Safety and Insulation Ratings Table on page 4.

ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, T_A =−40°C to +125°C, V_{DD1} = V_{DD2} = 2.5 V to 5.5 V, unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, I_{OH} = −4 mA	4.5	4.8	–	V	11
		V_{DD} = 3.3 V, I_{OH} = −2 mA	2.9	3.2			
		V_{DD} = 2.5 V, I_{OH} = −1 mA	2.1	2.4			
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, I_{OL} = 4 mA	–	0.1	0.4	V	12
		V_{DD} = 3.3 V, I_{OL} = 2 mA					
		V_{DD} = 2.5 V, I_{OL} = 1 mA					
V_{INT+}	Rising Input Voltage Threshold		–	–	$0.7 \times V_{DDI}$	V	
V_{INT-}	Falling Input Voltage Threshold		$0.1 \times V_{DDI}$	–	–	V	
$V_{INT(HYS)}$	Input Threshold Voltage Hysteresis		$0.1 \times V_{DDI}$	$0.2 \times V_{DDI}$	–	V	
I_{INH}	High Level Input Current	$V_{IH} = V_{DDI}$	–	–	1	μA	
I_{INL}	Low Level Input Current	V_{IL} = 0 V	−1	–	–	μA	
CMTI	Common Mode Transient Immunity	$V_I = V_{DDI}$ or 0 V, V_{CM} = 1500 V	100	150	–	kV/μs	16
C_{IN}	Input Capacitance	$V_{IN} = V_{DDI}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{DD} = 5 V	–	2	–	pF	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SUPPLY CURRENT CHARACTERISTICS

Apply over all recommended conditions, T_A =−40°C to +125°C unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
I_{DD1}	DC Supply Current	V_{DD} = 5 V, EN = 0/5 V, V_{IN} = 0/5 V	–	8.6	11.1	mA	
I_{DD2}				9.4	12.1		
I_{DD1}		V_{DD} = 3.3 V, EN = 0/3.3 V, V_{IN} = 0/3.3 V		8.3	10.8		
I_{DD2}				9.2	11.8		
I_{DD1}		V_{DD} = 2.5 V, EN = 0/2.5 V, V_{IN} = 0/2.5 V		8.2	10.6		
I_{DD2}				9.2	11.6		
I_{DD1}	AC Supply Current 1 Mbps	V_{DD} = 5 V, EN = 5 V, C_L = 15 pF, V_{IN} = 5 V Square Wave	–	8.5	11.1	mA	3, 4, 5, 6
I_{DD2}				9.6	12.1		
I_{DD1}		V_{DD} = 3.3 V, EN = 3.3 V, C_L = 15 pF, V_{IN} = 3.3 V Square Wave		8.5	10.8		
I_{DD2}				9.3	11.8		
I_{DD1}		V_{DD} = 2.5 V, EN = 2.5 V, C_L = 15 pF, V_{IN} = 2.5 V Square Wave		8.2	10.6		
I_{DD2}				9.2	11.6		
I_{DD1}	AC Supply Current 10 Mbps	V_{DD} = 5 V, EN = 5 V, C_L = 15 pF, V_{IN} = 5 V Square Wave	–	9.8	12.4	mA	
I_{DD2}				12.0	14.5		
I_{DD1}		V_{DD} = 3.3 V, EN = 3.3 V, C_L = 15 pF, V_{IN} = 3.3 V Square Wave		9.1	11.4		
I_{DD2}				10.6	13.1		
I_{DD1}		V_{DD} = 2.5 V, EN = 2.5 V, C_L = 15 pF, V_{IN} = 2.5 V Square Wave		8.7	11.1		
I_{DD2}				10.2	12.6		
I_{DD1}	AC Supply Current 15 Mbps	V_{DD} = 5 V, EN = 5 V, C_L = 15 pF, V_{IN} = 5 V Square Wave	–	10.4	13.0	mA	
I_{DD2}				13.2	15.7		
I_{DD1}		V_{DD} = 3.3 V, EN = 3.3 V, C_L = 15 pF, V_{IN} = 3.3 V Square Wave		9.5	11.8		
I_{DD2}				11.3	13.8		
I_{DD1}		V_{DD} = 2.5 V, EN = 2.5 V, C_L = 15 pF, V_{IN} = 2.5 V Square Wave		9.0	11.4		
I_{DD2}				10.7	13.1		

SWITCHING CHARACTERISTICS – NCID9301

Apply over all recommended conditions, T_A =−40°C to +125°C unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Ch	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay to Logic Low Output (Note 8)	All	V_{DD} = 5 V, C_L = 15 pF	–	115	170	ns	8, 13
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_{PLH}	Propagation Delay to Logic High Output (Note 9)	All	V_{DD} = 5 V, C_L = 15 pF	–	116	170	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
PWD	Pulse Width Distortion | $t_{PHL} - t_{PLH}$ | (Note 10)	All	V_{DD} = 5 V, C_L = 15 pF	–	26	70	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
$t_{PSK(PP)}$	Propagation Delay Skew (Part to Part) (Note 11)	All	V_{DD} = 5 V, C_L = 15 pF	−70	–	70	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_R	Output Rise Time (10% to 90%)	All	V_{DD} = 5 V, C_L = 15 pF	–	3.9	–	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_F	Output Fall Time (90% to 10%)	All	V_{DD} = 5 V, C_L = 15 pF	–	2.3	–	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_{PZL}	High Impedance to Logic Low Output Delay (Note 12)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	8.4	25	ns	14
			V_{DD} = 3.3 V, R_L = 1 kΩ		10.0			
			V_{DD} = 2.5 V, R_L = 1 kΩ		12.3			
t_{PLZ}	Logic Low to High Impedance Output Delay (Note 13)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	10.8	25	ns	
			V_{DD} = 3.3 V, R_L = 1 kΩ		14.3			
			V_{DD} = 2.5 V, R_L = 1 kΩ		17.5			
t_{PZH}	High Impedance to Logic High Output Delay (Note 14)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	0.53	1	μs	15
			V_{DD} = 3.3 V, R_L = 1 kΩ		0.50			
			V_{DD} = 2.5 V, R_L = 1 kΩ		0.50			
t_{PHZ}	Logic High to High Impedance Output Delay (Note 15)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	11.6	25	ns	
			V_{DD} = 3.3 V, R_L = 1 kΩ		12.9			
			V_{DD} = 2.5 V, R_L = 1 kΩ		14.7			

8. Propagation delay t_{PHL} is measured from the 50% level of the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
9. Propagation delay t_{PLH} is measured from the 50% level of the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
10. PWD is defined as | $t_{PHL} - t_{PLH}$ | for any given device.
11. Part−to−part propagation delay skew is the difference between the measured propagation delay times of a specified channel of any two parts at identical operating conditions and equal load.
12. Enable delay t_{PZL} is measured from the 50% level of the rising edge of the EN pulse to the 50% of the falling edge of the V_O signal as it switches from high impedance state to low state.
13. Disable delay t_{PLZ} is measured from the 50% level of the falling edge of the EN pulse to 0.5 V level of the rising edge of the V_O signal as it switches from low state to high impedance state.
14. Enable delay t_{PZH} is measured from the 50% level of the rising edge of the EN pulse to the 50% of the rising edge of the V_O signal as it switches from high impedance state to high state.
15. Disable delay t_{PHZ} is measured from the 50% level of the falling edge of the EN pulse to V_{OH} – 0.5 V level of the falling edge of the V_O signal as it switches from high state to high impedance state.

SWITCHING CHARACTERISTICS – NCID9311

Apply over all recommended conditions, T_A =−40°C to +125°C unless otherwise specified. All typical values are measured at T_A = 25°C.

Symbol	Parameter	Ch	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay to Logic Low Output (Note 8)	A, B	V_{DD} = 5 V, C_L = 15 pF	–	95	140	ns	9, 10, 13
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
		C	V_{DD} = 5 V, C_L = 15 pF	–	77	110	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_{PLH}	Propagation Delay to Logic High Output (Note 9)	A,B	V_{DD} = 5 V, C_L = 15 pF	–	96	140	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
		C	V_{DD} = 5 V, C_L = 15 pF	–	77	110	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
PWD	Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (Note 10)	A,B	V_{DD} = 5 V, C_L = 15 pF	–	19	60	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
		C	V_{DD} = 5 V, C_L = 15 pF	–	13	40	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
$t_{PSK(PP)}$	Propagation Delay Skew (Part to Part) (Note 11)	All	V_{DD} = 5 V, C_L = 15 pF	−60	–	60	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_R	Output Rise Time (10% to 90%)	All	V_{DD} = 5 V, C_L = 15 pF	–	2.7	–	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_F	Output Fall Time (90% to 10%)	All	V_{DD} = 5 V, C_L = 15 pF	–	2	–	ns	
			V_{DD} = 3.3 V, C_L = 15 pF					
			V_{DD} = 2.5 V, C_L = 15 pF					
t_{PZL}	High Impedance to Logic Low Output Delay (Note 12)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	8.4	25	ns	14
			V_{DD} = 3.3 V, R_L = 1 kΩ		10.0			
			V_{DD} = 2.5 V, R_L = 1 kΩ		12.3			
t_{PLZ}	Logic Low to High Impedance Output Delay (Note 13)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	10.8	25	ns	
			V_{DD} = 3.3 V, R_L = 1 kΩ		14.3			
			V_{DD} = 2.5 V, R_L = 1 kΩ		17.5			
t_{PZH}	High Impedance to Logic High Output Delay (Note 14)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	0.53	1	μs	15
			V_{DD} = 3.3 V, R_L = 1 kΩ		0.50			
			V_{DD} = 2.5 V, R_L = 1 kΩ		0.50			
t_{PHZ}	Logic High to High Impedance Output Delay (Note 15)	All	V_{DD} = 5 V, R_L = 1 kΩ	–	11.6	25	ns	
			V_{DD} = 3.3 V, R_L = 1 kΩ		12.9			
			V_{DD} = 2.5 V, R_L = 1 kΩ		14.7			

TYPICAL PERFORMANCE CHARACTERISTICS

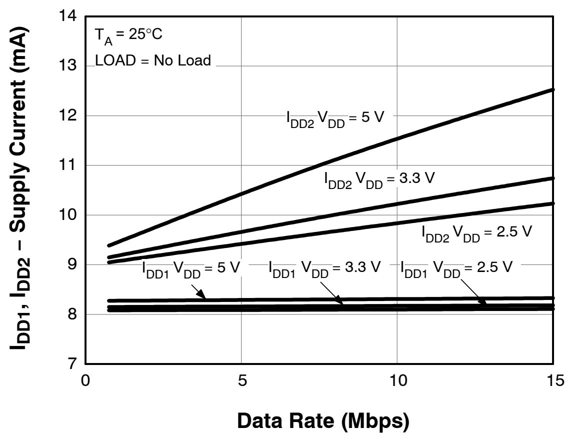


Figure 3. NCID9301 Supply Current vs. Data Rate (No Load)

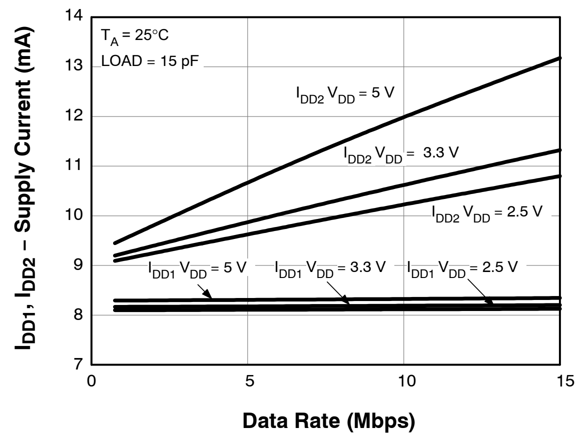


Figure 4. NCID9301 Supply Current vs. Data Rate (Load = 15 pF)

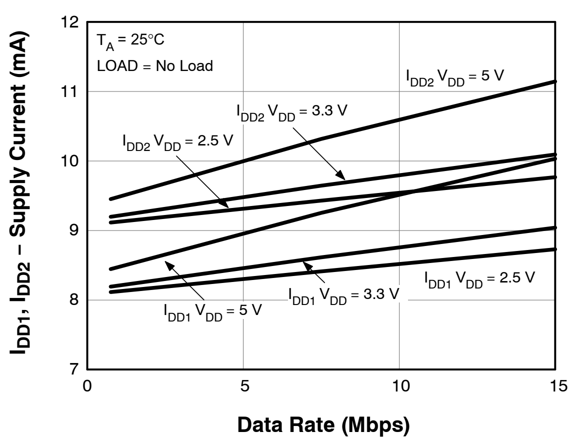


Figure 5. NCID9311 Supply Current vs. Data Rate (No Load)

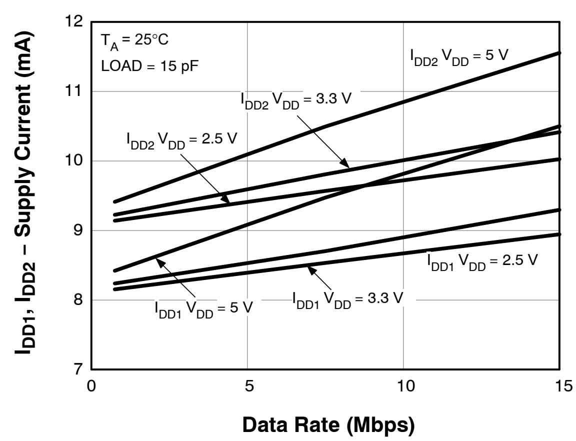


Figure 6. NCID9311 Supply Current vs. Data Rate (Load = 15 pF)

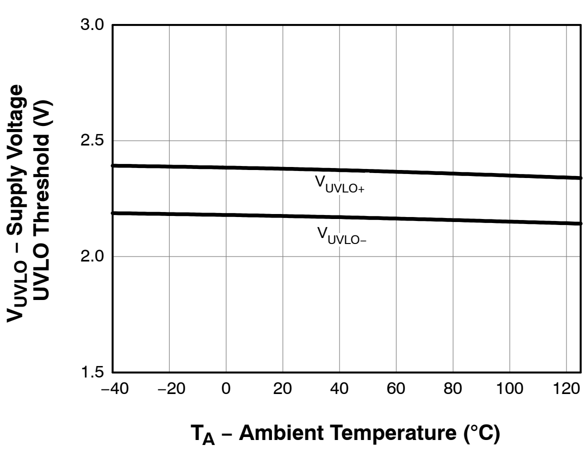


Figure 7. Supply Voltage UVLO Threshold vs. Ambient Temperature

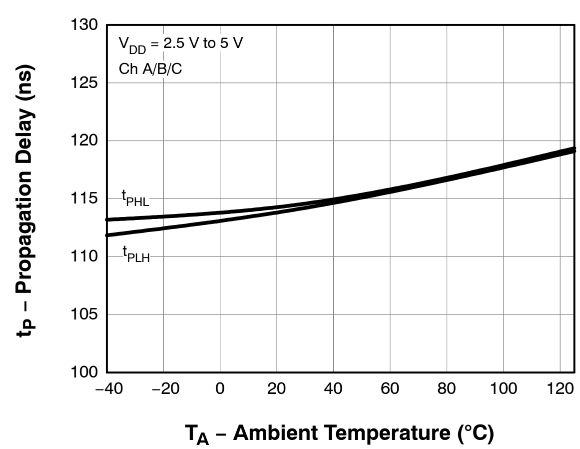


Figure 8. NCID9301 Propagation Delay vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

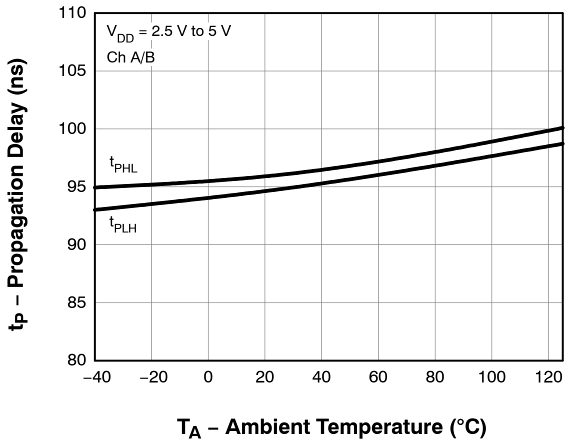


Figure 9. NCID9311 Channel A/B Propagation Delay vs. Ambient Temperature

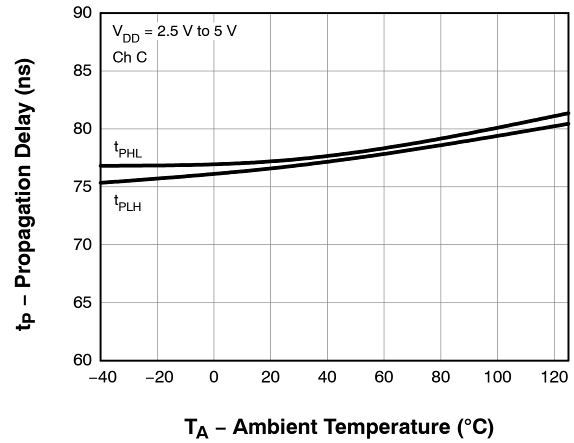


Figure 10. NCID9311 Channel C Propagation Delay vs. Ambient Temperature

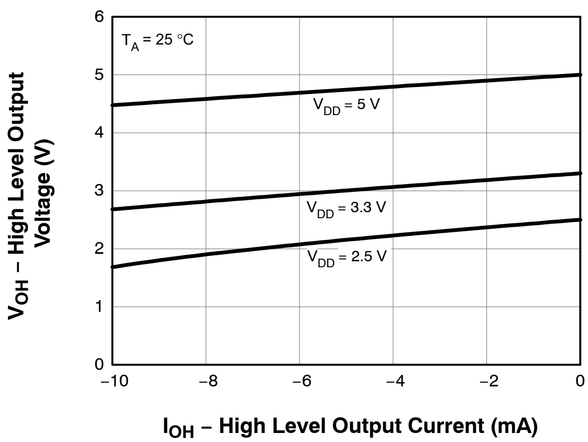


Figure 11. High Level Output Voltage vs. Current

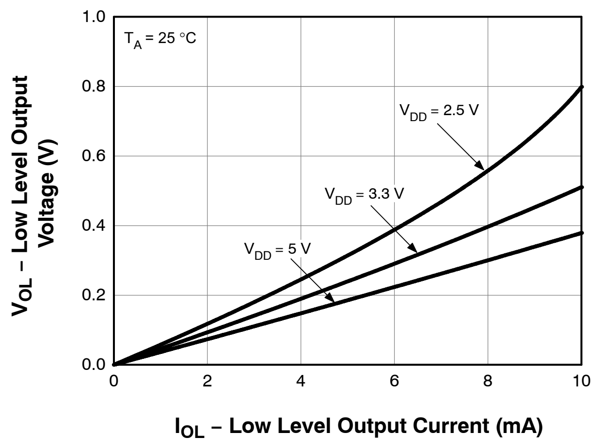


Figure 12. Low Level Output Voltage vs. Current

TEST CIRCUITS

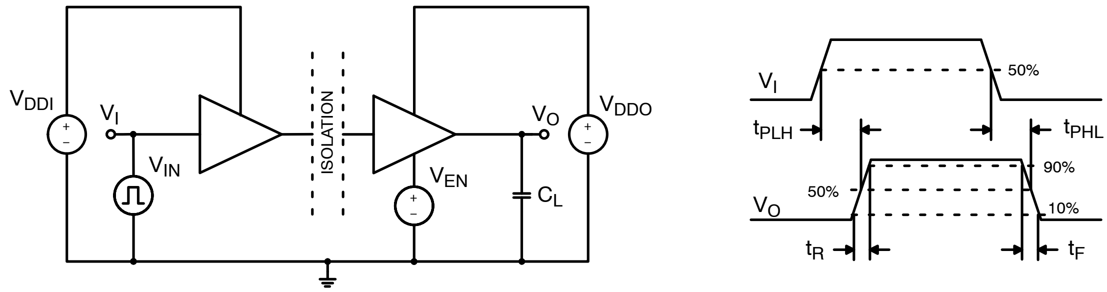


Figure 13. V_{IN} to V_O Propagation Delay Test Circuit and Waveform

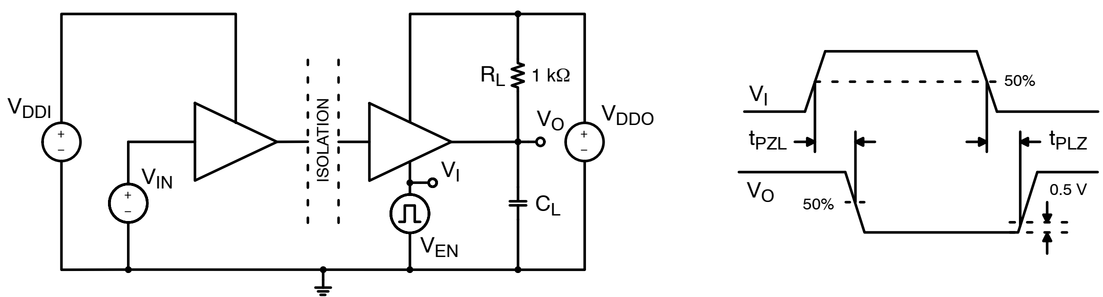


Figure 14. EN to Logic Low V_O Propagation Delay Test Circuit and Waveform

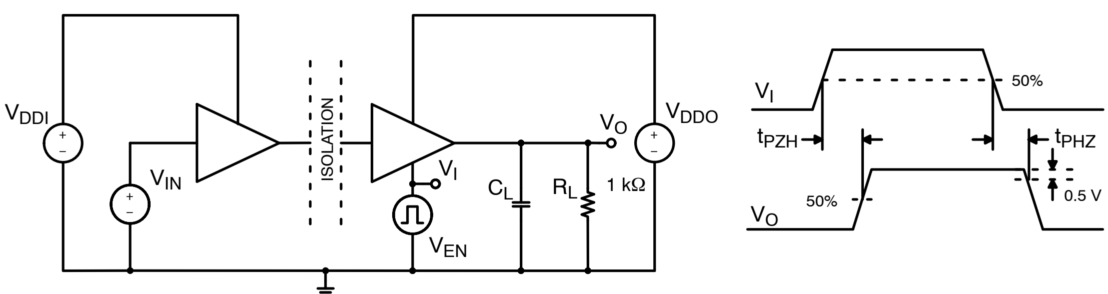
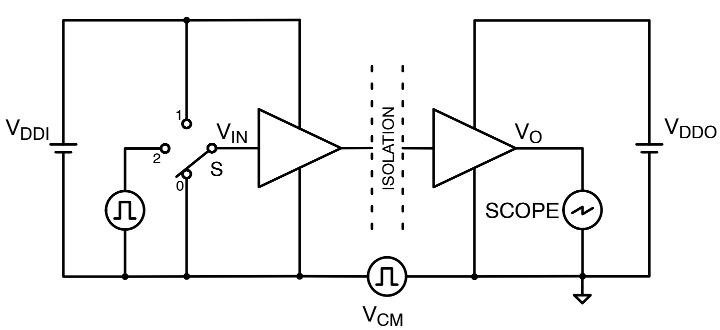


Figure 15. EN to Logic High V_O Propagation Delay Test Circuit and Waveform



S at 0, V_O remain consistently low
S at 1, V_O remain consistently high
S at 2, V_O data same as V_{IN} data

Figure 16. Common Mode Transient Immunity Test Circuit

APPLICATION INFORMATION

Theory of Operation

NCID9301 and NCID9311 are 3−channel digital isolators. The chip to chip galvanic isolation are provided by a pair of off−chip capacitors. Digital circuits are used for processing signals through the 0.5 mm thick isolation barrier.

Pins are trimmed internally as input or output at IO Switch. Each direction of communication between two isolated circuits are achieved by implementing a pair of Serializer/Deserializer and Manchester Encoder/Decoder functional blocks as shown in Figure 17. The Serializer circuit converts the parallel data from the IO Switch into a serial (one bit) stream and the Manchester Encoder converts this data stream into coded data making it more robust, efficient and accurate for transmission. After encoding, all inputs signals are coded as V_IT_X and transmitted across the isolation barrier via Transceiver.

The off−chip ceramic capacitors that serve both as the isolation barrier and as the medium of transmission for signal switching using On−Off keying (OOK) technique, illustrated in the transceiver block diagram in Figure 18 and Figure 19. At the transmitter side, the V_IT_X input logic state is modulated with a high frequency carrier signal. The resulting signal is amplified and transmitted to the isolation barrier. The receiver side detects the barrier signal and demodulates it using an envelope detection technique and output V_OR_X.

The output signal of the transceiver V_OR_X will go to the Manchester Decoder. This decoder is used along with the receiver to recover the original data from the coded form and the Deserializer converts the serial stream back to the original, parallel data and redistributed back to the corresponding output pins. Both the Serializer/Deserializer and Manchester Encoder/Decoder are functional blocks on the transmitting and receiving chips.

The output enable pin EN controls the impedance of the V_{OX}. When EN is at LOW, output V_{OX} is set to high impedance state. The V_{OX} will only follow the V_{INX} when EN is set to HIGH. V_{OX} is at default state LOW when the power supply at the transmitter side is turned off or the input V_{INX} is disconnected.

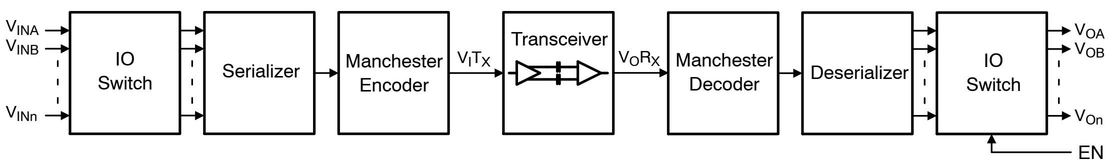


Figure 17. Operational Block Diagram of Multi−Channels for Forward Direction

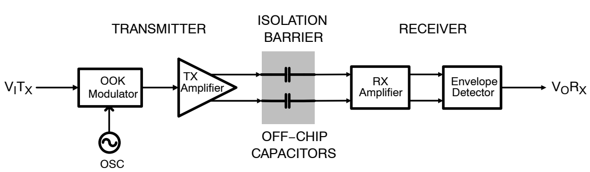


Figure 18. Block Diagram of Transceiver

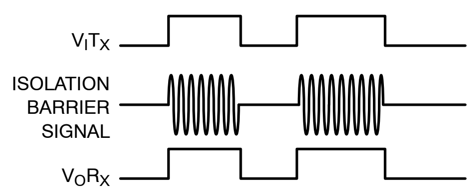


Figure 19. On−Off Keying Modulation Signals

Layout Recommendation

Layout of the digital circuits relies on good suppression of unwanted noise and electromagnetic interference. It is recommended to use 4−layer FR4 PCB, with ground plane below the components, power plane below the ground plane, signal lines and power fill on top, and signal lines and ground fill at the bottom as shown in Figure 20. The alternating polarities of the layers creates interplane capacitances that aids the bypass capacitors required for reliable operation at digital switching rates.

In the layout with digital isolators, it is required that the isolated circuits have separate ground and power planes. The section below the device should be clear with no power, ground or signal traces. Maintain a gap equal to or greater than the specified minimum creepage clearance of the device package.

It is highly advised to connect at least a pair of low ESR supply bypass capacitors, placed within 2 mm from the power supply pins 1 and 16 and ground pins 2 and 15 as shown in Figure 21. Recommended values are 1 μF and 0.1 μF, respectively. Place them between the V_{DD} pins of the device and the via to the power planes, with the higher frequency, lower value capacitor closer to the device pins. Directly connect the device ground pins 2, 8, 9 and 15 by via to their corresponding ground planes.

Over Temperature Detection

NCID9301 and NCID9311 have built−in Over Temperature Detection (OTD) feature that protects the IC from thermal damage. The output pins will automatically switch to default state when the ambient temperature exceeds the maximum junction temperature at threshold of approximately 160°C. The device will return to normal operation when the temperature decreases approximately 20°C below the OTD threshold.

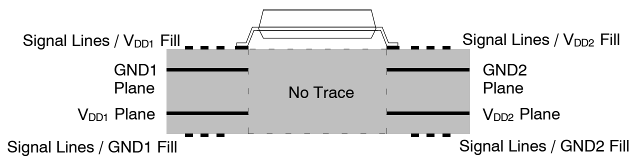


Figure 20. 4−Layer PCB for Digital Isolator

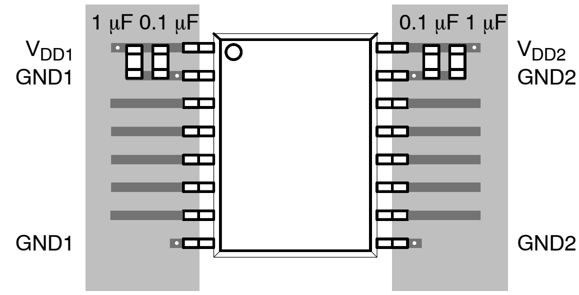


Figure 21. Placement of Bypass Capacitors

ORDERING INFORMATION

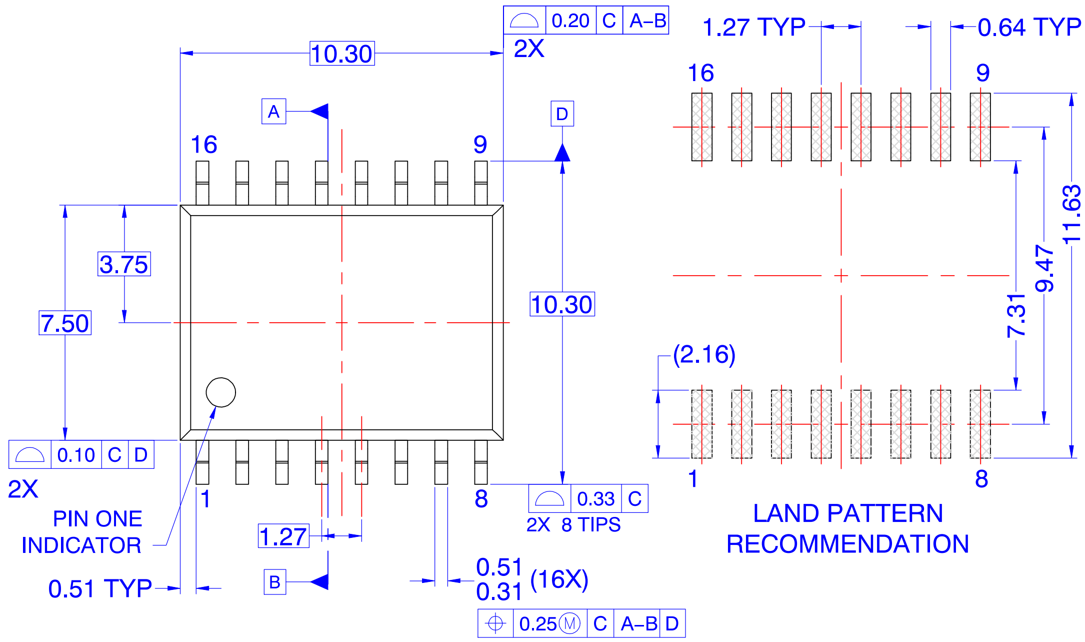
Part Number	Grade	Package	Shipping†
NCID9301	Industrial	SOIC16 W	50 Units / Tube
NCID9301R2	Industrial	SOIC16 W	750 Units / Tape & Reel
NCID9311	Industrial	SOIC16 W	50 Units / Tube
NCID9311R2	Industrial	SOIC16 W	750 Units / Tape & Reel
NCIV9301* (pending)	Automotive	SOIC16 W	50 Units / Tube
NCIV9301R2* (pending)	Automotive	SOIC16 W	750 Units / Tape & Reel
NCIV9311* (pending)	Automotive	SOIC16 W	50 Units / Tube
NCIV9311R2* (pending)	Automotive	SOIC16 W	750 Units / Tape & Reel

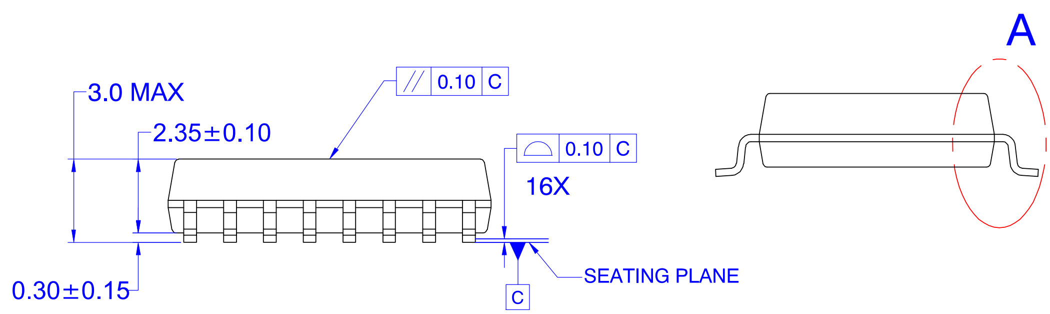
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

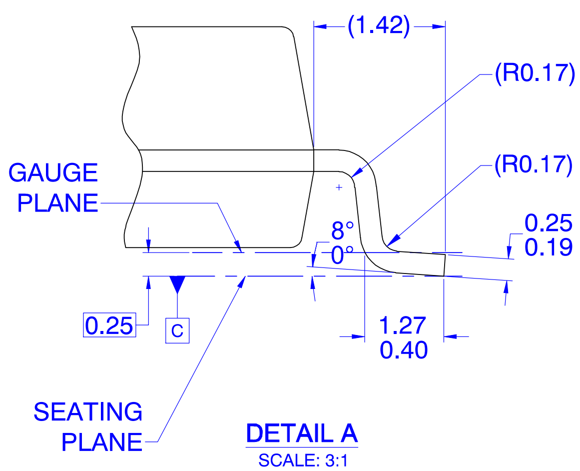
*NCIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SOIC16 W
CASE 751EN
ISSUE O







DETAIL A
SCALE: 3:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING REFERS TO JEDEC MS–013, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M–1994
E) LAND PATTERN STANDARD: SOIC127P1030X275–16N

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