

NCN7201

2:1 Gigabit Ethernet LAN Switch with Power-down Feature

The NCN7201 is an 8-channel, bidirectional Ethernet switch featuring a power shutdown feature with minimal current consumption. The NCN7201 is an upgraded version of the NCN7200, offering improved performance on the data lines while still maintaining backwards compatibility. This switch is compatible with 10/100/1000 Base-T Ethernet standards, providing high bandwidth and low return loss. Three additional lines are provided for status indicator LEDs that switch. ESD protection is built into the switch. This device can be used to route signals between a single Ethernet transceiver and an RJ45 connector and a docking station. The NCN7201 comes in a 42-pin WQFN package (3.5 mm x 9 mm, 0.5 mm pitch).

Features

- 2:1 Multiplexer/ Demultiplexer LAN Switch
- Three Additional Channels for LED Switching
- Fully Specified for Power Supply Range: 3 V to 3.6 V
- Power-down Feature Conserves Energy
- Insertion loss of -2.7 dB at 1 GHz
- ESD Performance: ± 8 kV Human Body Model (JEDEC)
 ± 8 kV Contact Discharge (IEC61000-4-2)
- This is a Pb-Free Device

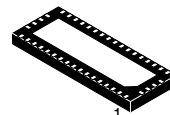
Typical Applications

- Signal Routing for 10/100/1000 Mbps Ethernet



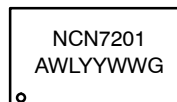
ON Semiconductor®

<http://onsemi.com>



WQFN42
CASE 510AP

MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCN7201MTTWG	WQFN42 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCN7201

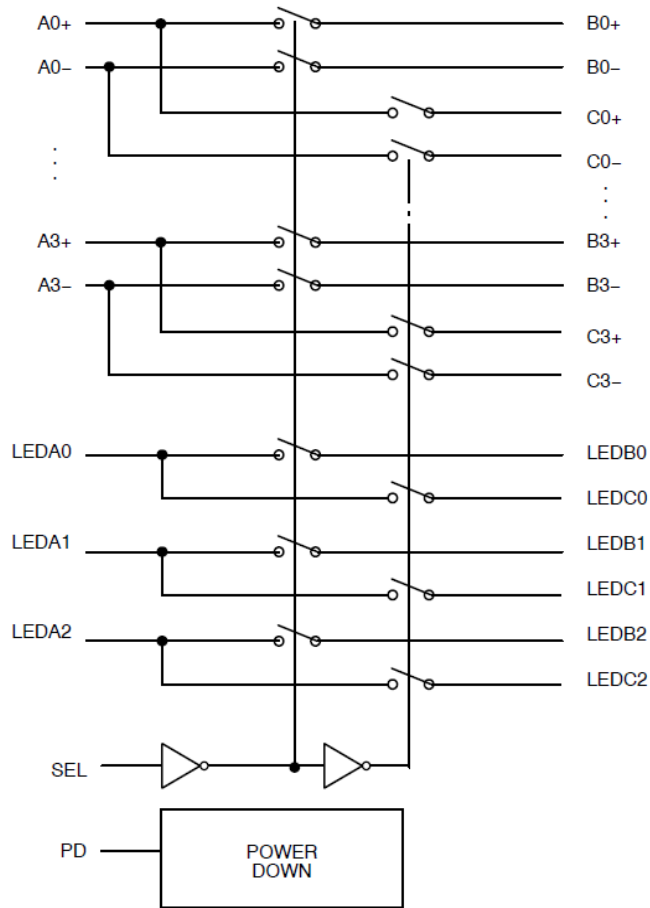


Figure 1. Block Diagram

TRUTH TABLE

PD	SEL	Function
0	0	AX to BX; LEDAX to LEDBX
0	1	AX to CX; LEDAX to LEDCX
1	X	Hi-Z

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1, 4, 8, 14, 30, 39	VDD	Power Supply Pin. It is recommended that a bypass capacitor of at least 0.1 μ F is placed as close as possible to each VDD pin.
5	PD	Power Down Pin. When PD is logic high, the device enters Power Down mode. All switch paths are high impedance. There is no internal pull-up or pull-down resistor; therefore, this pin cannot be floated.
13	SEL	Channel Select Pin. When PD is logic low, the SEL pin controls whether the AX pins are connected to BX or CX. There is no internal pull-up or pull-down resistor; therefore, this pin cannot be floated.
2, 3, 6, 7, 9, 10, 11, 12	AX+, AX-	Data Port A. This is the common side of the data switch.
24, 25, 28, 29, 33, 34, 37, 38	BX+, BX-	Data Port B. This is a switchable port of the data switch.
22, 23, 26, 27, 31, 32, 35, 36	CX+, CX-	Data Port C. This is a switchable port of the data switch.
15, 16, 42	LEDAX	LED Port A. This is the common side of the LED switch.
17, 18, 41	LEDBX	LED Port B. This is a switchable port of the LED switch.
19, 20, 40	LEDCX	LED Port C. This is a switchable port of the LED switch.
Exposed Pad on Underside	GND	Ground Supply. The exposed pad provides ground reference to the device.

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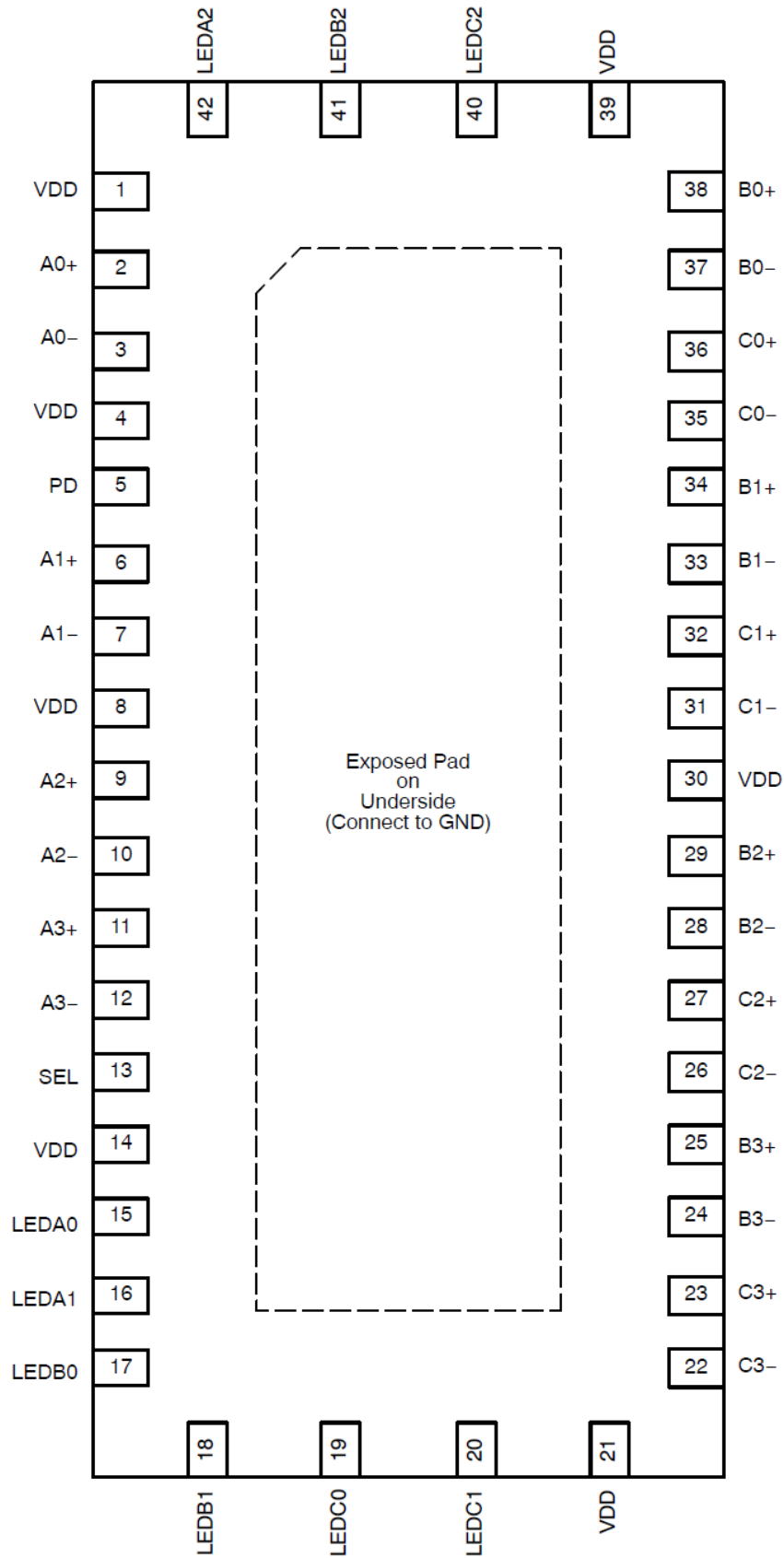


Figure 2. Pin Description
(Top View)

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit	
Maximum Supply Voltage Range	V_{DD}	-0.5 to 4.0	V	
Maximum Analog Signal Voltage Range	V_{IS}	-0.5 to $V_{DD}+0.5$	V	
Maximum Voltage Range on Control Pins	V_{IN}	-0.5 to 6.0	V	
Continuous Switch Current	I_{IS}	120	mA	
Maximum Junction Temperature	$T_{J(max)}$	150	°C	
Storage Temperature Range	T_{STG}	-65 to 150	°C	
Power Dissipation	P_d	0.5	W	
ESD Capability (Note 2)	Human Body Model	ESD_{HBM}	8000	V
	Machine Model	ESD_{MM}	400	
	Charged Device Model	ESD_{CDM}	2000	
Latch-up Current (Note 2)	I_{LU}	150	mA	
Moisture Sensitivity Level (Note 3)	MSL	Level 1		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (JEDEC standard: JESD22-A114)
 ESD Machine Model tested per AEC-Q100-003 (JEDEC standard: JESD22-A115)
 ESD Charged Device Model tested per AEC-Q1000-005 (JEDEC standard: JESD22-C101E)
 Latch-up Current tested per JEDEC standard: JESD78
- Moisture Sensitivity Level tested per IPC/JEDEC standard: J – STD – 020A

OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	3.0	3.6	V
Analog Signal Voltage	V_{IS}	0	V_{DD}	V
Control Input Voltage on PD and SEL	V_{IN}	0	V_{DD}	V
Ambient Temperature	T_A	-40	85	°C

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ELECTRICAL CHARACTERISTICS

Typical values are referenced to $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.3\text{ V}$, unless otherwise noted. Min/max values apply from $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise noted. (Notes 4 and 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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CURRENT CONSUMPTION

Quiescent Supply Current	$V_{DD} = 3.6\text{ V}$, $V_{IN} = 0\text{ V}$ or V_{DD}	I_{DD-Q}		380	450	μA
Power Down Supply Current	$V_{DD} = 3.6\text{ V}$, $V_{PD} = V_{DD}$	I_{DD-PD}		130	160	μA
Active Power Supply Current	$V_{DD} = 3.6\text{ V}$, $V_{SEL} = 0\text{ V}$ or V_{DD}	$I_{DD-ACTIVE}$		1	1.5	mA
Power Off Leakage Current	$V_{DD} = 0\text{ V}$, $V_{IN} = 0\text{ V}$ or V_{DD}	I_{OFF}	-0.1		0.1	μA

CONTROL LOGIC (SEL and PD Pins)

High Voltage Input Threshold	$V_{DD} = 3.2\text{ V}$ to 3.6 V	V_{IH}	2			V
Low Voltage Input Threshold	$V_{DD} = 3.2\text{ V}$ to 3.6 V	V_{IL}			0.8	V
Clamp Diode Voltage	$V_{DD} = 3.6\text{ V}$, $I_{IN} = -18\text{ mA}$	V_{IK}	-1.4	-0.9		V
Control Input Leakage – Logic High	$V_{DD} = 3.6\text{ V}$, $V_{SEL} = 3.6\text{ V}$ $V_{DD} = 3.6\text{ V}$, $V_{PD} = 3.6\text{ V}$	I_{IN}	-0.1 -1.2		0.1 1.2	μA
Control Input Leakage – Logic Low	$V_{DD} = 3.6\text{ V}$, $V_{IN} = 0\text{ V}$	I_{IN}	-0.1		0.1	μA
Control Input Capacitance	$f = 1\text{ MHz}$	C_{IN}		2.5		pF

DATA SWITCH DC CHARACTERISTICS (AX, BX, and CX Pins)

On Resistance	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$, $V_{IS} = 1.5\text{ V}$ $V_{IS} = V_{DD}$	R_{ON}		2.9 4.2	6 6	Ω
On Resistance Flatness	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$, $V_{IS} = 0$ to 2 V $V_{IS} = 2\text{ V}$ to V_{DD}	$R_{ON-FLAT}$		0.1 1.2		Ω
On Resistance Matching	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$, $V_{IS} = 1.5\text{ V}$ $V_{IS} = V_{DD}$	ΔR_{ON}		0.6 0.7		Ω
Switch Off Leakage	$V_{DD} = 3.6\text{ V}$, $V_{IS} = 0$ to 3.6 V	I_{SW_OFF}	-0.1		0.1	μA
Switch On Leakage	$V_{DD} = 3.6\text{ V}$, $V_{IS} = 0$ to 3.6 V	I_{SW_ON}	-0.1		0.1	μA

DATA SWITCH AC CHARACTERISTICS (AX, BX, and CX Pins)

On Capacitance	$f = 1\text{ MHz}$	C_{ON}		3.5		pF
Off Capacitance	$f = 1\text{ MHz}$	C_{OFF}		2.0		pF
Differential Bandwidth		D_{BW}		1.1		GHz
Differential Insertion Loss	$f = 250\text{ MHz}$ $f = 500\text{ MHz}$ $f = 1\text{ GHz}$	D_{IL}		-1.0 -0.9 -2.7		dB
Differential Return Loss	$f = 40\text{ MHz}$ $f = 100\text{ MHz}$	D_{RL}		-24 -16		dB
Differential Crosstalk, Adjacent Channel	$f = 250\text{ MHz}$ $f = 500\text{ MHz}$ $f = 1\text{ GHz}$	D_{CTK}		-46 -39 -30		dB
Differential Off Isolation	$f = 250\text{ MHz}$ $f = 500\text{ MHz}$ $f = 1\text{ GHz}$	D_{ISO}		-35 -28 -22		dB

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$.
6. Guaranteed by design.

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ELECTRICAL CHARACTERISTICS

Typical values are referenced to $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.3\text{ V}$, unless otherwise noted. Min/max values apply from $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise noted. (Notes 4 and 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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LED SWITCH DC CHARACTERISTICS (LEDAX, LEDBX, and LEDCX Pins)

On Resistance	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$, $V_{IS} = 1.5\text{ V}$ $V_{IS} = V_{DD}$	R_{ON}		17 12	25 25	Ω
On Resistance Flatness	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$, $V_{IS} = 0$ to V_{DD}	$R_{ON-FLAT}$		8.4		Ω
On Resistance Matching	$V_{DD} = 3.0\text{ V}$, $I_{IS} = 40\text{ mA}$ $V_{IS} = 1.5\text{ V}$ $V_{IS} = V_{DD}$	ΔR_{ON}		1.4 1.2		Ω
Switch Off Leakage	$V_{DD} = 3.6\text{ V}$, $V_{IS} = 0$ to 3.6 V	I_{SW_OFF}	-0.1		0.1	μA
Switch On Leakage	$V_{DD} = 3.6\text{ V}$, $V_{IS} = 0$ to 3.6 V	I_{SW_ON}	-0.1		0.1	μA

LED SWITCH AC CHARACTERISTICS (LEDAX, LEDBX, and LEDCX Pins)

On Capacitance	$f = 1\text{ MHz}$	C_{ON}		4.5		pF
Off Capacitance	$f = 1\text{ MHz}$	C_{OFF}		1.5		pF
Bandwidth		BW		750		MHz
Adjacent Channel Crosstalk	$f = 250\text{ MHz}$	CTK		-29		dB
Off Isolation	$f = 250\text{ MHz}$	ISO		-31		dB

DATA SWITCH TIMING CHARACTERISTICS

Propagation Delay	(Note 6)	t_{PD}		0.25		ns
Line Enable Time	$C_L = 10\text{ pF}$, $R_L = 50\ \Omega$	t_{PZH} , t_{PZL}		30		ns
Line Disable Time	$C_L = 10\text{ pF}$, $R_L = 50\ \Omega$	t_{PHZ} , t_{PLZ}		6		ns
Bit-to-Bit Skew	$C_L = 10\text{ pF}$, $R_L = 50\ \Omega$	t_{B-B}		0.1		ns
Channel-to-Channel Skew	$C_L = 10\text{ pF}$, $R_L = 50\ \Omega$	t_{CH-CH}		0.1		ns

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25^\circ\text{C}$.
6. Guaranteed by design.

TYPICAL OPERATING CHARACTERISTICS

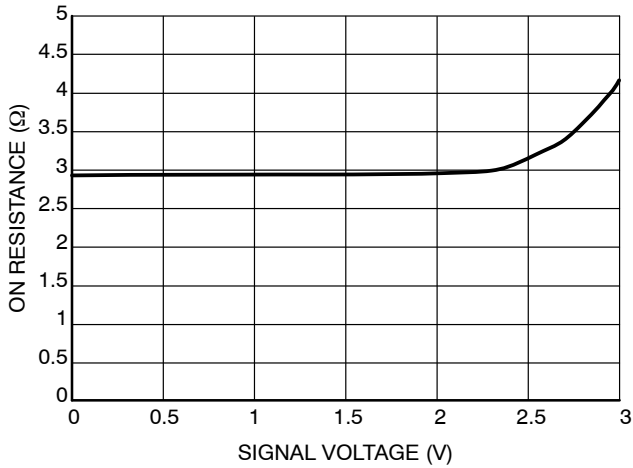


Figure 3. Data Path On Resistance at $V_{CC} = 3\text{ V}$

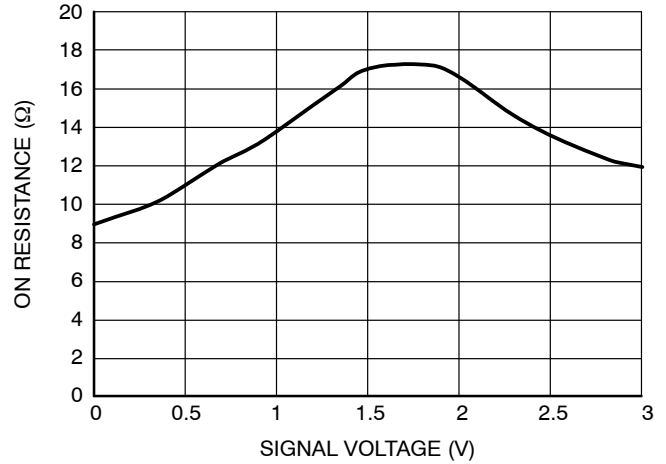


Figure 4. LED Path On Resistance at $V_{CC} = 3\text{ V}$

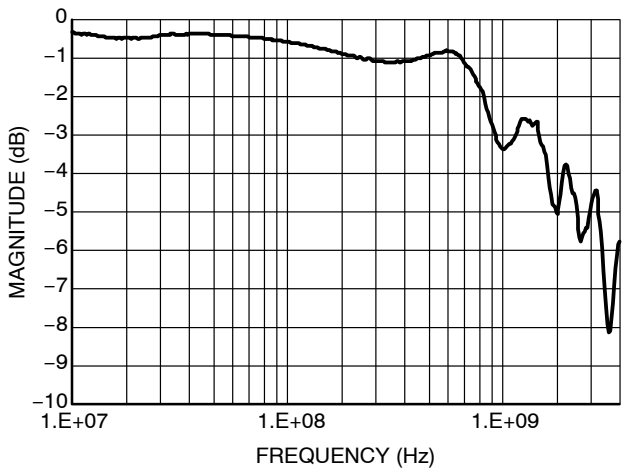


Figure 5. Data Switch Differential Insertion Loss

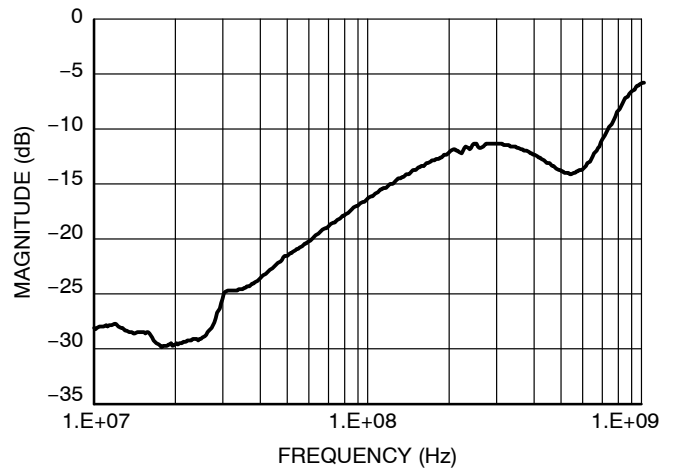


Figure 6. Data Switch Return Loss

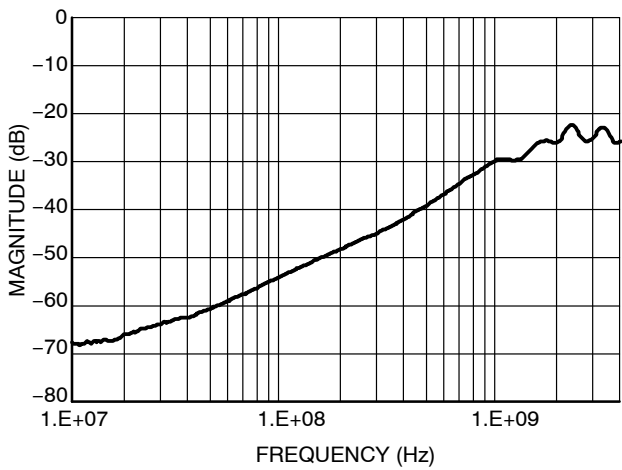


Figure 7. Data Switch Differential Crosstalk on Adjacent Channels

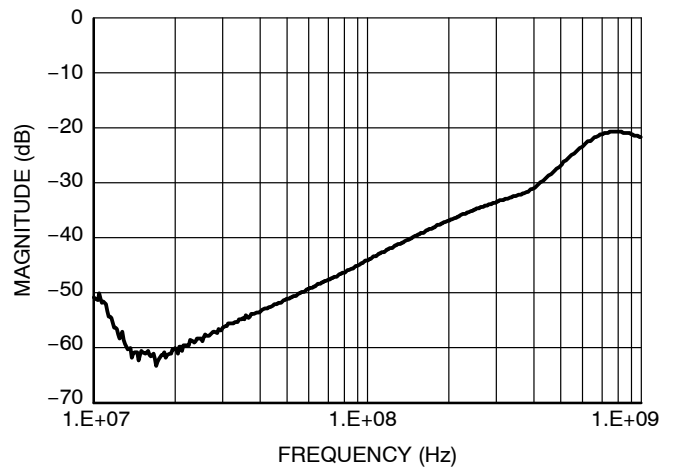


Figure 8. Data Switch Differential Off Isolation

PARAMETER MEASUREMENT INFORMATION

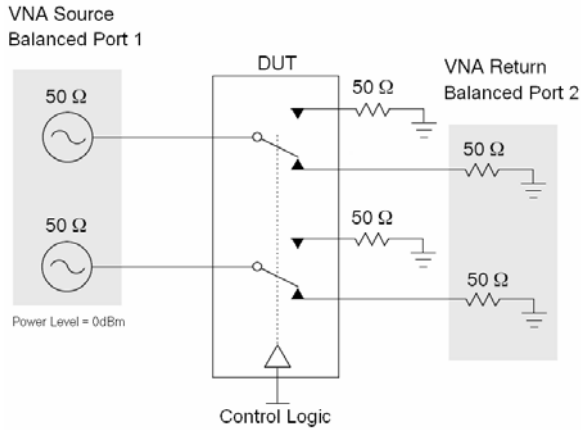


Figure 9. Differential Insertion Loss and Return Loss

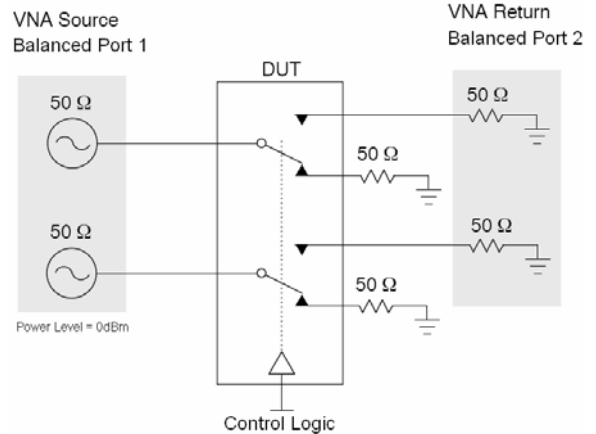


Figure 10. Differential Off Isolation

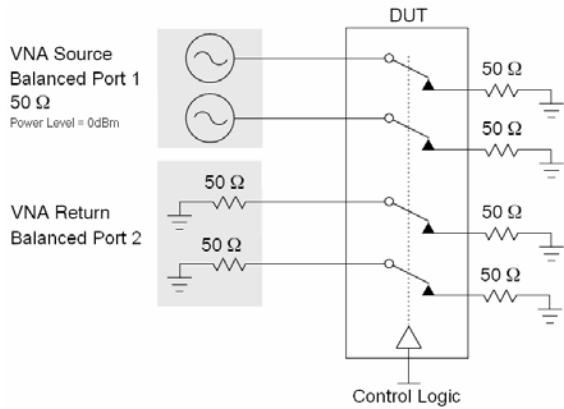


Figure 11. Differential Crosstalk

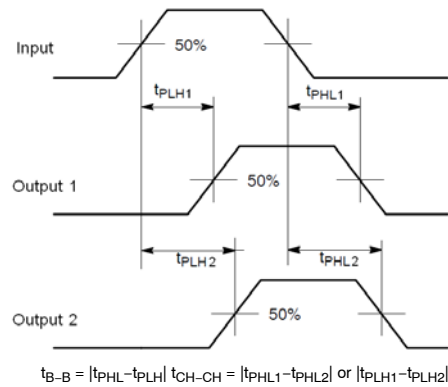


Figure 12. Bit-to-Bit and Channel-to-Channel Skew

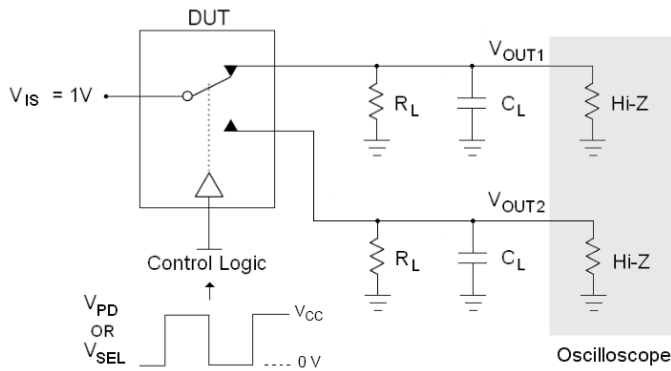


Figure 13. Line Enable and Disable Times

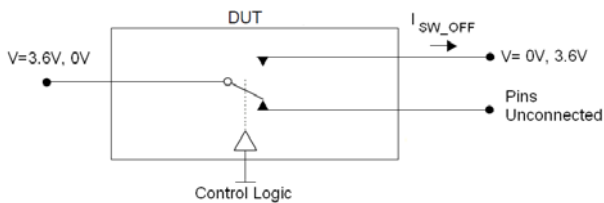
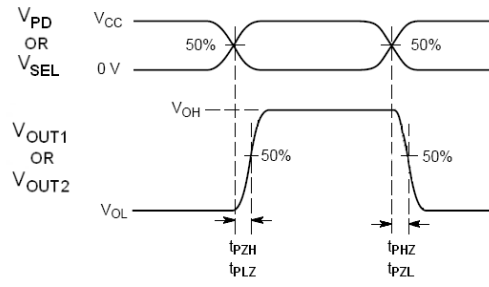


Figure 14. Off State Leakage

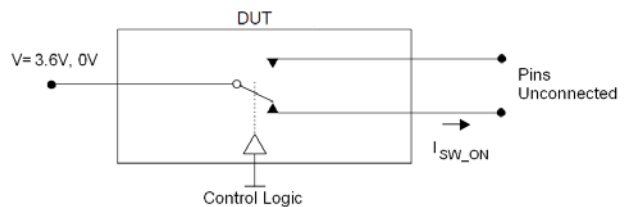
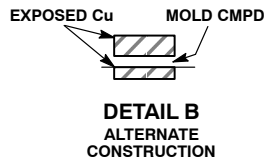
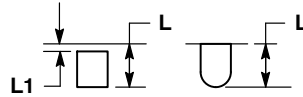
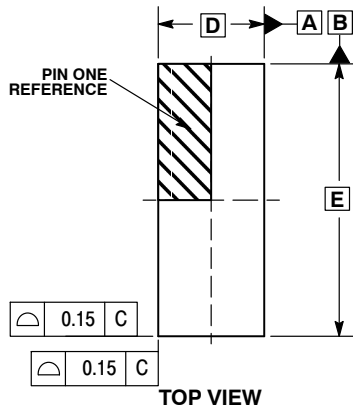


Figure 15. On State Leakage

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PACKAGE DIMENSIONS

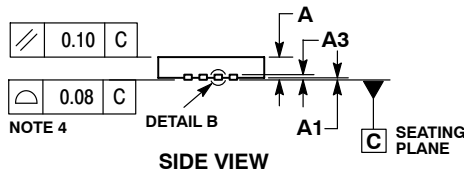
WQFN42 3.5x9, 0.5P CASE 510AP ISSUE O



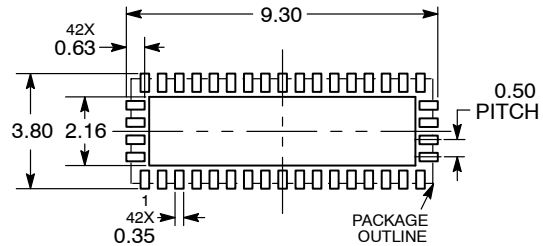
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.50 BSC	
D2	1.95	2.15
E	9.00 BSC	
E2	7.45	7.65
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

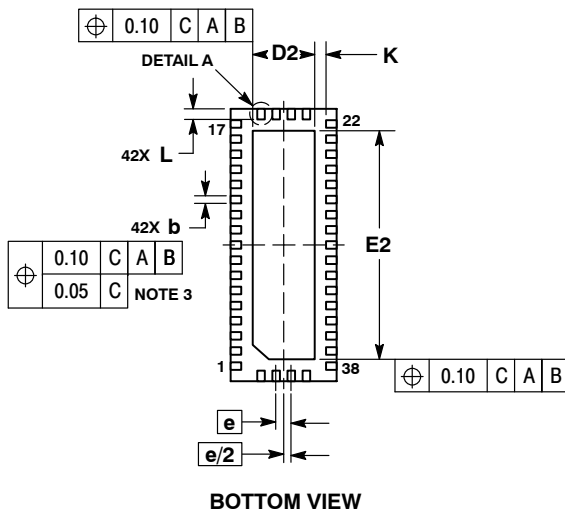


RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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