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MC74LCX139

Dual Low-Voltage CMOS 2-to-4 Decoder/Demultiplexer

With 5 V-Tolerant Inputs

The MC74LCX139 is a high performance, 2-to-4 decoder/demultiplexer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX139 inputs to be safely driven from 5 V devices. The MC74LCX139 is suitable for memory address decoding and other TTL level bus oriented applications.

The MC74LCX139 high-speed 2-to-4 decoder/demultiplexer accepts two binary weighted inputs (A0, A1) and, when enabled, provides four mutually exclusive active-LOW outputs. The LCX139 features an active low Enable input. All outputs will be HIGH unless En is LOW. The LCX139 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable input as a strobe. The Enable inputs which are not used must be permanently tied to ground.

Current drive capability is 24 mA at the outputs.

Features

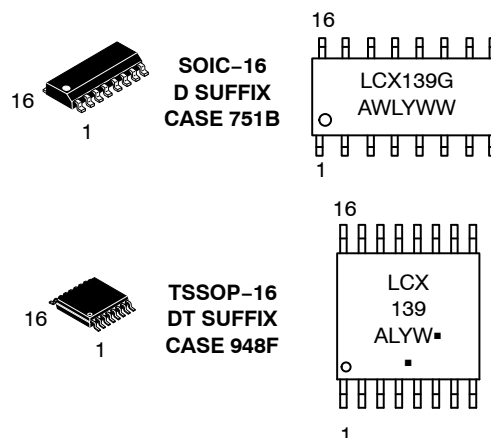
- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC74LCX139

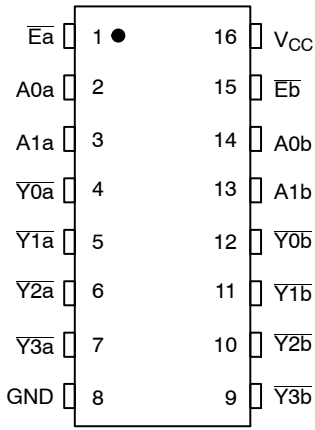


Figure 1. Pin Assignment

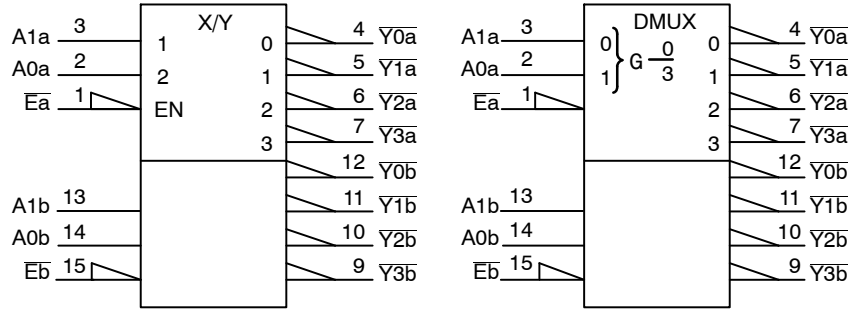
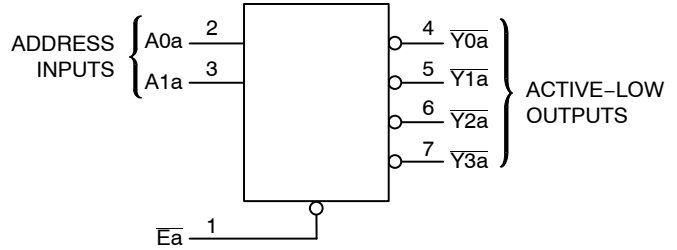


Figure 2. IEC Logic Diagram

PIN NAMES

| Pins | Function |
|---------|----------------|
| A0n–A1n | Address Inputs |
| En | Enable Inputs |
| Y0n–Y3n | Outputs |



TRUTH TABLE

| Inputs | | | Outputs | | | |
|--------|----|----|---------|----|----|----|
| E | A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = High Voltage Level;
 L = Low Voltage Level;
 Z = High Impedance State

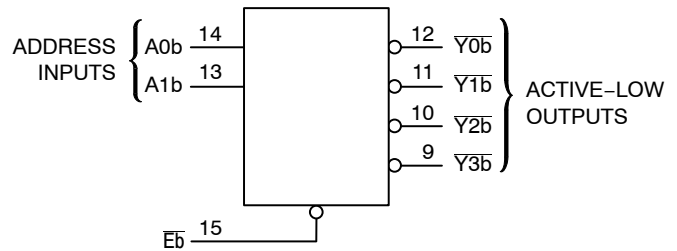


Figure 3. Logic Diagram

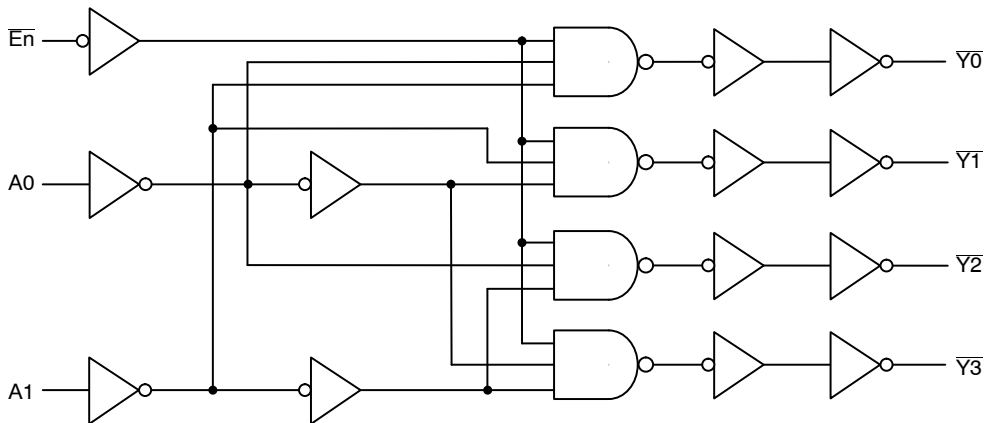


Figure 4. Expanded Logic Diagram
(1/2 of Device)

MC74LCX139

MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Units |
|------------------|----------------------------------|---|---------------------------------------|-------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | | V |
| V _I | DC Input Voltage | -0.5 ≤ V _I ≤ +7.0 | | V |
| V _O | DC Output Voltage | -0.5 ≤ V _O ≤ V _{CC} + 0.5 | Output in HIGH or LOW State. (Note 1) | V |
| I _{IK} | DC Input Diode Current | -50 | V _I < GND | mA |
| I _{OK} | DC Output Diode Current | -50 | V _O < GND | mA |
| | | +50 | V _O > V _{CC} | mA |
| I _O | DC Output Source/Sink Current | ±50 | | mA |
| I _{CC} | DC Supply Current Per Supply Pin | ±100 | | mA |
| I _{GND} | DC Ground Current Per Ground Pin | ±100 | | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | | °C |
| MSL | Moisture Sensitivity | | Level 1 | |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|--|-----|------------|-----------------|-------|
| V _{CC} | Supply Voltage Operating Data Retention Only | 2.0 | 2.3 to 3.3 | 3.6 | V |
| | | 1.5 | | 3.6 | |
| V _I | Input Voltage | 0 | | 5.5 | V |
| V _O | Output Voltage (HIGH or LOW State) | 0 | | V _{CC} | V |
| I _{OH} | HIGH Level Output Current V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V | | | -24 | mA |
| | | | | -12 | |
| | | | | -8 | |
| | | | | | |
| I _{OL} | LOW Level Output Current V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V | | | +24 | mA |
| | | | | +12 | |
| | | | | +8 | |
| | | | | | |
| T _A | Operating Free-Air Temperature | -40 | | +85 | °C |
| Δt/ΔV | Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V | 0 | | 10 | ns/V |

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|-----------------------|-----------------------|
| MC74LCX139DR2G | SOIC-16 (Pb-Free) | 2500 Tape & Reel |
| MC74LCX139DTG | TSSOP-16 (Pb-Free) | 96 Units / Rail |
| MC74LCX139DTR2G | TSSOP-16 (Pb-Free) | 2500 Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74LCX139

DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | T _A = -40°C to +85°C | | Units |
|------------------|---------------------------------------|--|---------------------------------|------|-------|
| | | | Min | Max | |
| V _{IH} | HIGH Level Input Voltage (Note 2) | 2.3 V ≤ V _{CC} ≤ 2.7 V | 1.7 | | V |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V | 2.0 | | |
| V _{IL} | LOW Level Input Voltage (Note 2) | 2.3 V ≤ V _{CC} ≤ 2.7 V | | 0.7 | V |
| | | 2.7 V ≤ V _{CC} ≤ 3.6 V | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA | V _{CC} - 0.2 | | V |
| | | V _{CC} = 2.3 V; I _{OH} = -8 mA | 1.7 | | |
| | | V _{CC} = 2.7 V; I _{OH} = -12 mA | 2.2 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -18 mA | 2.4 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -24 mA | 2.2 | | |
| V _{OL} | LOW Level Output Voltage | 2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA | | 0.2 | V |
| | | V _{CC} = 2.3 V; I _{OL} = 8 mA | | 0.7 | |
| | | V _{CC} = 2.7 V; I _{OL} = 12 mA | | 0.4 | |
| | | V _{CC} = 3.0 V; I _{OL} = 16 mA | | 0.4 | |
| | | V _{CC} = 3.0 V; I _{OL} = 24 mA | | 0.55 | |
| I _{OFF} | Power Off Leakage Current | V _{CC} = 0, V _{IN} = 5.5 V or V _{OUT} = 5.5 V | | 10 | μA |
| I _{IN} | Input Leakage Current | V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND | | ±5 | μA |
| I _{CC} | Quiescent Supply Current | V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND | | 10 | μA |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V | | 500 | μA |

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω)

| Symbol | Parameter | Limits | | | | | | Units |
|--|--------------------------------|----------------------------------|------------|-------------------------|------------|----------------------------------|------------|-------|
| | | T _A = -40°C to +85°C | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | V _{CC} = 2.7 V | | V _{CC} = 2.3 V to 2.7 V | | |
| | | C _L = 50 pF | | C _L = 50 pF | | C _L = 30 pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay A to Y | 0.8 0.8 | 6.2 6.2 | 1.0 1.0 | 7.3 7.3 | 0.8 0.8 | 9.3 9.3 | ns |
| t _{PLH} t _{PHL} | Propagation Delay E to Y | 0.8 0.8 | 4.7 4.7 | 1.0 1.0 | 5.2 5.2 | 0.8 0.8 | 7.2 7.2 | |
| t _{OSSL} t _{OSLH} | Output-to-Output Skew (Note 3) | | 1.0 1.0 | | | | | ns |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Units |
|------------------|-------------------------------|---|---------|-------|
| C _{IN} | Input Capacitance | V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 7 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 8 | pF |
| C _{PD} | Power Dissipation Capacitance | 10MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 25 | pF |

MC74LCX139

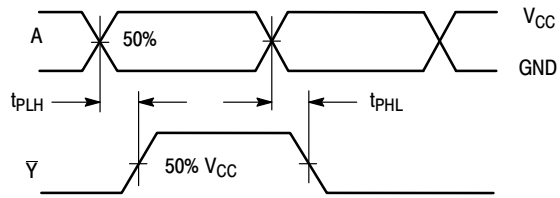


Figure 5. Waveform 1 Prop Delays

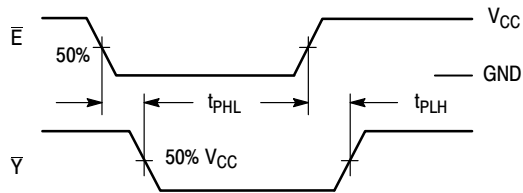
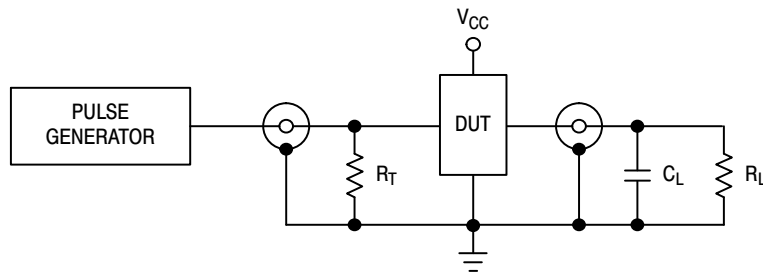


Figure 6. Waveform 2 Output Enable



$C_L = 50$ pF or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500 \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

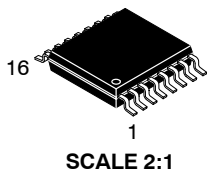
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MECHANICAL CASE OUTLINE

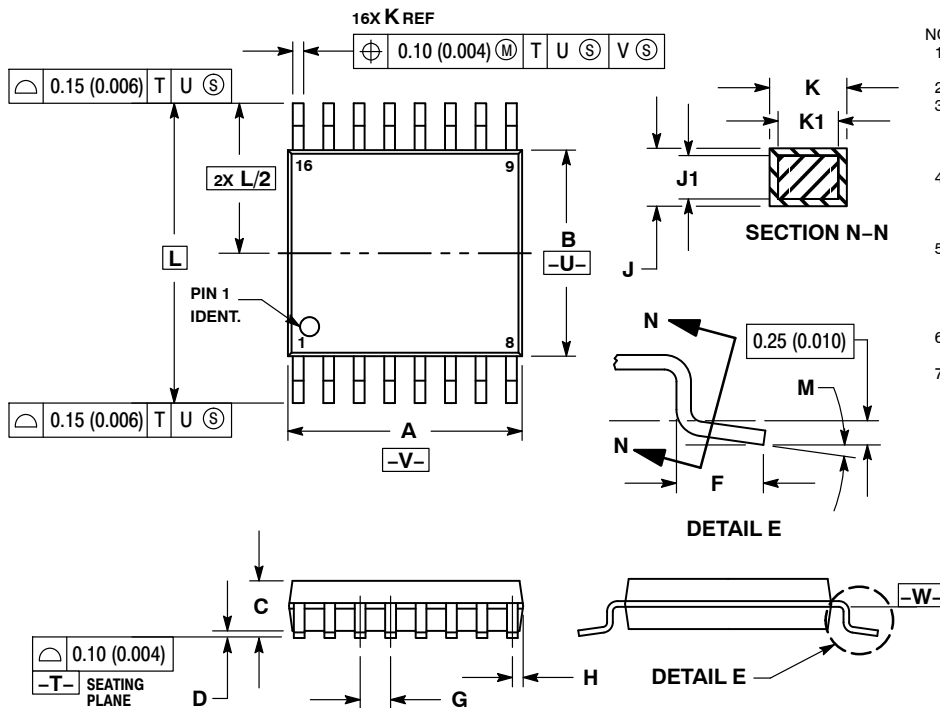
PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16
CASE 948F-01
ISSUE B

DATE 19 OCT 2006

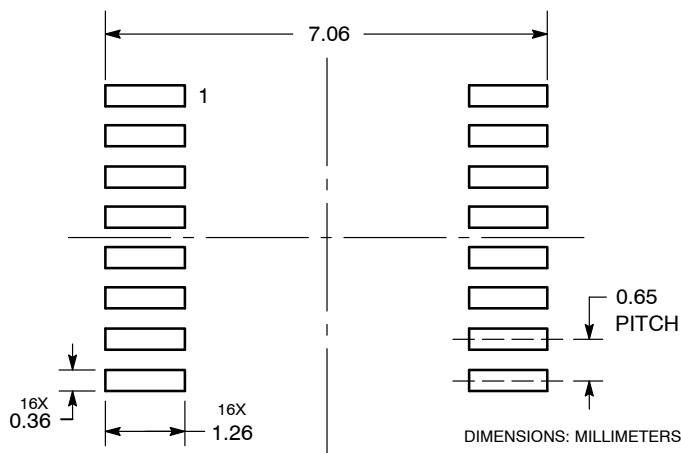


NOTES:

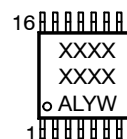
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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