

NB7L572

2.5V / 3.3V Differential 4:1 Mux Input to 1:2 LVPECL Clock/Data Fanout / Translator

Multi-Level Inputs w/ Internal Termination

The NB7L572 is a high performance differential 4:1 Clock/Data input multiplexer and a 1:2 LVPECL Clock/Data fanout buffer. The IN_x/\overline{IN}_x inputs includes internal $50\ \Omega$ termination resistors and will accept differential LVPECL, CML, or LVDS logic levels. The NB7L572 incorporates a pair of Select pins that will choose one of four differential inputs and will produce two identical LVPECL output copies of Clock or Data operating up to 7 GHz or 10 Gb/s, respectively. As such, NB7L572 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The NB7L572 IN_x/\overline{IN}_x inputs, outputs and core logic are powered by a $2.5\text{ V} \pm 5\% \text{ V}$ or $3.3\text{ V} \pm 10\% \text{ V}$ power supply. The two differential LVPECL outputs will swing 750 mV when externally terminated with a $50\ \Omega$ resistor to $V_{CC} - 2\text{ V}$, and are optimized for low skew and minimal jitter.

The NB7L572 is offered in a low profile 5x5 mm 32-pin QFN Pb-free package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7L572 is a member of the GigaComm™ family of high performance clock products.

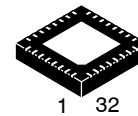
Features

- Input Data Rate > 10.7 Gb/s Typical
- Data Dependent Jitter < 15 ps
- Maximum Input Clock Frequency > 7 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:2 LVPECL Outputs, < 15 ps max
- 4:1 Multi-Level Mux Inputs, Accepts LVPECL, CML LVDS
- 150 ps Typical Propagation Delay
- 45 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 750 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 2.375\text{ V}$ to 3.6 V
- Internal $50\ \Omega$ Input Termination Resistors
- V_{REFAC} Reference Output
- -40°C to $+85^\circ\text{C}$ Ambient Operating Temperature
- These are Pb-Free Devices



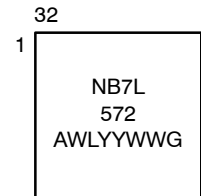
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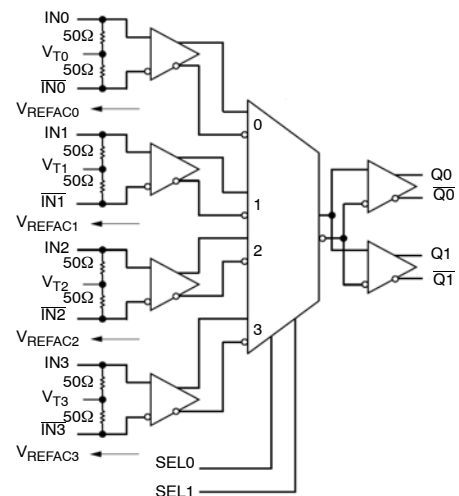
QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM*



A = Assembly Site
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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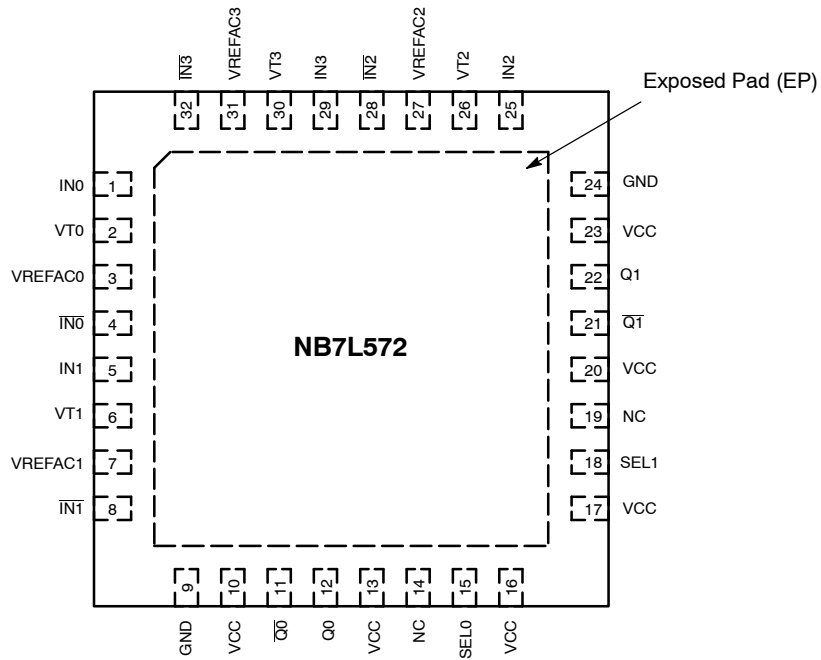


Figure 1. Pinout Configuration (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

SEL1*	SEL0*	Clock / Data Input Selected
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
1	1	IN3 Input Selected

*Defaults HIGH when left open.

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Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1, 4 5, 8 25, 28 29, 32	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$ IN2, $\overline{IN2}$ IN3, $\overline{IN3}$	LVPECL, CML, LVDS Input	Non-inverted, Inverted, Differential Clock or Data Inputs.
2, 6 26, 30	VT0, VT1 VT2, VT3		Internal 100 Ω Center-tapped Termination Pin for INx / \overline{INx}
15 18	SEL0 SEL1	LVTTTL/LVCMOS Input	Input Select pins, default HIGH when left open through a 28k- Ω pull-up resistor. Input logic threshold is $V_{CC}/2$. See Select Function, Table 1.
14, 19	NC	-	No Connect
10, 13, 16 17, 20, 23	VCC	-	Positive Supply Voltage. All VCC pins must be connected to the positive power supply for correct DC and AC operation.
11, 12 21, 22	$\overline{Q0}$, Q0 $\overline{Q1}$, Q1	LVPECL Output	Inverted, Non-inverted Differential Outputs.
9, 24	GND		Negative Supply Voltage, connected to Ground
3 7 27 31	VREFAC0 VREFAC1 VREFAC2 VREFAC3	-	Output Voltage Reference for Capacitor-Coupled Inputs
-	EP	-	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND.

1. In the differential configuration when the input termination pins (VT0, VT1, VT2, VT3) are connected to a common termination voltage or left open, and if no signal is applied on INx / \overline{INx} input, then the device will be susceptible to self-oscillation.
2. All VCC, and GND pins must be externally connected to a power supply for proper operation.

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Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 150 V
Input Pullup Resistor (R _{PU})		28 kΩ
Moisture Sensitivity (Note 3)	QFN32	Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in
Transistor Count		205
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		-0.5 to +4.0	V
V _{IN}	Positive Input Voltage	GND = 0 V		-0.5 to V _{CC} +0.5	V
V _{INPP}	Differential Input Voltage I _N - I _N			1.89	V
I _{out}	LVPECL Output Current	Continuous Surge		50 100	mA mA
I _{IN}	Input Current Through RT (50 Ω Resistor)			± 40	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case) (Note 4)		QFN-32	12	°C/W
T _{sol}	Wave Solder	≤ 20 sec		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 5. DC CHARACTERISTICS POSITIVE LVPECL OUTPUT $V_{CC} = 2.375 \text{ V to } 3.6 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$
(Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
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POWER SUPPLY

V_{CC}	Power Supply Voltage	$V_{CC} = 2.5 \text{ V}$ $V_{CC} = 3.3 \text{ V}$	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current for V_{CC} (Inputs and Outputs Open)			90	110	mA

LVPECL OUTPUTS

V_{OH}	Output HIGH Voltage (Note 6)	$V_{CC} = 2.5 \text{ V}$ $V_{CC} = 3.3 \text{ V}$	$V_{CC} - 1145$ 1355 2155	$V_{CC} - 900$ 1600 2400	$V_{CC} - 825$ 1675 2475	mV
V_{OL}	Output LOW Voltage (Note 6)	$V_{CC} = 2.5 \text{ V}$ $V_{CC} = 3.3 \text{ V}$	$V_{CC} - 2000$ 500 1300	$V_{CC} - 1700$ 800 1600	$V_{CC} - 1500$ 1000 1800	mV

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 4 & 6) (Note 7)

V_{IH}	Single-Ended Input HIGH Voltage		$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage		GND		$V_{th} - 100$	mV
V_{th}	Input Threshold Reference Voltage Range (Note 8)		1100		$V_{CC} - 100$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)		200		2400	mV

VREFAC

V_{REF-AC}	Output Reference Voltage (100 μA Load)		$V_{CC} - 1500$	$V_{CC} - 1200$	$V_{CC} - 1000$	mV
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DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 5 & 7) (Note 9)

V_{IHD}	Differential Input HIGH Voltage (I_N, \bar{I}_N)		1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (I_N, \bar{I}_N)		0		$V_{IHD} - 100$	mV
V_{ID}	Differential Input Voltage (I_N, \bar{I}_N) ($V_{IHD} - V_{ILD}$)		100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 8)		800		$V_{CC} - 50$	mV
I_{IH}	Input HIGH Current I_N/\bar{I}_N (VT IN/VT \bar{I}_N Open)		-150		150	μA
I_{IL}	Input LOW Current I_N/\bar{I}_N (VT IN/VT \bar{I}_N Open)		-150		150	μA

CONTROL INPUT (SELx Pin)

V_{IH}	Input HIGH Voltage for Control Pin		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pin		GND		0.8	V
I_{IH}	Input HIGH Current				40	μA
I_{IL}	Input LOW Current		-215		0	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor (Measured from I_N x to V_T x)		45	50	55	Ω
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NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and Output parameters vary 1:1 with V_{CC} .
- LVPECL outputs loaded with 50 Ω to $V_{CC} - 2\text{V}$ for proper operation.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 6. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit	
f_{MAX}	Maximum Input Clock Frequency $V_{OUT} \geq 400\text{ mV}$	7	8		GHz	
$f_{DATAMAX}$	Maximum Operating Data Rate NRZ, (PRBS23)	10	11		Gbps	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Figure 2 & 9) (Note 12)	$f_{in} \leq 5\text{ GHz}$ 400	750 500		mV	
t_{PLH} , t_{PHL}	Propagation Delay to Differential Outputs Measured at Differential Cross-Point	@ 1 GHz INx/\overline{INx} to Qx/\overline{Qx} (Figure 9) @ 50 MHz $SELx$ to Qx (Figure 10)	125 300	150 1000	175 1000	ps
$t_{PD\ Tempco}$	Differential Propagation Delay Temperature Coefficient		115		fs/ $^\circ\text{C}$	
t_{skew}	Output – Output skew (within device) (Note 13) Device – Device skew (tpd max – tpd min)		0	10 50	ps	
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	45	50	55	%	
t_{JITTER}	Additive Random Clock Jitter, RJ(RMS) (Note 14) Data Dependent Jitter, DDJ (Note 15)	$f_{in} \leq 7.0\text{ GHz}$ $f_{in} \leq 10\text{ Gbps}$	0.5 6	0.8 15	ps rms ps pk-pk	
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 16)	100		1200	mV	
t_r, t_f	Output Rise/Fall Times @ 1 GHz; (20% – 80%), $V_{IN} = 800\text{ mV } Q, \overline{Q}$	25	45	65	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 100 mVpk-pk source, 50% duty cycle clock source. All output loading with external $50\ \Omega$ to $V_{CC} - 2\text{ V}$. Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak-to-Peak data dependent jitter with input NRZ data at K28.5.
16. Input voltage swing is a single-ended measurement operating in differential mode.

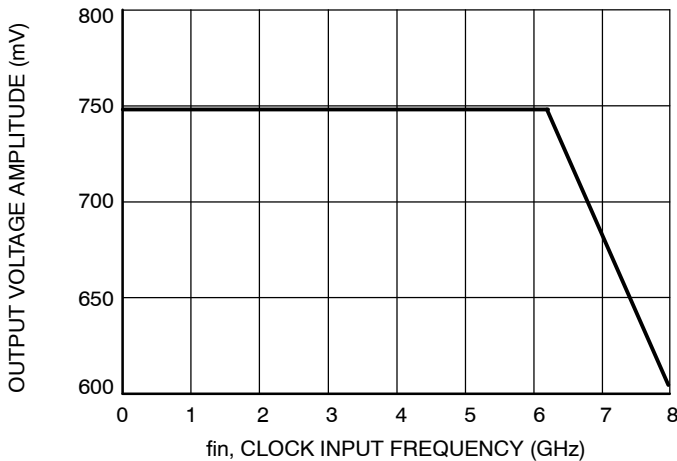


Figure 2. CLOCK Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (typical)

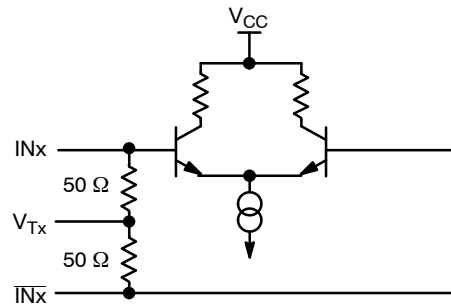


Figure 3. Input Structure

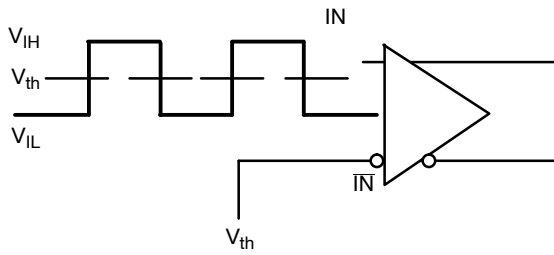


Figure 4. Differential Input Driven Single-Ended

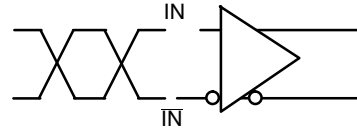


Figure 5. Differential Inputs Driven Differentially

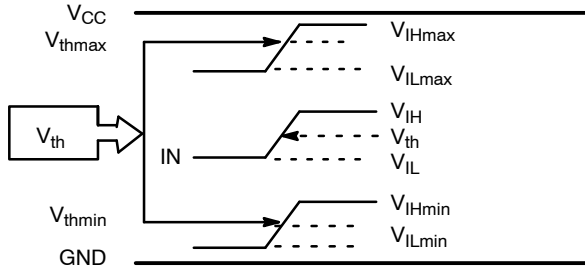


Figure 6. V_{th} Diagram

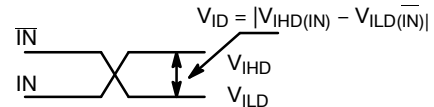


Figure 7. Differential Inputs Driven Differentially

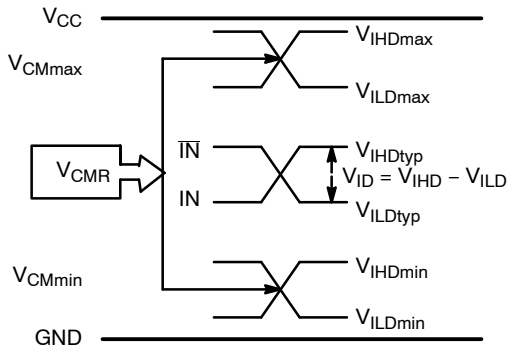


Figure 8. V_{CMR} Diagram

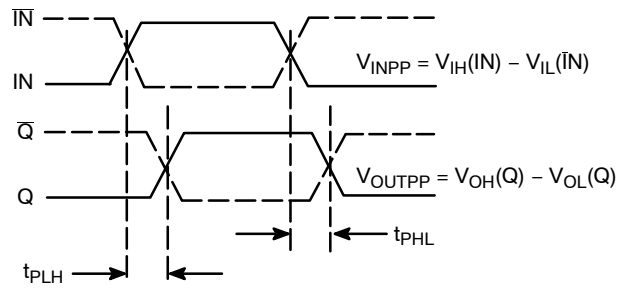


Figure 9. AC Reference Measurement

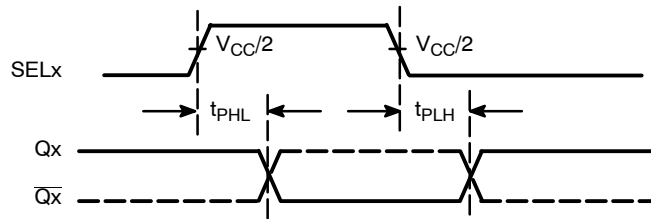
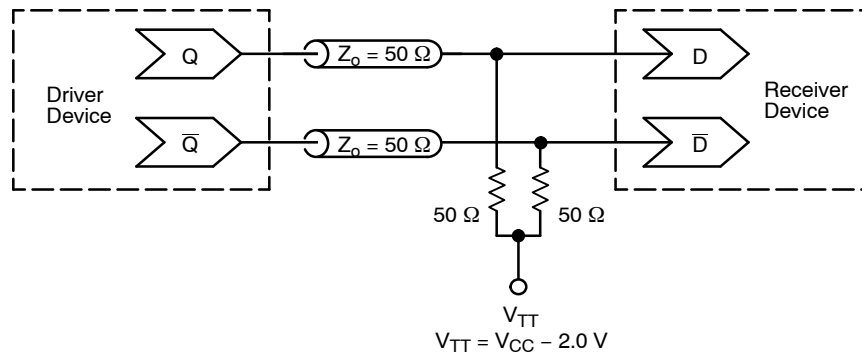


Figure 10. SELx to Qx Timing Diagram

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**Figure 11. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

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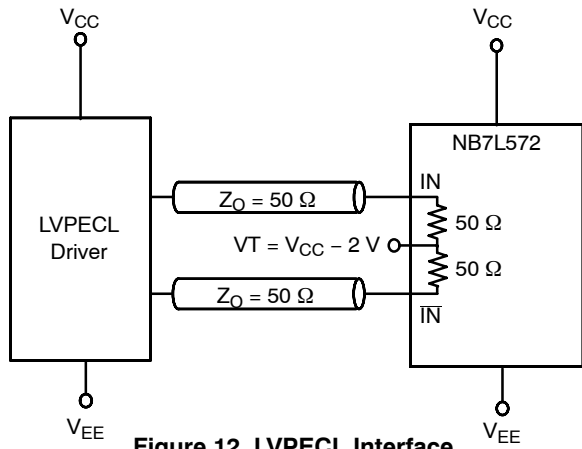


Figure 12. LVPECL Interface

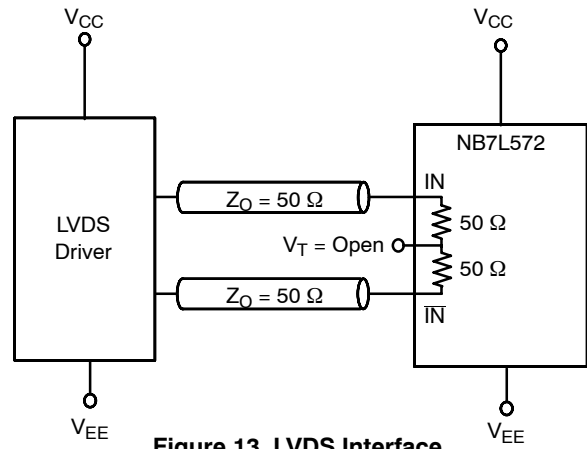


Figure 13. LVDS Interface

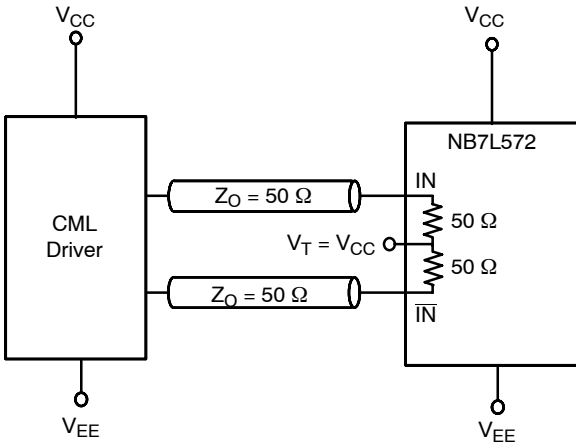


Figure 14. Standard 50 Ω Load CML Interface

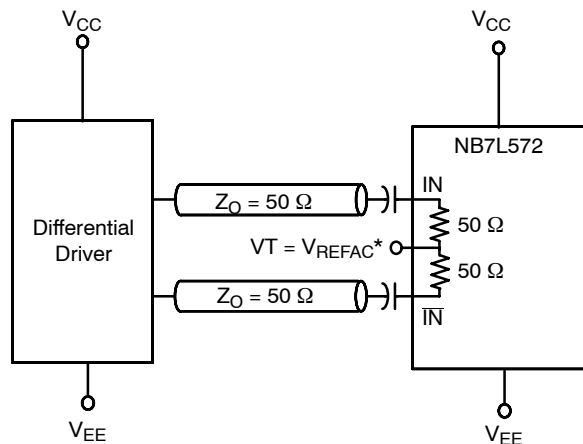


Figure 15. Capacitor-Coupled Differential Interface
(VT Connected to V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μ F capacitor

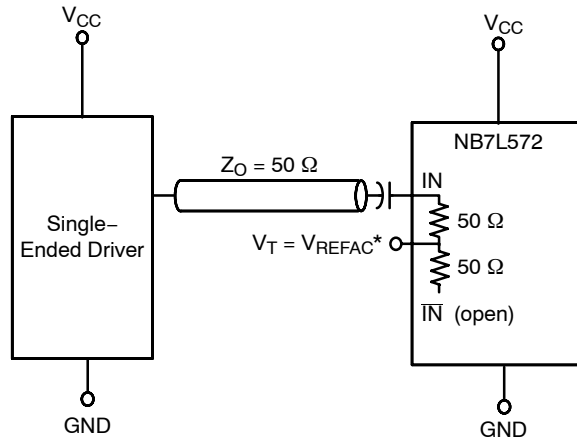


Figure 16. Capacitor-Coupled Single-Ended Interface
(VT Connected to External V_{REFAC})

NB7L572

ORDERING INFORMATION

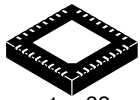
Device	Package	Shipping†
NB7L572MNG	QFN32 (Pb-Free)	79 Units / Rail
NB7L572MNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

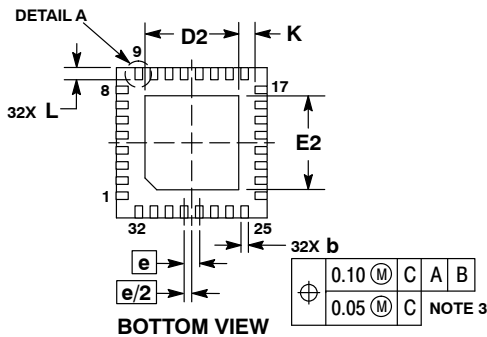
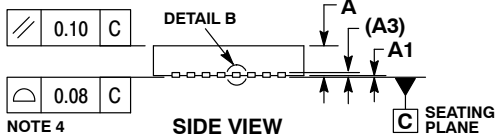
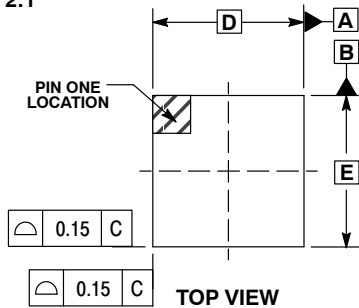
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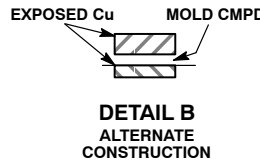
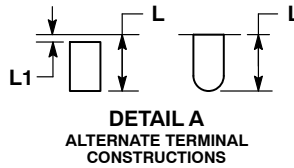
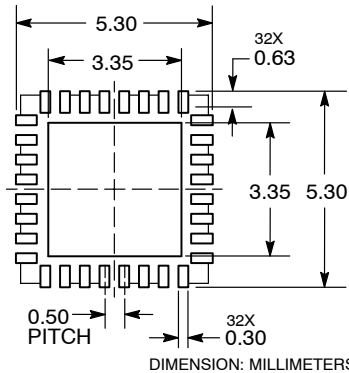
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SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



RECOMMENDED SOLDERING FOOTPRINT*

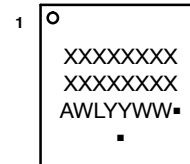


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.18	0.30
D	5.00	BSC
D2	2.95	3.25
E	5.00	BSC
E2	2.95	3.25
e	0.50	BSC
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	QFN32 5x5 0.5P	PAGE 1 OF 1

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