

# Low Voltage Single Supply SPDT Analog Switch

## NLAST4599

The NLAST4599 is an advanced high speed CMOS single pole – double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power–supply range (from  $V_{CC}$  to GND).

The device has been designed so the ON resistance ( $R_{ON}$ ) is much lower and more linear over input voltage than  $R_{ON}$  of typical CMOS analog switches.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- Select Pin Compatible with TTL Levels
- Channel Select Input Over–Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break–Before–Make Circuitry
- Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25^\circ C$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch–up Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V
- Chip Complexity: 38 FETs
- NLVAST Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

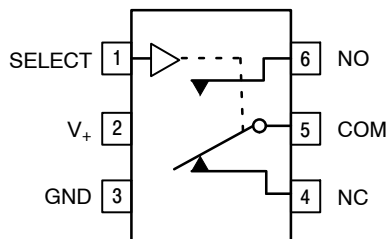


Figure 1. Pin Assignment

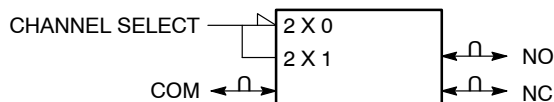
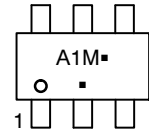


Figure 2. Logic Symbol

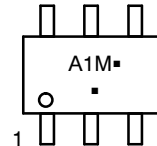
### MARKING DIAGRAMS



TSOP–6  
DT SUFFIX  
CASE 318G



SC–88/SC–70/SOT–363  
DF SUFFIX  
CASE 419B



- A1 = Specific Device Code
- A = Assembly Location
- M = Date Code\*
- = Pb–Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position and underbar may vary depending upon manufacturing location.

### FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# NLAST4599

## MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive DC Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
Analog Input Voltage ( $V_{NO}$ or $V_{COM}$ )	$V_{IS}$	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
Digital Select Input Voltage	$V_{IN}$	$-0.5 \leq V_I \leq +7.0$	V
DC Current, Into or Out of Any Pin	$I_{IK}$	$\pm 50$	mA
Power Dissipation in Still Air	$P_D$	200 200	mW
	SC-88 TSOP6		
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature, 1mm from Case for 10 seconds	$T_L$	260	°C
Junction Temperature Under Bias	$T_J$	150	°C
ESD Withstand Voltage	$V_{ESD}$	2000 200 N/A	V
	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)		
Latchup Performance	$I_{LATCHUP}$	$\pm 300$	mA
	Above $V_{CC}$ and Below GND at 125°C (Note 5)		
Thermal Resistance	$\theta_{JA}$	333 333	°C/W
	SC-88 TSOP6		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	$V_{CC}$	2.0	5.5	V
Digital Select Input Voltage	$V_{IN}$	GND	5.5	V
Analog Input Voltage (NC, NO, COM)	$V_{IS}$	GND	$V_{CC}$	V
Operating Temperature Range	$T_A$	-55	+125	°C
Input Rise or Fall Time SELECT	$t_r, t_f$	0 0	100 20	ns/V
	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$			

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

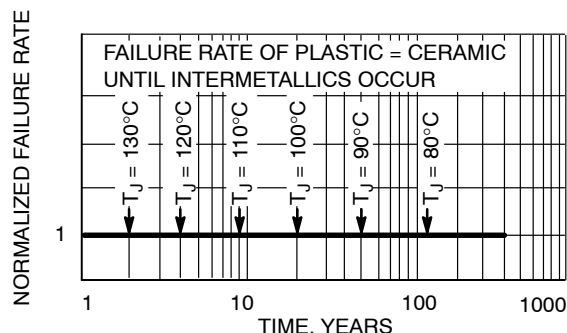


Figure 3. Failure Rate vs. Time Junction Temperature

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## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V <sub>CC</sub>	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
Minimum High-Level Input Voltage, Select Input		V <sub>IH</sub>	3.0	2.0	2.0	2.0	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
Maximum Low-Level Input Voltage, Select Input		V <sub>IL</sub>	3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
Maximum Input Leakage Current, Select Input	V <sub>IN</sub> = 5.5 V or GND	I <sub>IN</sub>	5.5	±0.1	±1.0	±1.0	µA
Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or GND	I <sub>OFF</sub>	0	±10	±10	±10	µA
Maximum Quiescent Supply Current	Select and V <sub>IS</sub> = V <sub>CC</sub> or GND	I <sub>CC</sub>	5.5	1.0	1.0	2.0	µA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Condition	Symbol	V <sub>CC</sub>	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
Maximum "ON" Resistance (Figures 17 – 23)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = GND to V <sub>CC</sub>  I <sub>IN</sub>   ≤ 10.0 mA	R <sub>ON</sub>	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
ON Resistance Flatness (Figures 17 – 23)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>IN</sub>   ≤ 10.0 mA V <sub>IS</sub> = 1V, 2V, 3.5V	R <sub>FLAT (ON)</sub>	4.5	4	4	5	Ω
ON Resistance Match Between Channels	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>IN</sub>   ≤ 10.0 mA V <sub>NO</sub> or V <sub>NC</sub> = 3.5 V	ΔR <sub>ON (ON)</sub>	4.5	2	2	3	Ω
NO or NC Off Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> or V <sub>NC</sub> = 1.0 V <sub>COM</sub> 4.5 V	I <sub>NC(OFF)</sub> I <sub>NO(OFF)</sub>	5.5	1	10	100	nA
COM ON Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> 1.0 V or 4.5 V with V <sub>NC</sub> floating or V <sub>NO</sub> 1.0 V or 4.5 V with V <sub>NO</sub> floating V <sub>COM</sub> = 1.0 V or 4.5 V	I <sub>COM(ON)</sub>	5.5	1	10	100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Parameter	Test Conditions	Symbol	$V_{CC}$ (V)	$V_{IS}$ (V)	Guaranteed Max Limit						Unit	
					-55 to 25°C			<85°C		<125°C		
					Min	Typ*	Max	Min	Max	Min		Max
Turn-On Time (Figures 12 and 13)	$R_L = 300 \Omega$ , $C_L = 35$ pF (Figures 5 and 6)	$t_{ON}$	2.5	2.0	5	23	28	5	30	5	30	ns
			3.0	2.0	5	16	21	5	25	5	25	
			4.5	3.0	2	11	16	2	20	2	20	
			5.5	3.0	2	9	14	2	20	2	20	
Turn-Off Time (Figures 12 and 13)	$R_L = 300 \Omega$ , $C_L = 35$ pF (Figures 5 and 6)	$t_{OFF}$	2.5	2.0	1	7	12	1	15	1	15	ns
			3.0	2.0	1	5	10	1	15	1	15	
			4.5	3.0	1	4	9	1	12	1	12	
			5.5	3.0	1	3	8	1	12	1	12	
Minimum Break-Before-Make Time	$V_{IS} = 3.0$ V (Figure 4) $R_L = 300 \Omega$ , $C_L = 35$ pF	$t_{BBM}$	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		
<b>Typical @ 25, VCC = 5.0 V</b>												
Maximum Input Capacitance, Select Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)		$C_{IN}$ $C_{NO}$ or $C_{NC}$ $C_{COM}$ $C_{(ON)}$						8 10 10 20			pF	

\*Typical Characteristics are at 25°C.

## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Parameter	Condition	Symbol	$V_{CC}$ V	Typical 25°C	Unit
Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm $V_{IN}$ centered between $V_{CC}$ and GND (Figure 7)	BW	3.0 4.5 5.5	170 200 200	MHz
Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz $V_{IN}$ centered between $V_{CC}$ and GND (Figure 7)	$V_{ONL}$	3.0 4.5 5.5	-2 -2 -2	dB
Off-Channel Isolation (Figure 10)	$f = 100$ kHz; $V_{IS} = 1$ V RMS $V_{IN}$ centered between $V_{CC}$ and GND (Figure 7)	$V_{ISO}$	3.0 4.5 5.5	-93 -93 -93	dB
Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$ , $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$ , (Figure 8)	Q	3.0 5.5	1.5 3.0	pC
Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = R_{gen} = 600 \Omega$ , $C_L = 50$ pF $V_{IS} = 5.0$ V <sub>PP</sub> sine wave	THD	5.5	0.1	%

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NLAST4599DFT2G	SC-88/SC-70/SOT-363 (Pb-Free)	3000 / Tape & Reel
NLAST4599DTT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NLVA54599DTT1G*		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLVAST Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

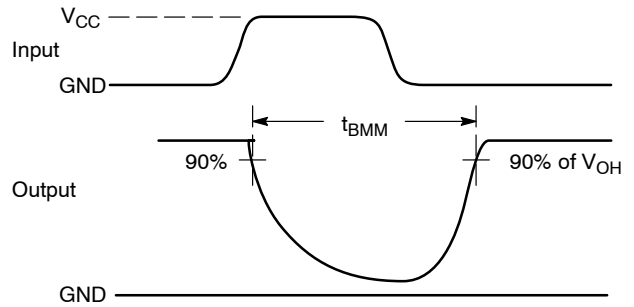
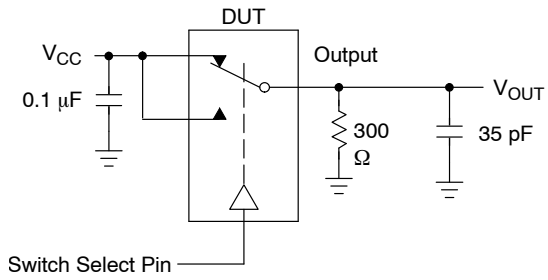


Figure 4.  $t_{BMM}$  (Time Break-Before-Make)

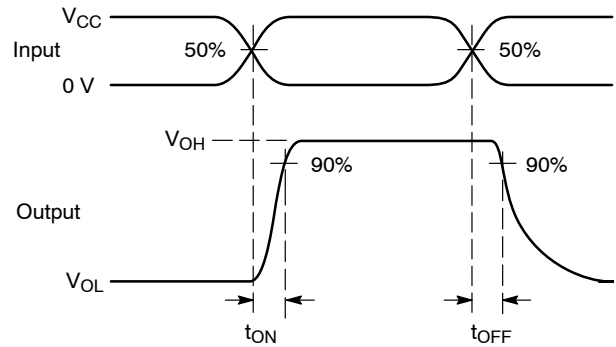
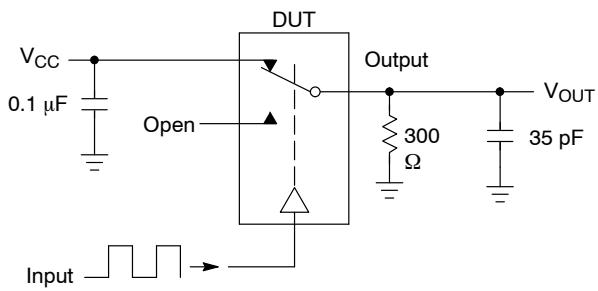


Figure 5.  $t_{ON}/t_{OFF}$

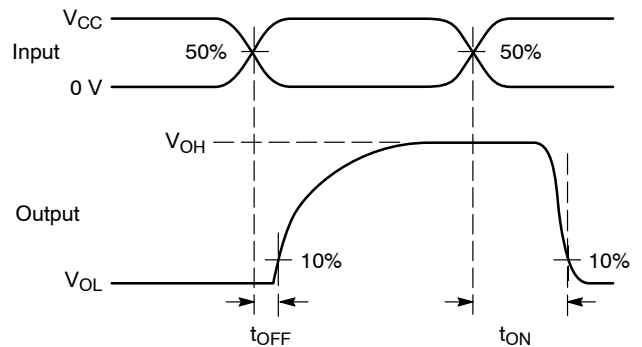
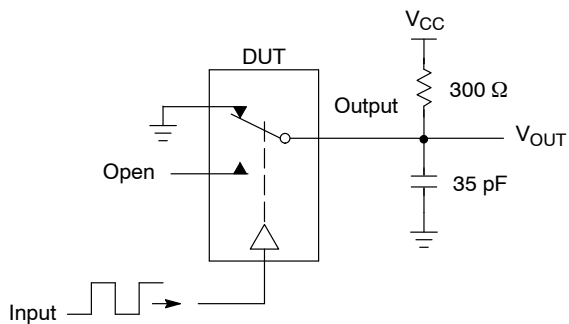
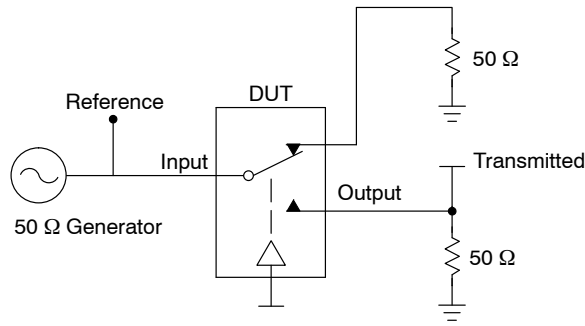


Figure 6.  $t_{ON}/t_{OFF}$

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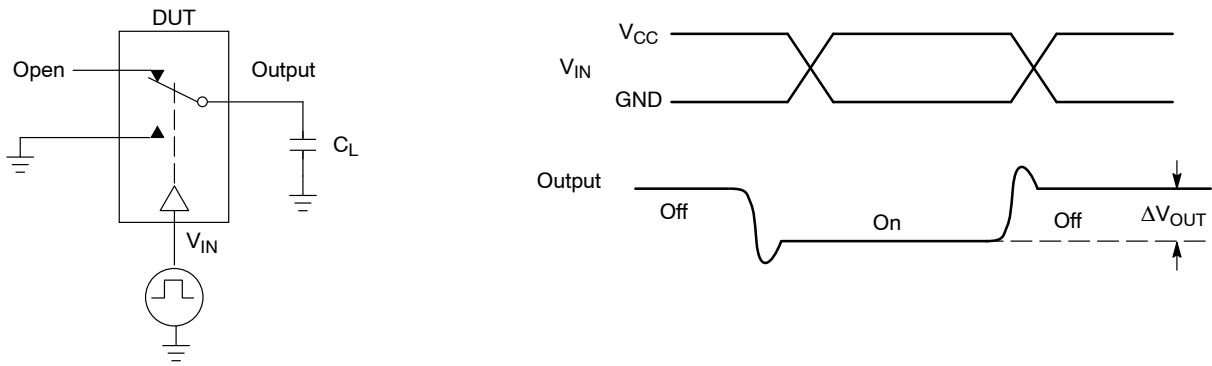
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

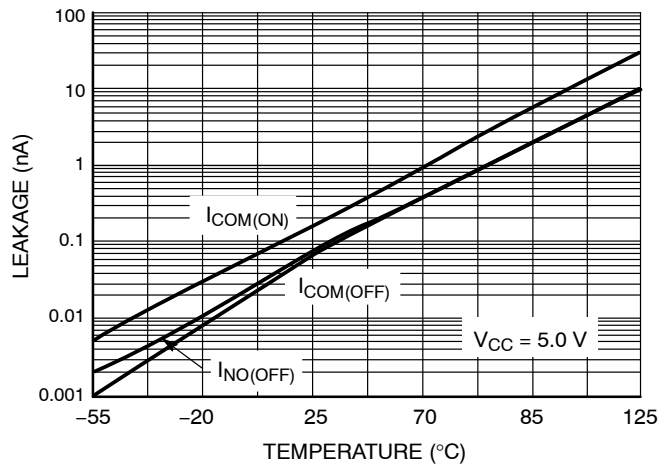
$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

**Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**



**Figure 8. Charge Injection: (Q)**



**Figure 9. Switch Leakage vs. Temperature**

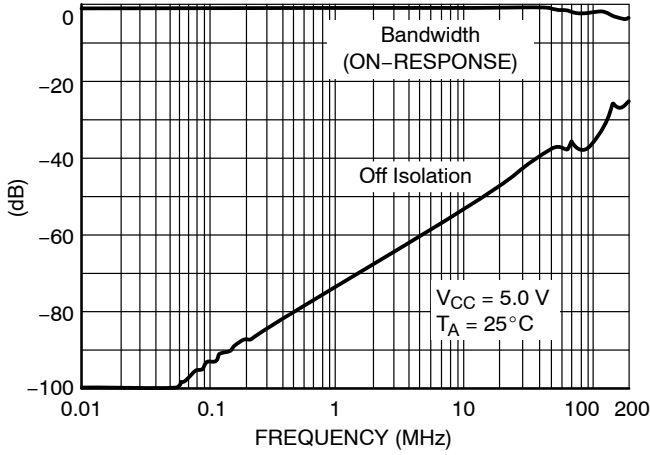


Figure 10. Bandwidth and Off-Channel Isolation

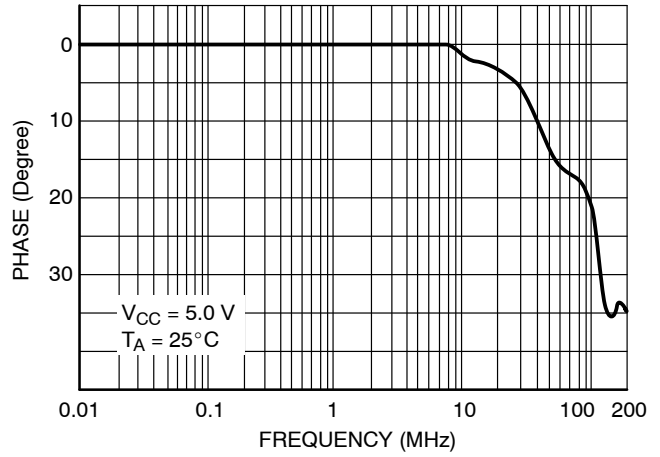


Figure 11. Phase vs. Frequency

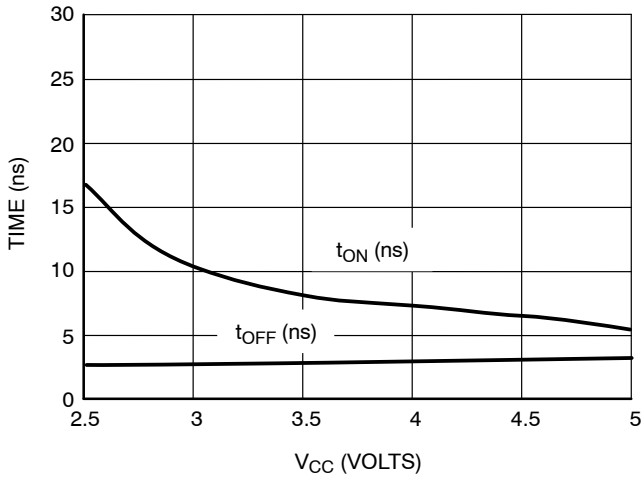


Figure 12.  $t_{ON}$  and  $t_{OFF}$  vs.  $V_{CC}$  at 25°C

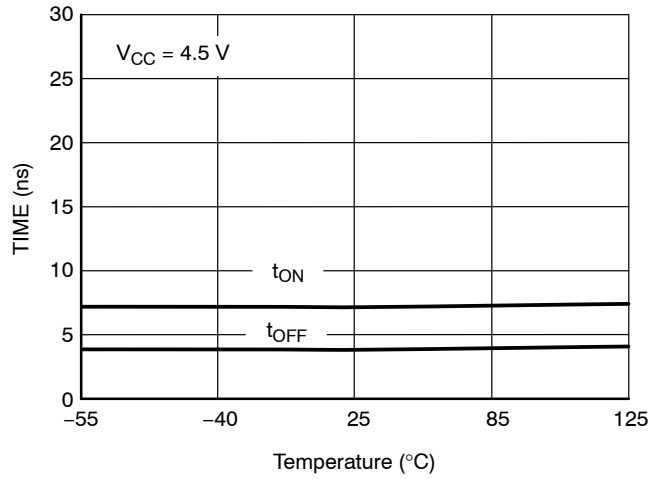


Figure 13.  $t_{ON}$  and  $t_{OFF}$  vs. Temp

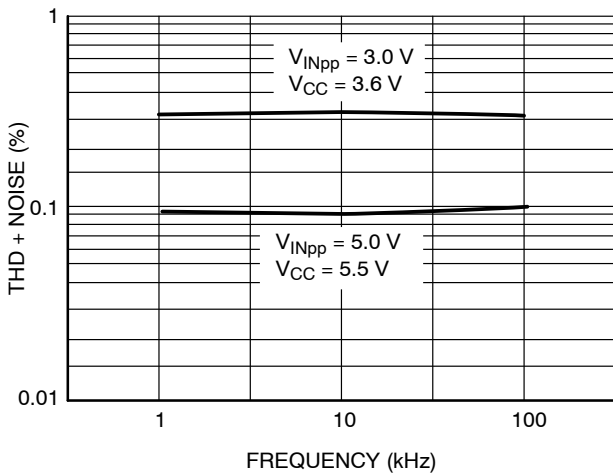


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

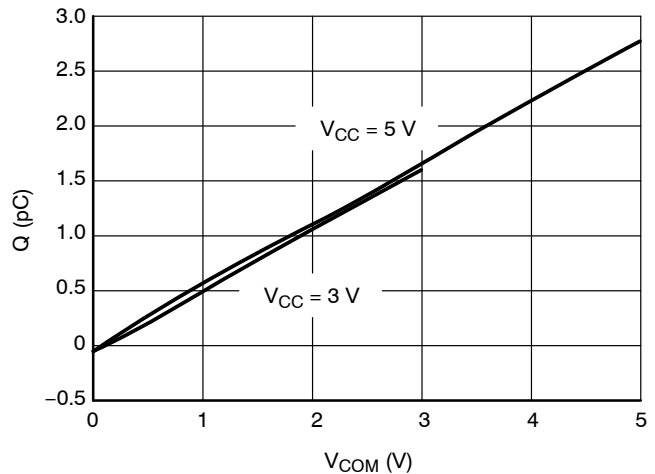


Figure 15. Charge Injection vs. COM Voltage

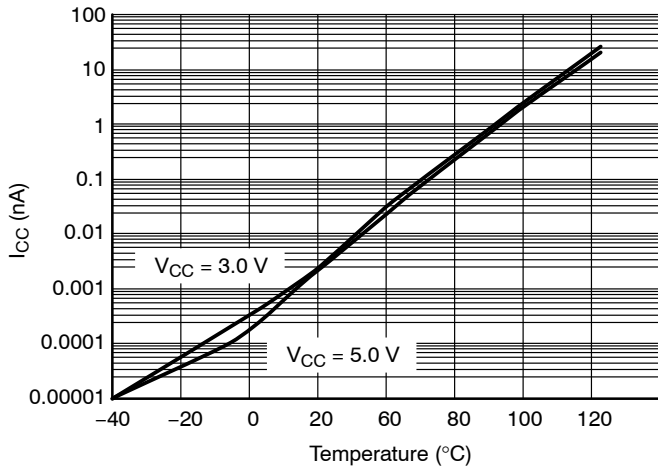


Figure 16.  $I_{CC}$  vs. Temp,  $V_{CC} = 3\text{ V}$  &  $5\text{ V}$

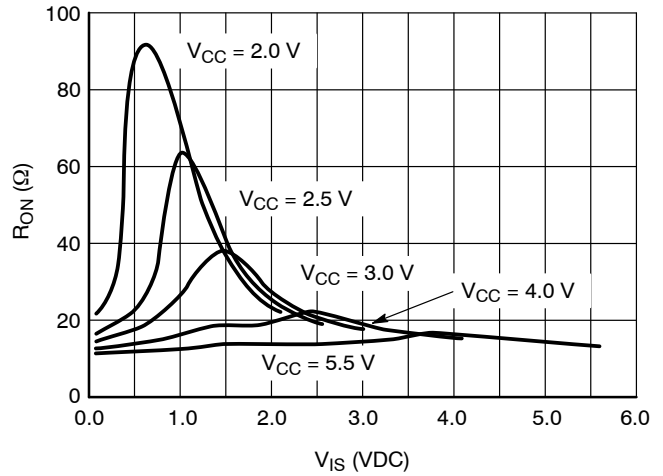


Figure 17.  $R_{ON}$  vs.  $V_{CC}$ , Temp =  $25^\circ\text{C}$

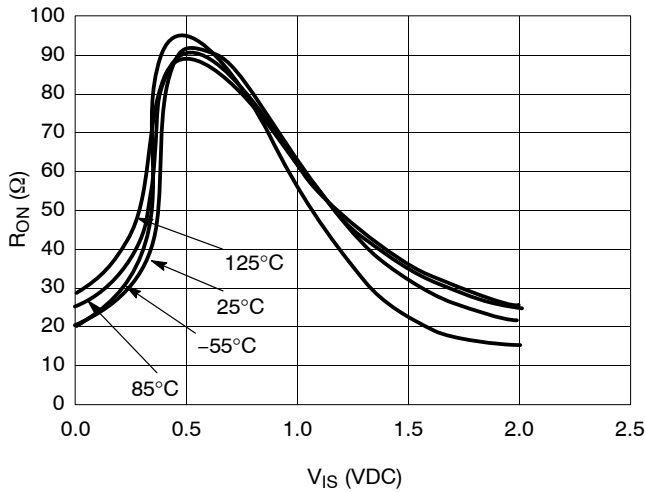


Figure 18.  $R_{ON}$  vs Temp,  $V_{CC} = 2.0\text{ V}$

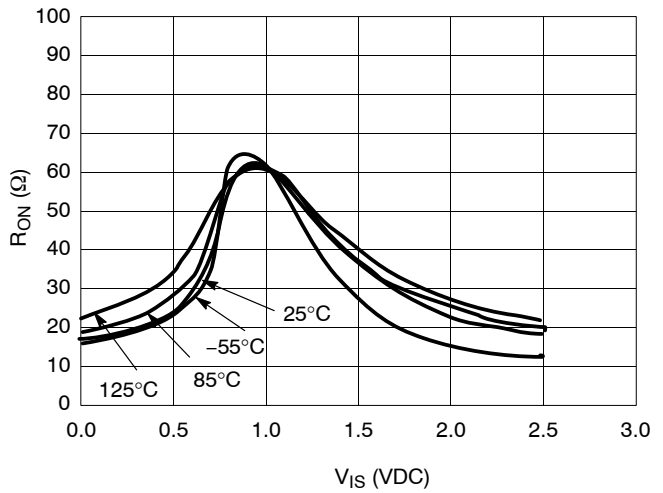


Figure 19.  $R_{ON}$  vs. Temp,  $V_{CC} = 2.5\text{ V}$

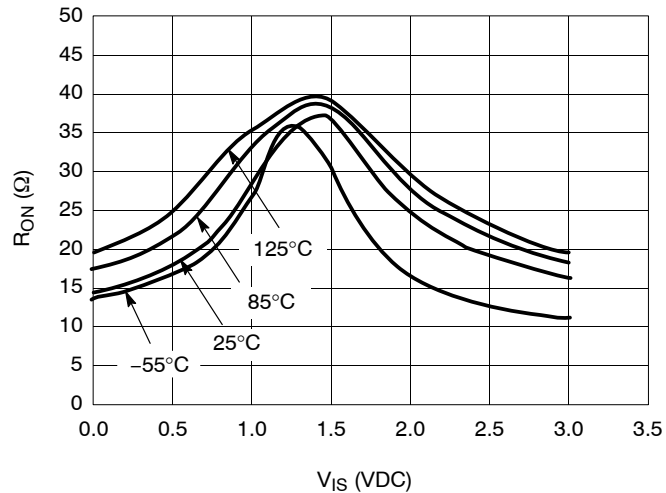


Figure 20.  $R_{ON}$  vs. Temp,  $V_{CC} = 3.0\text{ V}$

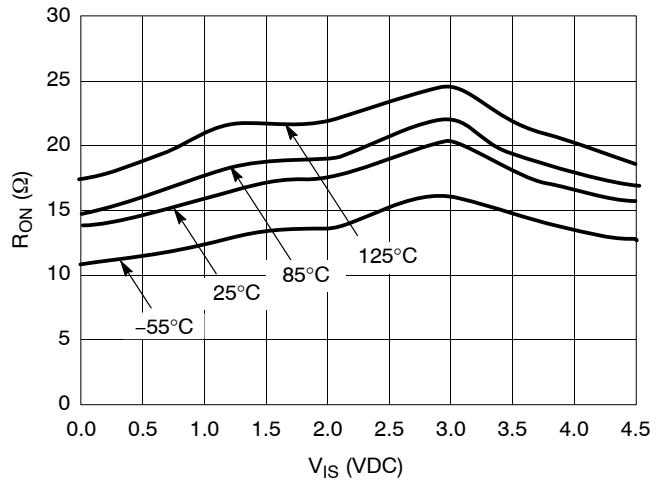


Figure 21.  $R_{ON}$  vs. Temp,  $V_{CC} = 4.5\text{ V}$



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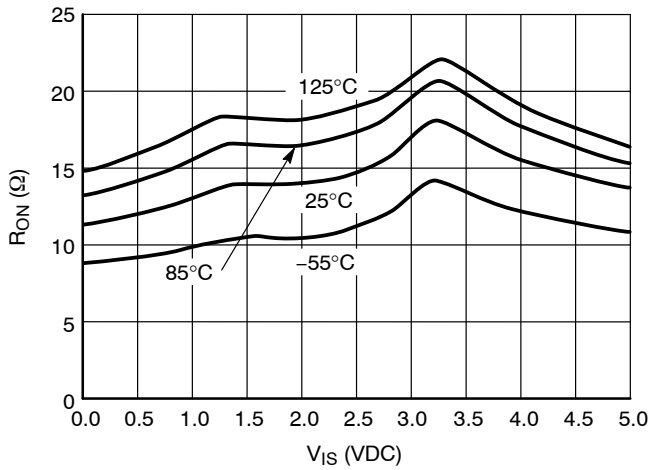


Figure 22.  $R_{ON}$  vs. Temp,  $V_{CC} = 5.0$  V

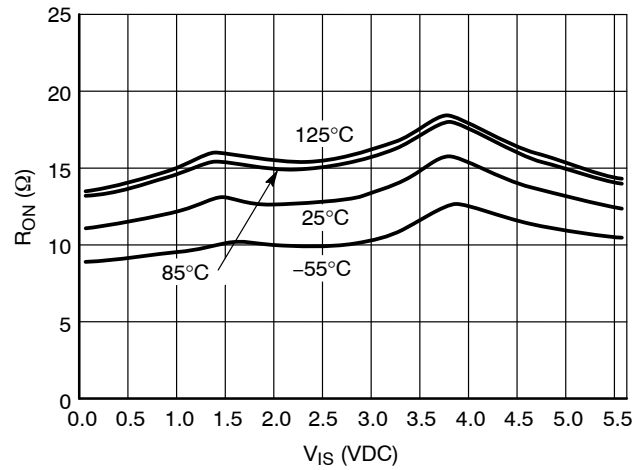


Figure 23.  $R_{ON}$  vs. Temp,  $V_{CC} = 5.5$  V

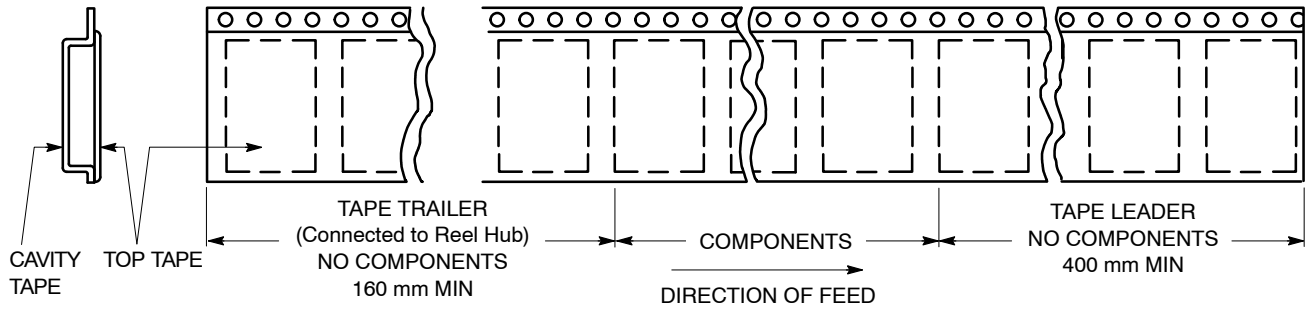


Figure 24. Tape Ends for Finished Goods

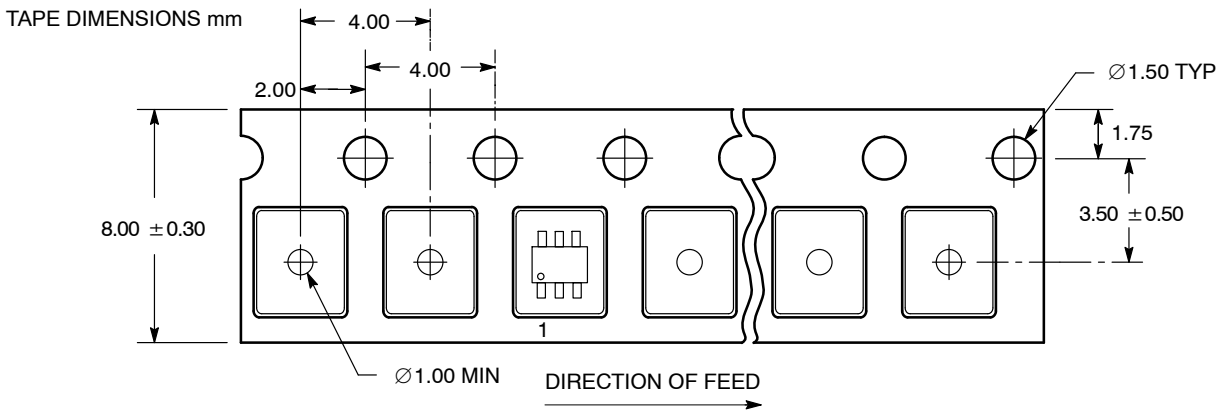


Figure 25. SC70-6/SC-88/SOT-363 DFT2 and SOT23-6/TSOP-6/SC59-6 DTT1 Reel Configuration/Orientation

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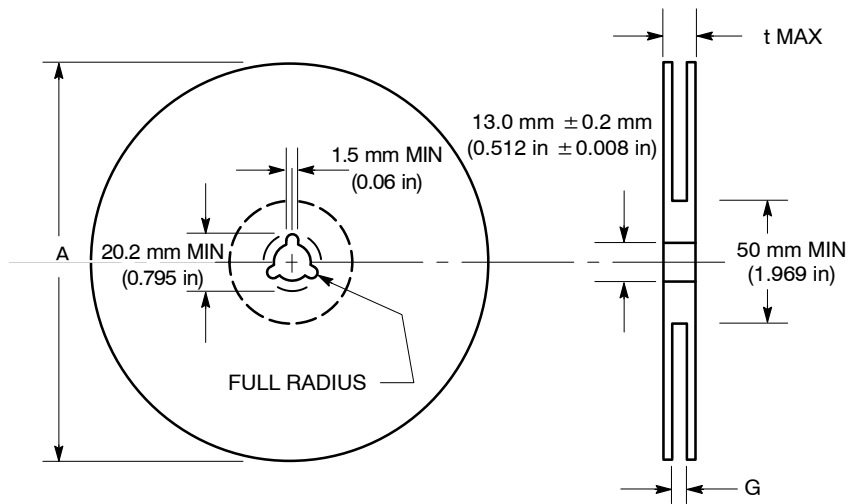


Figure 26. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

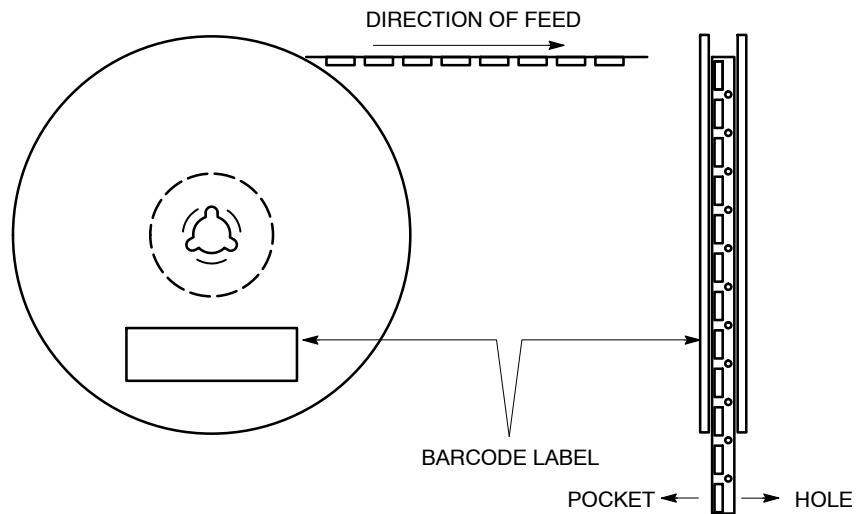


Figure 27. Reel Winding Direction

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

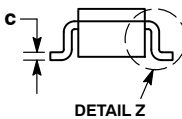
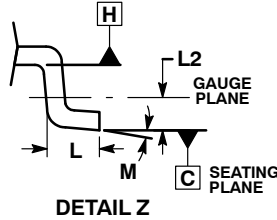
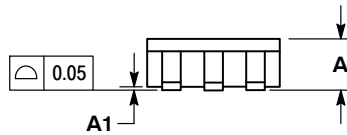
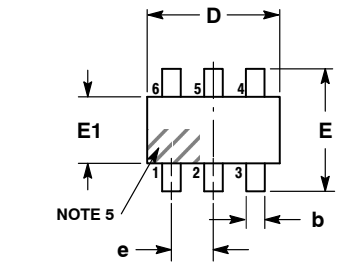
ON Semiconductor®



SCALE 2:1

### TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

STYLE 1:

1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:

1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:

1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:

1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:

1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:

1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:

1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:

1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:

1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:

1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+

STYLE 11:

1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:

1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:

1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:

1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:

1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

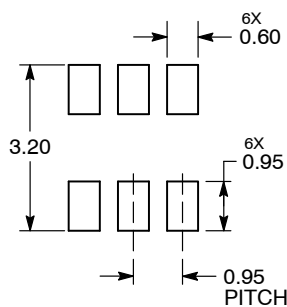
STYLE 16:

1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:

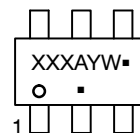
1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

### RECOMMENDED SOLDERING FOOTPRINT\*

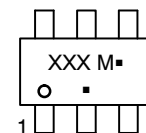


DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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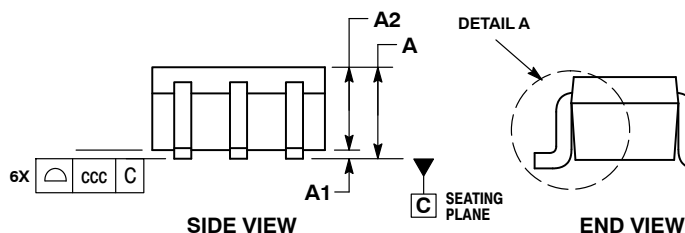
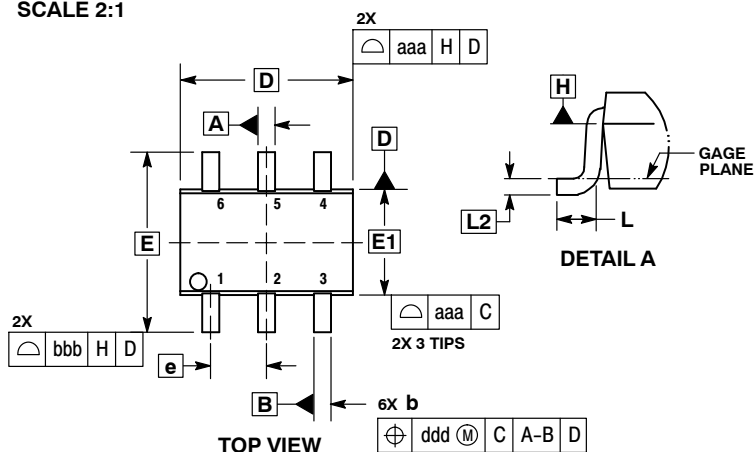
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1  
 SCALE 2:1

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 ISSUE Y

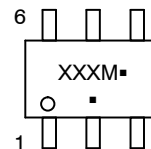
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**GENERIC MARKING DIAGRAM\***



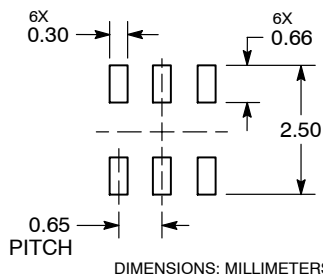
XXX = Specific Device Code  
 M = Date Code\*  
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**SC-88/SC70-6/SOT-363**  
**CASE 419B-02**  
**ISSUE Y**

DATE 11 DEC 2012

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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