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74VCX162244

Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistor in Outputs

General Description

The VCX162244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74VCX162244 is designed for low voltage (1.2V to 3.6V) V_{CC} applications with I/O capability up to 3.6V. The 74VCX162244 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74VCX162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.2V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD}
3.3 ns max for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal
- Static Drive (I_{OH}/I_{OL})
±12 mA @ 3.0V V_{CC}
- Uses proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

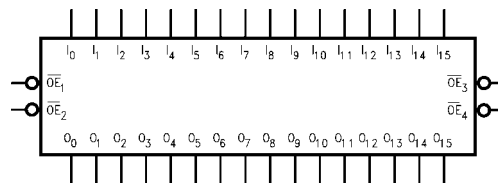
Ordering Code:

| Order Number | Package Number | Package Description |
|----------------------------------|----------------|---|
| 74VCX162244G (Note 2)(Note 3) | BGA54A | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide |
| 74VCX162244MTD (Note 3) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Note 2: Ordering Code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

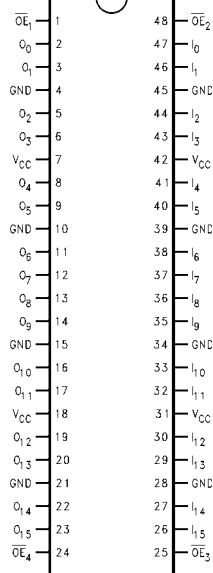
Logic Symbol



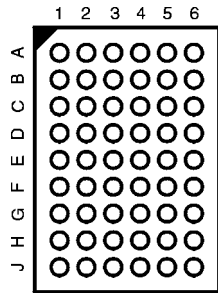
74VCX162244 Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistor in Outputs

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

| Pin Names | Description |
|-------------------|----------------------------------|
| \overline{OE}_n | Output Enable Input (Active LOW) |
| I_0-I_{15} | Inputs |
| O_0-O_{15} | Outputs |
| NC | No Connect |

FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|----------|----------|-------------------|-------------------|----------|----------|
| A | O_0 | NC | \overline{OE}_1 | \overline{OE}_2 | NC | I_0 |
| B | O_2 | O_1 | NC | NC | I_1 | I_2 |
| C | O_4 | O_3 | V_{CC} | V_{CC} | I_3 | I_4 |
| D | O_6 | O_5 | GND | GND | I_5 | I_6 |
| E | O_8 | O_7 | GND | GND | I_7 | I_8 |
| F | O_{10} | O_9 | GND | GND | I_9 | I_{10} |
| G | O_{12} | O_{11} | V_{CC} | V_{CC} | I_{11} | I_{12} |
| H | O_{14} | O_{13} | NC | NC | I_{13} | I_{14} |
| J | O_{15} | NC | \overline{OE}_4 | \overline{OE}_3 | NC | I_{15} |

Truth Tables

| Inputs | | Outputs |
|-------------------|-----------|-----------|
| \overline{OE}_1 | I_0-I_3 | O_0-O_3 |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|-------------------|-----------|-----------|
| \overline{OE}_2 | I_4-I_7 | O_4-O_7 |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|-------------------|--------------|--------------|
| \overline{OE}_3 | I_8-I_{11} | O_8-O_{11} |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|-------------------|-----------------|-----------------|
| \overline{OE}_4 | $I_{12}-I_{15}$ | $O_{12}-O_{15}$ |
| L | L | L |
| L | H | H |
| H | X | Z |

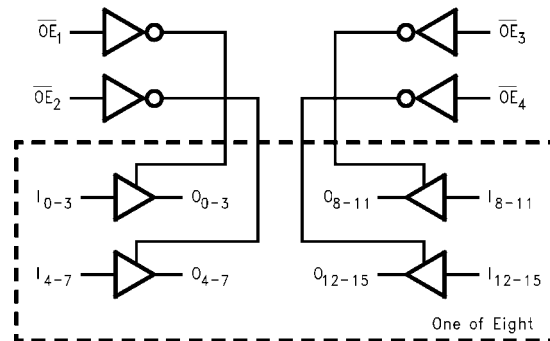
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Functional Description

The 74VCX162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram



Absolute Maximum Ratings (Note 4)

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +4.6V |
| DC Input Voltage (V_I) | -0.5V to +4.6V |
| Output Voltage (V_O) | |
| Outputs 3-STATE | -0.5V to +4.6V |
| Outputs Active (Note 5) | -0.5V to $V_{CC} + 0.5V$ |
| DC Input Diode Current (I_{IK}) $V_I < 0V$ | -50 mA |
| DC Output Diode Current (I_{OK}) | |
| $V_O < 0V$ | -50 mA |
| $V_O > V_{CC}$ | +50 mA |
| DC Output Source/Sink Current | |
| (I_{OH}/I_{OL}) | ± 50 mA |
| DC V_{CC} or GND Current per | |
| Supply Pin (I_{CC} or GND) | ± 100 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |

Recommended Operating Conditions (Note 6)

| | |
|---|-------------------|
| Power Supply | |
| Operating | 1.2V to 3.6V |
| Data Retention Only | 1.2V to 3.6V |
| Input Voltage | -0.3V to +3.6V |
| Output Voltage (V_O) | |
| Output in Active States | 0V to V_{CC} |
| Output in 3-State | 0.0V to 3.6V |
| Output Current in I_{OH}/I_{OL} | |
| $V_{CC} = 3.0V$ to 3.6V | ± 12 mA |
| $V_{CC} = 2.3V$ to 2.7V | ± 8 mA |
| $V_{CC} = 1.65V$ to 2.3V | ± 3 mA |
| $V_{CC} = 1.4V$ to 1.6V | ± 2 mA |
| $V_{CC} = 1.2V$ | ± 100 μ A |
| Free Air Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate ($\Delta t/\Delta V$) | |
| $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$ | 10 ns/V |

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} \leq 3.6V)

| Symbol | Parameter | Conditions | V_{CC} (V) | Min | Max | Units |
|----------|---------------------------|--|-----------------|----------------------|----------------------|-------|
| V_{IH} | HIGH Level Input Voltage | | 2.7 - 3.6 | 2.0 | | V |
| | | | 2.3 - 2.7 | 1.6 | | |
| | | | 1.65 - 2.3 | $0.65 \times V_{CC}$ | | |
| | | | 1.4 - 1.6 | $0.65 \times V_{CC}$ | | |
| | | | 1.2 | $0.65 \times V_{CC}$ | | |
| V_{IL} | LOW Level Input Voltage | | 2.7 - 3.6 | | 0.8 | V |
| | | | 2.3 - 2.7 | | 0.7 | |
| | | | 1.65 - 2.3 | | $0.35 \times V_{CC}$ | |
| | | | 1.4 - 1.6 | | $0.35 \times V_{CC}$ | |
| | | | 1.2 | | $0.5 \times V_{CC}$ | |
| V_{OH} | HIGH Level Output Voltage | $I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA | 2.7 - 3.6 | $V_{CC} - 0.2$ | | V |
| | | | 2.7 | 2.2 | | |
| | | | 3.0 | 2.4 | | |
| | | | 3.0 | 2.2 | | |
| | | $I_{OH} = -100 \mu A$ $I_{OH} = -4$ mA $I_{OH} = -6$ mA $I_{OH} = -8$ mA | 2.7 - 3.6 | $V_{CC} - 0.2$ | | |
| | | | 2.3 | 2.0 | | |
| | | | 2.3 | 1.8 | | |
| | | | 2.3 | 1.7 | | |
| | | $I_{OH} = -100 \mu A$ $I_{OH} = -3$ mA | 1.65 - 2.3 | $V_{CC} - 0.2$ | | |
| | | | 1.65 | 1.25 | | |
| | | $I_{OH} = -100 \mu A$ $I_{OH} = -1$ mA | 1.4 - 1.6 | $V_{CC} - 0.2$ | | |
| | | | 1.4 | 1.05 | | |
| | | $I_{OH} = -100 \mu A$ | 1.2 | $V_{CC} - 0.1$ | | |

| DC Electrical Characteristics (2.7V < VCC ≤ 3.6V) (Continued) | | | | | | | |
|---|---------------------------------------|--|------------------------|--|-----------|-------|--------------------|
| Symbol | Parameter | Conditions | V _{CC} (V) | Min | Max | Units | |
| V _{OL} | LOW Level Output Voltage | I _{OL} = 100 μA | 2.7 - 3.6 | | 0.2 | V | |
| | | I _{OL} = 6 mA | 2.7 | | 0.4 | | |
| | | I _{OL} = 8 mA | 3.0 | | 0.55 | | |
| | | I _{OL} = 12 mA | 3.0 | | 0.8 | | |
| | | I _{OL} = 100 μA | 2.7 - 3.6 | | 0.2 | | |
| | | I _{OL} = 6 mA | 2.3 | | 0.4 | | |
| | | I _{OL} = 8 mA | 2.3 | | 0.6 | | |
| | | I _{OL} = 100 μA | 1.65 - 2.3 | | 0.2 | | |
| | | I _{OL} = 3 mA | 1.65 | | 0.3 | | |
| I _I | Input Leakage Current | 0 ≤ V _I ≤ 3.6V | 1.2 - 3.6 | | ±5.0 | μA | |
| | | I _{OZ} | 3-STATE Output Leakage | 0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL} | 1.2 - 3.6 | | ±10 |
| I _{OFF} | Power-OFF Leakage Current | 0 ≤ (V _I , V _O) ≤ 3.6V | 0 | | 10 | μA | |
| I _{CC} | Quiescent Supply Current | V _I = V _{CC} or GND | 1.2 - 3.6 | | 20 | μA | |
| | | V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 7) | 1.2 - 3.6 | | ±20 | μA | |
| ΔI _{CC} | Increase in I _{CC} per Input | V _{IH} = V _{CC} - 0.6V | 2.7 - 3.6 | | 750 | μA | |
| Note 7: Outputs disabled or 3-STATE only. | | | | | | | |
| AC Electrical Characteristics (Note 8) | | | | | | | |
| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = -40°C to +85°C | | Units | Figure Number |
| | | | | Min | Max | | |
| t _{PHL} , t _{PLH} | Propagation Delay | C _L = 30 pF, R _L = 500Ω | 3.3 ± 0.3 | 0.8 | 3.3 | ns | Figures 1, 2 |
| | | | 2.5 ± 0.2 | 1.0 | 3.8 | | |
| | | | 1.8 ± 0.15 | 1.5 | 7.6 | | |
| | | C _L = 15 pF, R _L = 2kΩ | 1.5 ± 0.1 | 1.0 | 15.2 | | Figures 5, 6 |
| | | | 1.2 | 1.5 | 38 | | |
| | | | | | | | |
| t _{PZL} , t _{PZH} | Output Enable Time | C _L = 30 pF, R _L = 500Ω | 3.3 ± 0.3 | 0.8 | 3.8 | ns | Figures 1, 3, 4 |
| | | | 2.5 ± 0.2 | 1.0 | 5.1 | | |
| | | | 1.8 ± 0.15 | 1.5 | 9.8 | | |
| | | C _L = 15 pF, R _L = 2kΩ | 1.5 ± 0.1 | 1.0 | 19.6 | | Figures 5, 7, 8 |
| | | | 1.2 | 1.5 | 49 | | |
| | | | | | | | |
| t _{PLZ} , t _{PHZ} | Output Disable Time | C _L = 30 pF, R _L = 500Ω | 3.3 ± 0.3 | 0.8 | 3.6 | ns | Figures 1, 3, 4 |
| | | | 2.5 ± 0.2 | 1.0 | 4.0 | | |
| | | | 1.8 ± 0.15 | 1.5 | 7.2 | | |
| | | C _L = 15 pF, R _L = 2kΩ | 1.5 ± 0.1 | 1.0 | 14.4 | | Figures 5, 7, 8 |
| | | | 1.2 | 1.5 | 36 | | |
| | | | | | | | |
| t _{OSSL} , t _{OSLH} | Output to Output Skew (Note 9) | C _L = 30 pF, R _L = 500Ω | 3.3 ± 0.3 | | 0.5 | ns | |
| | | | 2.5 ± 0.2 | | 0.5 | | |
| | | | 1.8 ± 0.15 | | 0.75 | | |
| | | C _L = 15 pF, R _L = 2kΩ | 1.5 ± 0.1 | | 1.5 | | |
| | | | 1.2 | | 1.5 | | |
| | | | | | | | |
| Note 8: For C _L = 50 pF, add approximately 300 ps to the AC maximum specification. | | | | | | | |
| Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t _{OSSL}) or LOW-to-HIGH (t _{OSLH}). | | | | | | | |

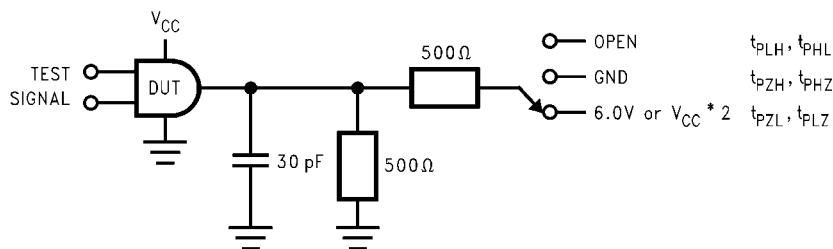
Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = +25°C | Units |
|------------------|---|--|------------------------|------------------------|-------|
| | | | | Typical | |
| V _{OLP} | Quiet Output Dynamic Peak V _{OL} | C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V | 1.8 | 0.15 | V |
| | | | 2.5 | 0.25 | |
| | | | 3.3 | 0.35 | |
| V _{OLV} | Quiet Output Dynamic Valley V _{OL} | C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V | 1.8 | -0.15 | V |
| | | | 2.5 | -0.25 | |
| | | | 3.3 | -0.35 | |
| V _{OHV} | Quiet Output Dynamic Valley V _{OH} | C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V | 1.8 | 1.55 | V |
| | | | 2.5 | 2.05 | |
| | | | 3.3 | 2.65 | |

Capacitance

| Symbol | Parameter | Conditions | T _A = +25°C | Units |
|------------------|-------------------------------|---|------------------------|-------|
| | | | Typical | |
| C _{IN} | Input Capacitance | V _{CC} = 1.8, 2.5V or 3.3V, V _I = 0V or V _{CC} | 6 | pF |
| C _{OUT} | Output Capacitance | V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V | 7 | pF |
| C _{PD} | Power Dissipation Capacitance | V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V | 20 | pF |

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



| TEST | SWITCH |
|--------------------|--|
| t_{PLH}, t_{PHL} | Open |
| t_{PZL}, t_{PLZ} | 6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8 \pm 0.15V$ |
| t_{PZH}, t_{PHZ} | GND |

FIGURE 1. AC Test Circuit

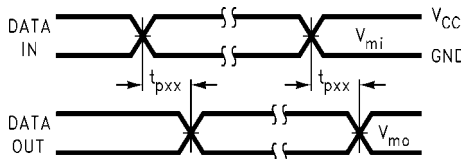


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

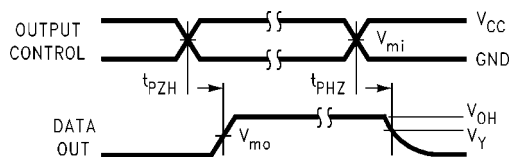


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

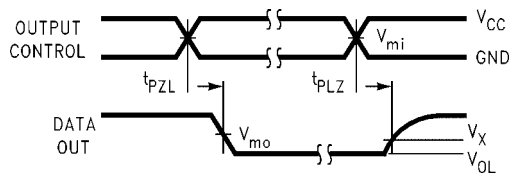
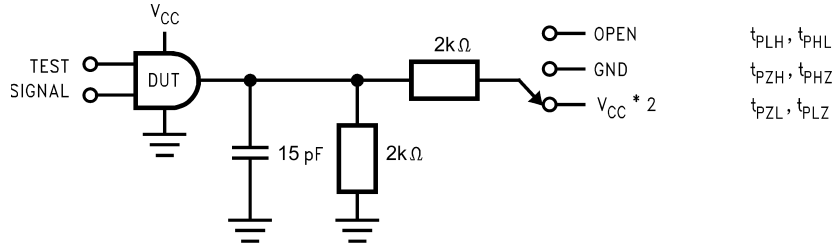


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

| Symbol | V_{CC} | | |
|----------|-----------------|------------------|------------------|
| | 3.3V ± 0.3V | 2.5V ± 0.2V | 1.8V ± 0.15V |
| V_{mi} | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| V_{mo} | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| V_X | $V_{OL} + 0.3V$ | $V_{OL} + 0.15V$ | $V_{OL} + 0.15V$ |
| V_Y | $V_{OH} - 0.3V$ | $V_{OH} - 0.15V$ | $V_{OH} - 0.15V$ |

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$ to $1.2V$)



| TEST | SWITCH |
|--------------------|---|
| t_{PLH}, t_{PHL} | Open |
| t_{PZL}, t_{PLZ} | $V_{CC} \times 2$ at $V_{CC} = 1.5V \pm 0.1V$ |
| t_{PZH}, t_{PHZ} | GND |

FIGURE 5. AC Test Circuit

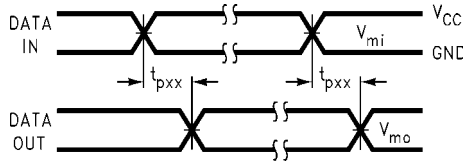


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

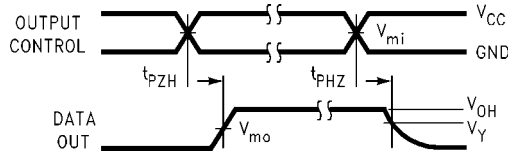


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

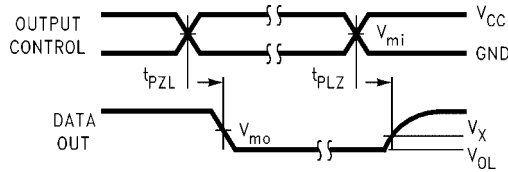
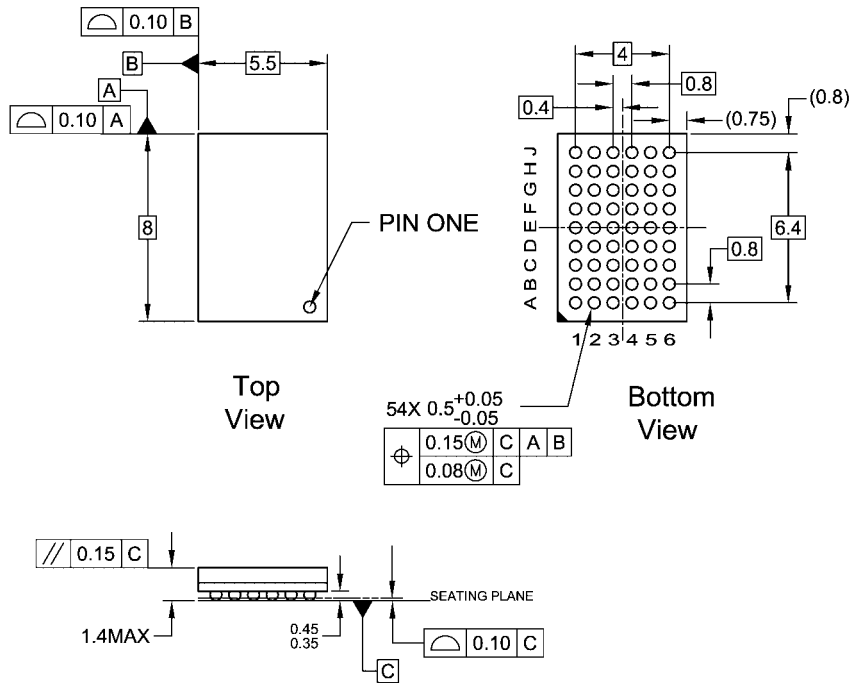


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

| Symbol | V_{CC} |
|----------|-----------------|
| | $1.5V \pm 0.1V$ |
| V_{mi} | $V_{CC}/2$ |
| V_{mo} | $V_{CC}/2$ |
| V_X | $V_{OL} + 0.1V$ |
| V_Y | $V_{OL} - 0.1V$ |

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REV C

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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