3 Amp V_{TT} Termination Regulator DDR1, DDR2, DDR3, LPDDR3, DDR4

NCP51403

The NCP51403 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low−noise systems where space is a key consideration.

The NCP51403 maintains a fast transient response and only requires a minimum output capacitance of 20 μF. The NCP51403 supports a remote sensing function and all power requirements for DDR V_{TT} bus termination. The NCP51403 can also be used in low−power chipsets and graphics processor cores that require dynamically adjustable output voltages.

The NCP51403 is available in the thermally−efficient DFN10 Exposed Pad package, and is rated both Green and Pb−free.

Features

- Input Voltage Rails: Supports 2.5 V, 3.3 V and 5 V Rails
- PV_{CC} Voltage Range: 1.1 to 3.5 V
- Integrated Power MOSFETs
- Phase Margin >45° with Recommended 20 μF V_{TT} Capacitance
- P_{GOOD} − Logic output pin to Monitor V_{TT} Regulation
- EN − Logic input pin for Shutdown mode
- V_{RI} − Reference Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (V_{TTS})
- Built−in Under Voltage Lockout and Over Current Limit
- Thermal Shutdown
- Small, Low−Profile 10−pin, 3x3 DFN Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD−TV/PDP−TV, Copier/Printers
- Chipset/RAM Supplies as Low as 0.5 V
- Active Bus Termination

DDR3/DDR4 SELECTOR GUIDE

	VTT Startup	DDR Level	VTT Droop	VTT Capacitor
NCP51400	Soft Start	3 / 4	Yes	Cer/Poly
NCP51401	<35usec	3 / 4	Yes	Cer/Poly
NCP51402	<35usec	4	No*	Cer/Poly
NCP51403	<35usec	4	No*	Cer/PM>45°

* Recommended for New DDR4 Designs

(see notes on page 7)

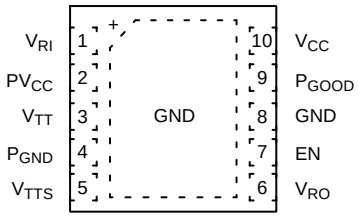
DFN10, 3x3, 0.5P
CASE 506CL

MARKING DIAGRAM

51403	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



Exposed Pad

ORDERING INFORMATION

Device	Package	Shipping†
NCP51403MNTXG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{RI}	V_{TT} External Reference Input (set to V_{DDQ} / 2 thru resistor network).
2	PV_{CC}	Power input. Internally connected to the output source MOSFET.
3	V_{TT}	Power Output of the Linear Regulator.
4	P_{GND}	Power Ground. Internally connected to the output sink MOSFET.
5	V_{TTS}	V_{TT} Sense Input. The V_{TTS} pin provides accurate remote feedback sensing of V_{TT}. Connect V_{TTS} to the remote DDR termination bypass capacitors.
6	V_{RO}	Independent Buffered V_{TT} Reference Output. Sources and sinks over 5 mA. Connect to GND thru 0.1 μF ceramic capacitor.
7	EN	Shutdown Control Input. CMOS compatible input. Logic high = enable, logic low = shutdown. Connect to V_{DDQ} for normal operation.
8	GND	Common Ground.
9	P_{GOOD}	Power Good (Open Drain output).
10	V_{CC}	Analog power supply input. Connect to GND thru a 1 − 4.7 μF ceramic capacitor.
	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}, PV_{CC}, V_{TT}, V_{TTS}, V_{RI}, V_{RO} (Note 1)		−0.3 to 6.0	V
EN, P_{GOOD} (Note 1)		−0.3 to 6.0	V
P_{GND} to GND (Note 1)		−0.3 to +0.3	V
Storage Temperature	T_{STG}	−55 to 150	°C
Operating Junction Temperature Range	T_J	150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following method:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

DISSIPATION RATINGS

Package	T_A = 25°C Power Rating	Derating Factor above T_A = 25°C	T_A = +85°C Power Rating
10−Pin DFN	1.92 W	19 mW/°C	0.79 W

RECOMMENED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.375 to 5.5	V
Voltage Range	V_{RO}	−0.1 to 1.8	V
	V_{RI}	0.5 to 1.8	
	PV_{CC}, V_{TT}, V_{TTS}, EN, P_{GOOD}	−0.1 to 3.5	
	P_{GND}	−0.1 to +0.1	
Operating Free−Air Temperature	T_A	−40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 125°C$; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; $V_{RI} = V_{TTS}$ = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 μF (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT						
V_{CC} Supply Current	T_A = +25°C, EN = 3.3 V, No Load	I_{VCC}		0.7	1	mA
V_{CC} Shutdown Current	T_A = +25°C, EN = 0 V, V_{RI} = 0 V, No Load	$I_{VCC\ SHD}$		65	80	μA
	T_A = +25°C, EN = 0 V, V_{RI} > 0.4 V, No Load			200	400	
V_{CC} UVLO Threshold	Wake−up, T_A = +25°C	V_{UVLO}	2.15	2.3	2.375	V
	Hysteresis			50		mV
PV_{CC} Supply Current	T_A = +25°C, EN = 3.3 V, No Load	I_{PVCC}		1	50	μA
PV_{CC} Shutdown Current	T_A = +25°C, EN = 0 V, No Load	$I_{PVCC\ SHD}$		0.1	50	μA
V_{TT} OUTPUT						
V_{TT} Output DC Voltage	PV_{CC} = 1.50 V, V_{RO} = 0.75 V, I_{TT} = 0 A	V_{OS}		0.75		mV
	PV_{CC} = 1.35 V, V_{RO} = 0.675 V, I_{TT} = 0 A			0.675		
	PV_{CC} = 1.20 V, V_{RO} = 0.60 V, I_{TT} = 0 A			0.60		
V_{TT} Output Tolerance to V_{RO} −2 A < I_{TT} < 2 A	PV_{CC} = 1.50 V, V_{RO} = 0.75 V		−18		+18	mV
	PV_{CC} = 1.20 V, V_{RO} = 0.60 V PV_{CC} = 1.35 V, V_{RO} = 0.675 V		−20		+20	
Source Current Limit	V_{TTS} = 90% * V_{RO}		3		4.5	A
Sink Current Limit	V_{TTS} = 110% * V_{RO}		3.5		5.5	A
V_{TT} Rise Time	Enable to V_{TT} = 95% of V_{RI}, V_{TT} has 100 μF ceramic cap load, V_{RI} = 600 mV			25	35	μs
Discharge MOSFET On−resistance	V_{RI} = 0 V, V_{TT} = 0.3 V, EN = 0 V, T_A = +25°C	R_{DIS}		18	25	Ω
V_{RI} − INPUT REFERENCE						
V_{RI} Voltage Range		V_{RI}	0.5		1.8	V
V_{RI} Input−bias Current	EN = 3.3 V	I_{RI}			+1	μA
V_{RI} UVLO Voltage	V_{RI} rising	$V_{RI\ UVLO}$	360	390	435	mV
	Hysteresis	$V_{RI\ HYS}$		60		
V_{RO} − OUTPUT REFERENCE						
V_{RO} Voltage				V_{RI}		V
V_{RO} Voltage Tolerance to V_{RI}	I_{RO} = ±10 mA, 0.6 V ≤ V_{RI} ≤ 1.25 V		−15		+15	mV
V_{RO} Source Current Limit	V_{RO} = 0 V		10	40		mA
V_{RO} Sink Current Limit	V_{RO} = 0 V		10	40		mA
P_{GOOD} − POWERGOOD COMPARATOR						
P_{GOOD} Lower Threshold	(with respect to V_{RO})		−23.5%	−20%	−17.5%	V/V
P_{GOOD} Upper Threshold	(with respect to V_{RO})		17.5%	20%	23.5%	
P_{GOOD} Hysteresis				5%		
P_{GOOD} Start−up Delay	Start−up rising edge, V_{TTS} within 15% of V_{RO}			2		ms
P_{GOOD} Leakage Current	$V_{TTS} = V_{RI}$ (P_{GOOD} = True) $P_{GOOD} = V_{CC}$ + 0.2 V				1	μA
P_{GOOD} = False Delay	V_{TTS} is beyond ±20% P_{GOOD} trip thresholds			10		μs
P_{GOOD} Output Low Voltage	I_{GOOD} = 4 mA				0.4	V

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ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 125°C$; V_{CC} = 3.3 V; PV_{CC} = 1.8 V; $V_{RI} = V_{TTS}$ = 0.9 V; EN = V_{CC}; C_{OUT} = 3 x 10 μF (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
EN − ENABLE LOGIC						
Logic Input Threshold	EN Logic high	V_{IH}	1.7			V
	EN Logic low	V_{IL}			0.3	
Hysteresis Voltage	EN pin	V_{ENHYS}		0.5		V
Logic Leakage Current	EN pin, T_A = +25°C	I_{ILEAK}	−1		+1	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}		150		°C
Thermal Shutdown Hysteresis		T_{SH}		25		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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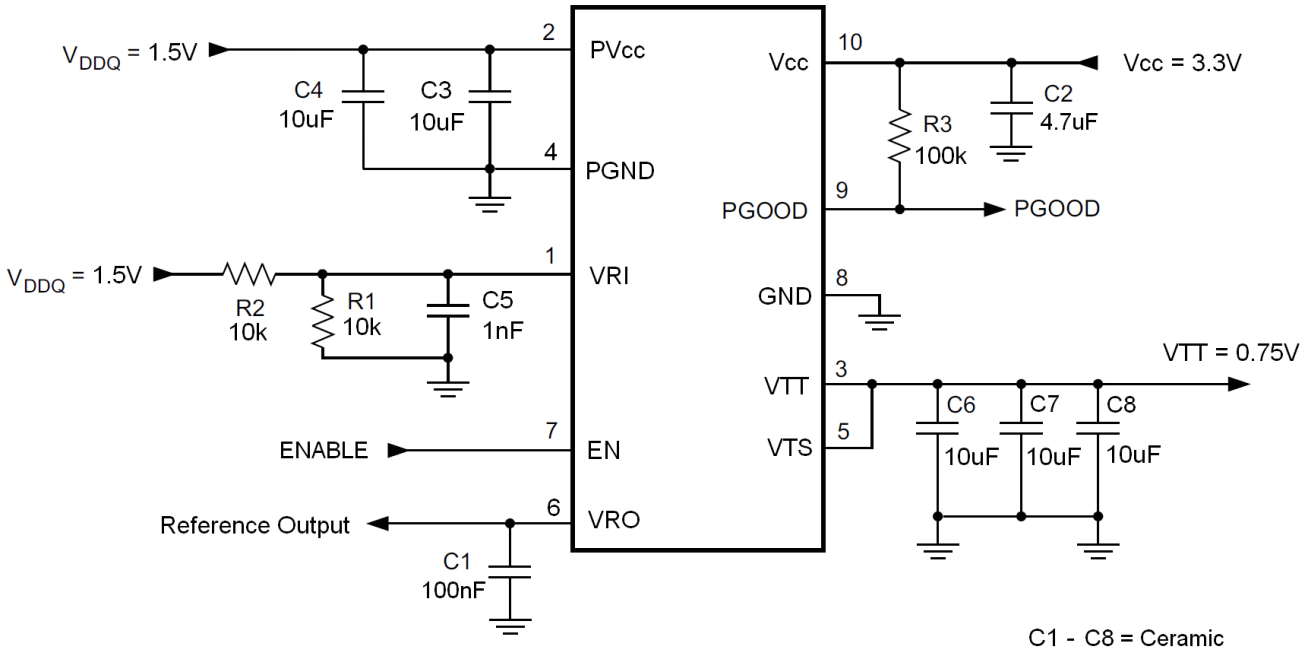

Figure 1. Typical DDR−3 Application Schematic

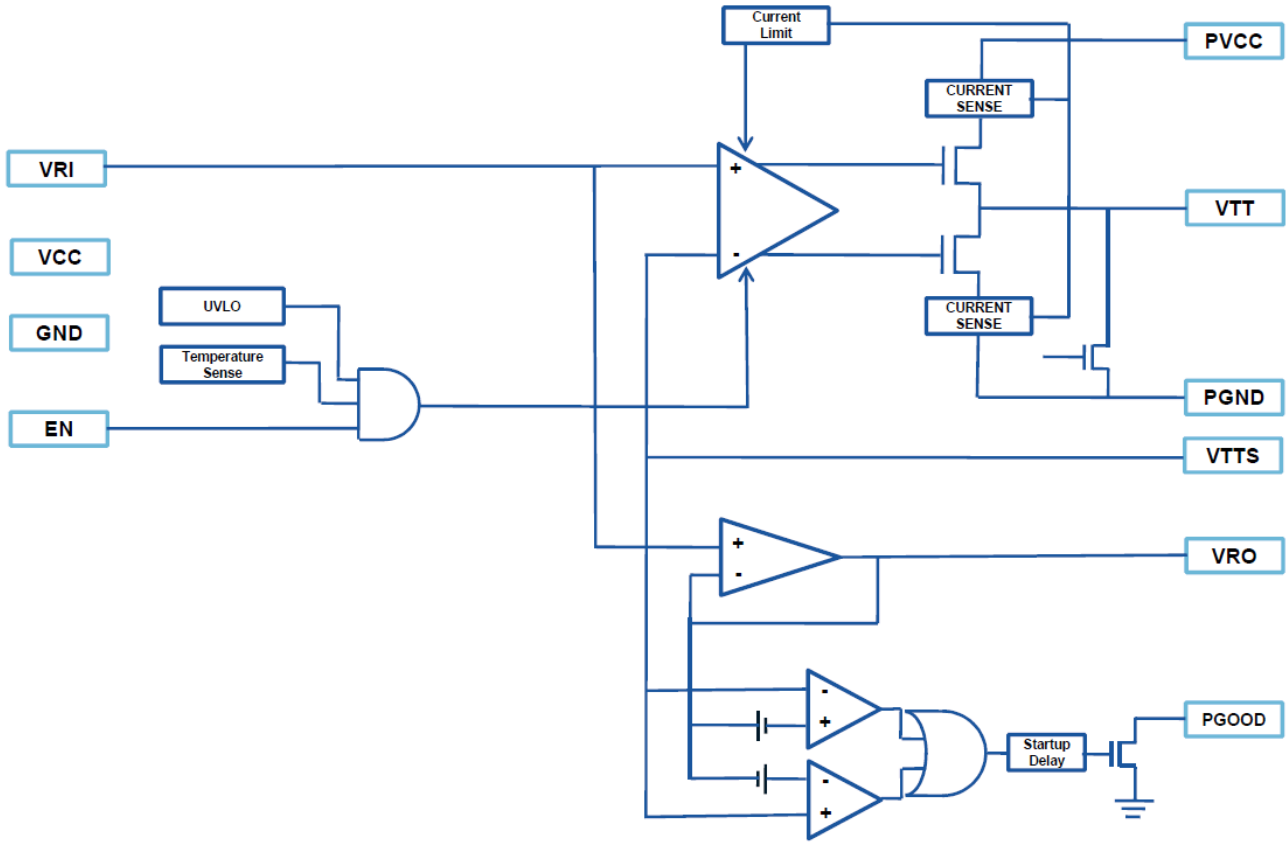

Figure 2. Block Diagram

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General

The NCP51403 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51403 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, V_{TTS}, should be connected to the positive terminal of the output capacitors as a separate trace from the high current path from V_{TT}.

V_{RI} − Generation of Internal Voltage Reference

The output voltage, V_{TT}, is regulated to V_{RO}. When V_{RI} is configured for standard DDR termination applications, V_{RI} can be set by an external equivalent ratio voltage divider connected to the memory supply bus (V_{DDQ}). The NCP51403 supports V_{RI} voltage from 0.5 V to 1.8 V, making it versatile and ideal for many types of low−power LDO applications.

V_{RO} − Reference Output

When it is configured for DDR termination applications, V_{RO} generates the DDR V_{TT} reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA. V_{RO} becomes active when V_{RI} voltage rises to 435 mV and V_{CC} is above the UVLO threshold. When V_{RO} is less than 360 mV, it is disabled and subsequently discharges to GND through an internal 10 kΩ MOSFET. V_{RO} is independent of the EN pin state.

EN − Enable Control

When EN is driven high, the NCP51403 V_{TT} regulator begins normal operation. When EN is driven low, V_{TT} is discharges to GND through an internal 18−Ω MOSFET. V_{REF} remains on when EN is driven low.

P_{GOOD} − PowerGood

The NCP51403 provides an open−drain P_{GOOD} output that goes high when the V_{TT} output is within ±20% of V_{RO}. P_{GOOD} de−asserts within 10 μs after the output exceeds the limits of the PowerGood window. During initial V_{TT} startup, P_{GOOD} asserts high 2 ms after the V_{TT} enters power good window. Because P_{GOOD} is an open−drain output, a 100 kΩ, pull−up resistor between P_{GOOD} and a stable active supply voltage rail is required.

The LDO has a constant over−current limit (OCL). Note that the OCL level reduces by one−half when the output voltage is not within the power good window. This reduction is non−latch protection. For V_{CC} under−voltage lockout (UVLO) protection, the NCP51403 monitors V_{CC} voltage. When the V_{CC} voltage is lower than the UVLO threshold voltage, both the V_{TT} and V_{RO} regulators are powered off. This shutdown is also non−latch protection.

Thermal Shutdown with Hysteresis

If the NCP51403 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP51403 provides on−chip thermal shutdown protection. When the chip junction temperature exceeds 150°C, the part will shutdown. When the junction temperature falls back to 125°C, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold then the V_{TT} and V_{RO} regulators are both shut off, discharged by the internal discharge MOSFETs. The shutdown is a non−latch protection.

Tracking Startup and Shutdown

The NCP51403 also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, V_{TT} follows V_{RO} once V_{RI} voltage is greater than 435 mV. V_{RI} follows the rise of V_{DDQ} memory supply rail via a voltage divider. P_{GOOD} is asserted 2 ms after V_{TT} is within ±20% of V_{RO}. During tracking shutdown, V_{TT} falls following V_{RO} until V_{RO} reaches 360 mV. Once V_{RO} falls below 360 mV, the internal discharge MOSFETs are turned on and quickly discharge both V_{RO} and V_{TT} to GND. P_{GOOD} is de−asserted once V_{TT} is beyond the ±20% range of V_{RO}.

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DDR3/DDR4 SELECTOR GUIDE

	VTT Startup	DDR Level	VTT Droop	VTT Capacitor
NCP51400	Soft Start	3 / 4	Yes	Cer/Poly
NCP51401	<35usec	3 / 4	Yes	Cer/Poly
NCP51402	<35usec	4	No*	Cer/Poly
NCP51403	<35usec	4	No*	Cer/PM=45°

* Recommended for New DDR4 Designs

VTT Startup Time

In order to speed up the time it takes a modern computer to Boot−up or Resume after Stand−by, some newer motherboard specs require VTT to rise from 0 V to 95% of VTT in less than 35 μsec. This new requirement is met in the new ON Semiconductor NCP51401, NCP51403 and NCP51403 devices.

VTT Droop

Droop is a technique to reduce error voltage due to a transient, or as a design tradeoff, to reduce system cost for a given transient magnitude, by using smaller, less expensive capacitors. Figure 3 shows the transient response in a system without droop and is showing a peak−to−peak error voltage of ±30 mV. Figure 4 shows the same magnitude of transient response, but this time the regulation is performed *with* droop. For example the magnitude of the transient in Figure 4 is +30 mV = +20 mV – (−10 mV) which is the same magnitude as in Figure 3, but since the output voltage is allowed to sag 10 mV when loaded (as opposed to the “perfect” Load Regulation, i.e. 0 mV of VTT output voltage sag as shown in Figure 3) then this same +30 mV transient starts at −10 mV and now only peaks to +20 mV. The net result is that with 10 mV of droop, the overall, peak−to−peak error voltage has been reduced from ±30 mV to ±20 mV.

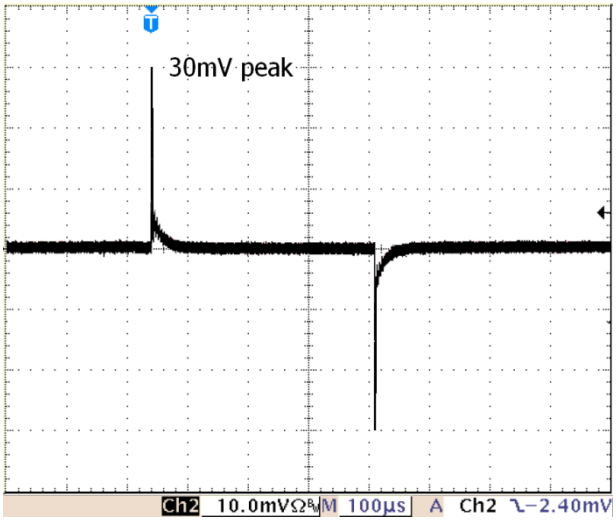

Figure 3.

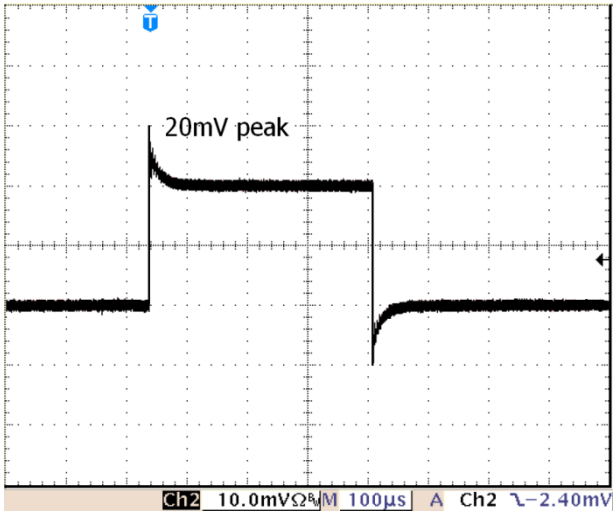

Figure 4.

Legacy DDR2/3, DDR4 and Droop

When the popular, now industry−standard, 51200−compatible devices were first introduced, the PC memory industry was transitioning from DDR2 (VTT = 900 mV) to DDR3 (VTT = 750 mV) and a value of ±14 mV of Droop per ±1.5 amps of DC current was designed−in. This value of Droop was appropriate for the DDR2 and DDR3 memory in use at the time, but this amount of Droop has now become excessive for DDR4. For example for DDR4 with a VTT voltage of 600 mV, the 5% error tolerance is ±30 mV, which leaves no transient−response margin for a DC load of ±2 amps. This excessive DDR2/3 Droop issue of using 51200 devices in newer DDR4 applications has been solved in the new ON Semiconductor NCP51403 and NCP51403 devices, which have no Droop for improved, high−current DDR4 transient response.

VTT Capacitor Selection

Many 51200−compatible devices have specified VTT capacitor ESR requirements and must be loaded with at least 20 μF of ceramic capacitance in order to guarantee stability. In contrast, the NCP51400, NCP51401 and NCP51403 were all designed to be stable with a wide range of ESR and can use both ceramic and higher−ESR, polymer capacitors.

Extending the NCP5140x family of parts, in applications that have specified phase margin requirements, we have introduced the NCP51403 which has >45° of phase margin when VTT is loaded with a ceramic capacitance of 20 μF. However just like our competitor’s 51200−compatible devices, the NCP51403 cannot be loaded solely with polymer capacitors because the 45° phase margin reduces the ESR−stability range of the VTT capacitor.

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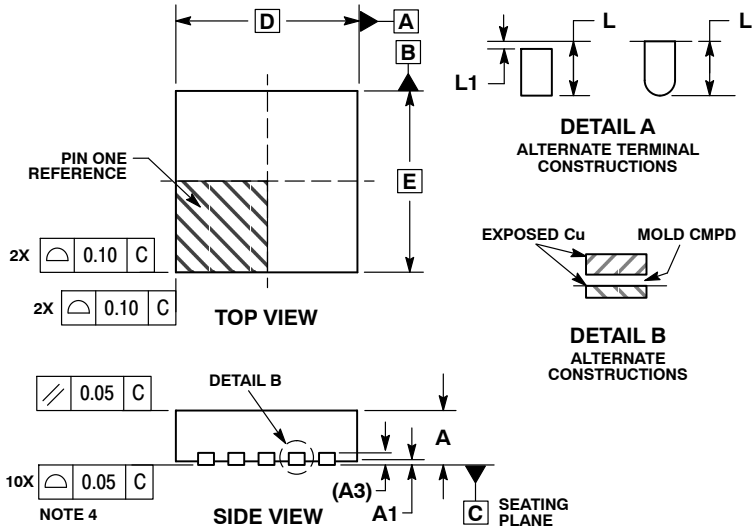
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

DFN10, 3x3, 0.5P
CASE 506CL
ISSUE O

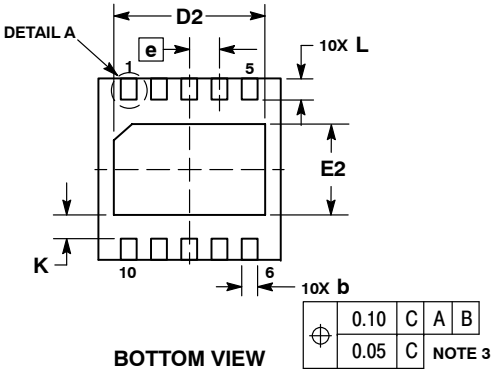
DATE 02 APR 2013

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.40	1.60
e	0.50 BSC	
K	0.25	---
L	0.25	0.45
L1	0.00	0.03

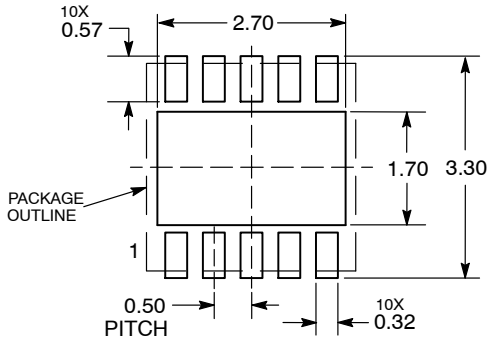


GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN10, 3X3, 0.5P	PAGE 1 OF 1

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