

# NYE08-10B6ST1G

## Protected Triac

### Silicon Bidirectional Thyristor

Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

#### Features

- Sensitive Gate Trigger Current in Two Quadrants
- Blocking Voltage to 600 V
- Surface Mount Package
- Compliant with IEC6100-4-5
- These are Pb-Free Devices

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (Sine Wave, 50 to 60 Hz, Gate Open, T <sub>J</sub> = 25 to 125°C)	V <sub>DRM</sub> , V <sub>RRM</sub>	600	V
On-State Current RMS (T <sub>C</sub> = 80°C) (Full Sine Wave 50 to 60 Hz)	I <sub>T(RMS)</sub>	0.8	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 25°C)	I <sub>TSM</sub>	8.0	A
Circuit Fusing Considerations (Pulse Width = 8.3 ms)	I <sup>2</sup> t	0.4	A <sup>2</sup> s
Peak Gate Power (T <sub>C</sub> = 80°C, Pulse Width ≤ 1.0 μs)	P <sub>GM</sub>	5.0	W
Average Gate Power (T <sub>C</sub> = 80°C, t = 8.3 ms)	P <sub>G(AV)</sub>	0.1	W
Non-Repetitive Line Peak Voltage (IEC6100-4-5)	V <sub>PP</sub>	2.0	kV
Critical Rate of Rise of All-State Current (I <sub>G</sub> = 2 × I <sub>GT</sub> , t <sub>r</sub> < 100 μs, T <sub>J</sub> = 125°C)	di/dt	100	A/μs
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

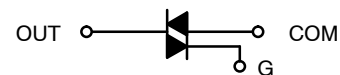
1. V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



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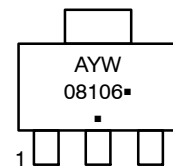
**PROTECTED TRIAC  
0.8 AMPERE RMS  
600 VOLTS**



#### MARKING DIAGRAM



**SOT-223  
CASE 318E**



A = Assembly Location  
Y = Year  
W = Work Week  
08106 = Device Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT

Pin	Assignment
1	OUT
2	COM
3	Gate
4	COM

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NYE08-10B6ST1G	SOT-223 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NYE08-10B6ST1G

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	50	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	160	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	$T_L$	260	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Peak Repetitive Blocking Current ( $V_D = V_{DRM}/V_{RRM}$ ; Gate Open)	$T_J = 25^{\circ}C$	$I_{DRM}, I_{RRM}$	-	-	2.0	$\mu A$
	$T_J = +125^{\circ}C$		-	-	200	$\mu A$

### ON CHARACTERISTICS

Peak On-State Voltage ( $I_{TM} = \pm 1.1$ A Peak; Pulse Width $\leq 2.0$ ms, Duty Cycle $\leq 2.0\%$ )	$V_{TM}$	-	-	1.3	V
Gate Trigger Current (dc) ( $V_D = 12$ Vdc, $R_L = 30 \Omega$ ) OUT(+), G(-) OUT(-), G(-)	$I_{GT}$	0.15	-	10	mA
		0.15	-	10	
Latching Current ( $V_D = 12$ V, $I_G = 1.2 \times I_{GT}$ ) OUT(+), G(-) All Types OUT(-), G(-) All Types	$I_L$	-	-	30	mA
		-	-	30	
Gate Trigger Voltage (dc) ( $V_D = 12$ Vdc, $R_L = 30 \Omega$ )	$V_{GT}$	-	-	1.0	V
Gate Non-Trigger Voltage ( $V_D = 12$ V, $R_L = 30 \Omega$ , $T_J = 125^{\circ}C$ ) Quadrants 2, 3	$V_{GD}$	0.15	-	-	V
Dynamic Resistance	$R_D$	-	-	300	m $\Omega$
Holding Current ( $V_D = 12$ Vdc, Initiating Current = 50 mA, Gate Open)	$I_H$	-	-	25	mA

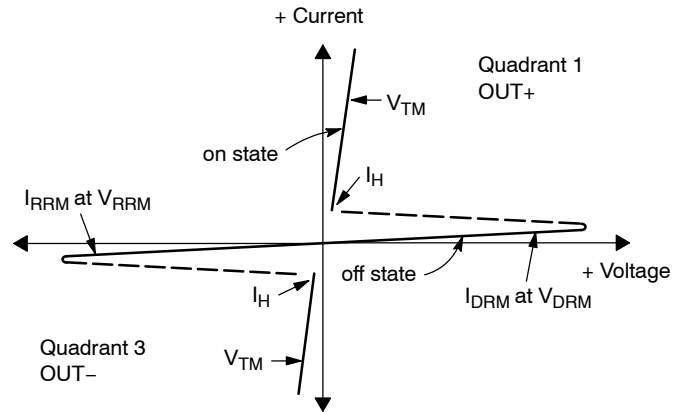
### DYNAMIC CHARACTERISTICS

Rate of Change of Commutating Current (Commutating $dv/dt = 15$ V/ $\mu s$ , Gate Open, $T_J = 125^{\circ}C$ , $f = 250$ Hz, without Snubber)	$di/dt(c)$	0.3	-	-	A/ms
Critical Rate of Rise of Off-State Voltage ( $V_D = 67\% V_{DRM}$ , Exponential Waveform, Gate Open, $T_J = 125^{\circ}C$ )	$dv/dt$	500	-	-	V/ $\mu s$
Clamping Voltage ( $I_{CL} = 1.0$ mA, $t_p = 1$ ms, $T_J = 125^{\circ}C$ )	$V_{CL}$	650	-	-	V

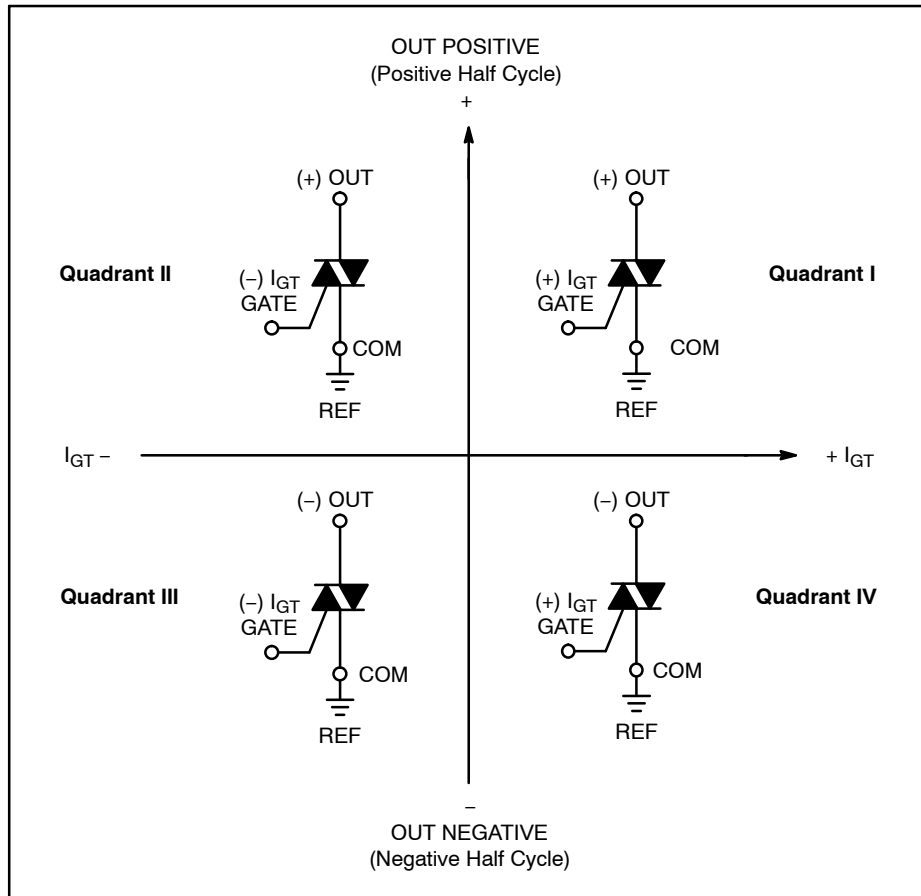
# NYE08-10B6ST1G

## Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Forward Off State Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Reverse Off State Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Maximum On State Voltage
$I_H$	Holding Current

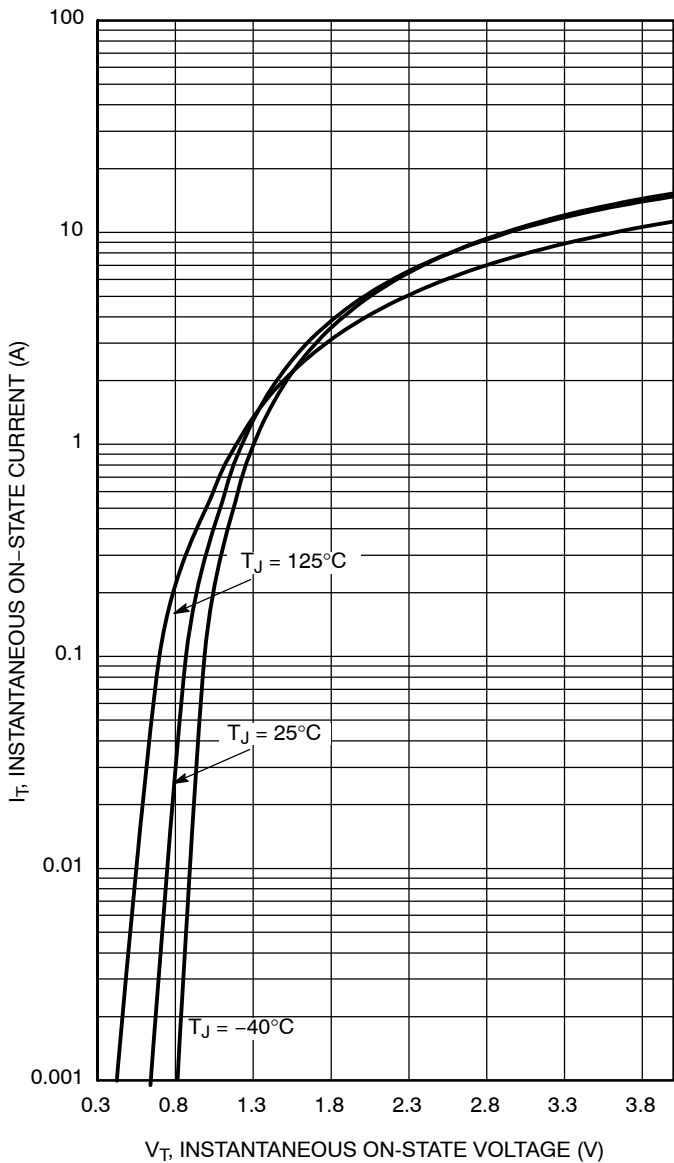


### Quadrant Definitions for a Triac

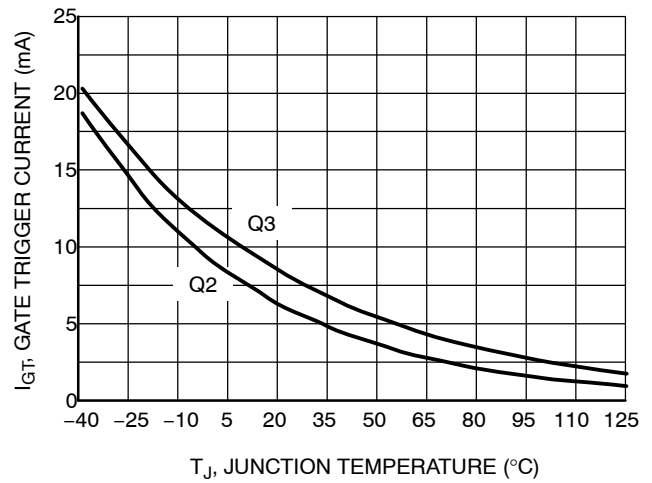


All polarities are referenced to COM.

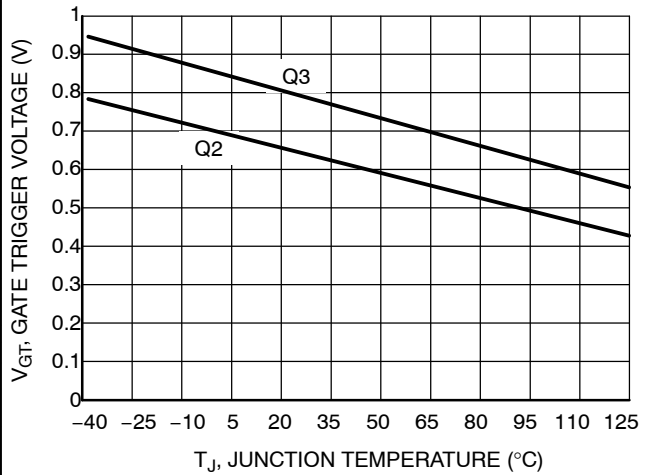
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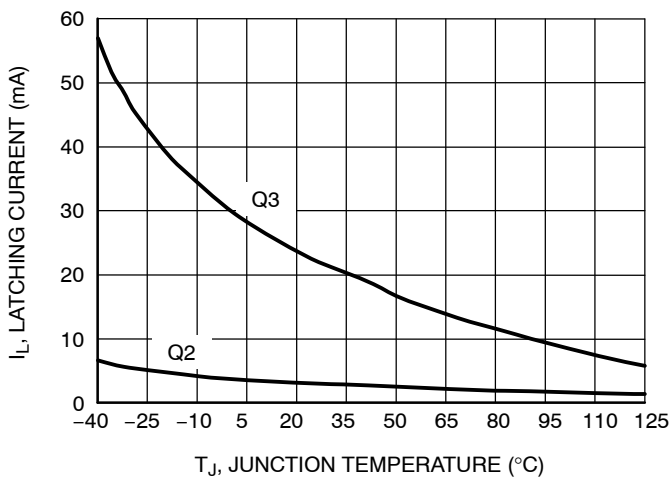
**Figure 1. Maximum On-State Voltage Characteristics**



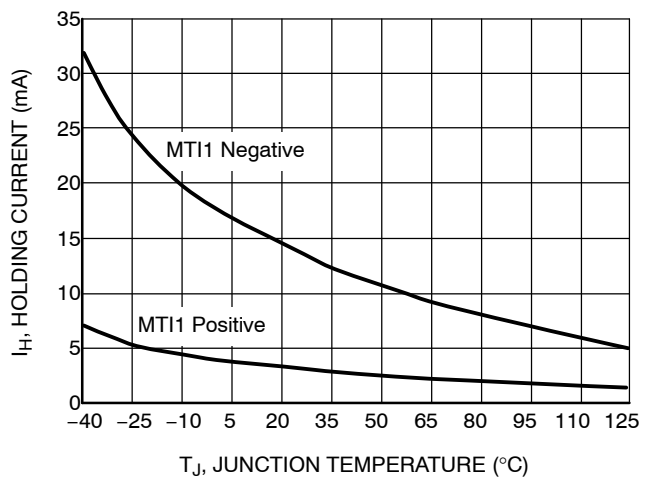
**Figure 2. Typical Gate Trigger Current**



**Figure 3. Typical Gate Trigger Voltage**

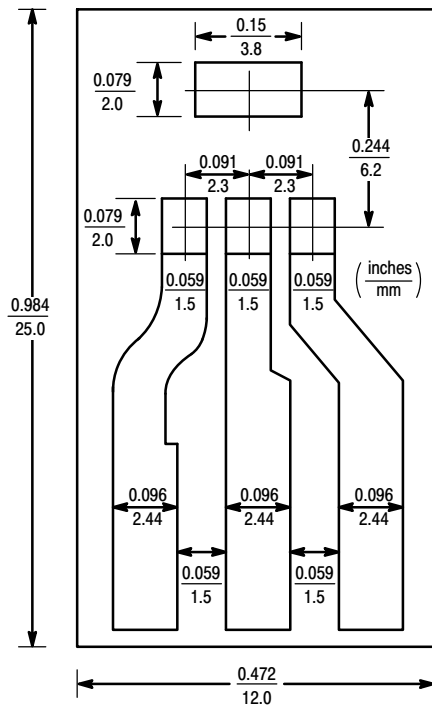


**Figure 4. Typical Latching Current**



**Figure 5. Typical Holding Current**

# NYE08-10B6ST1G



BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.  
 BOARD THICKNESS = 65 MIL, FOIL THICKNESS = 2.5 MIL  
 MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

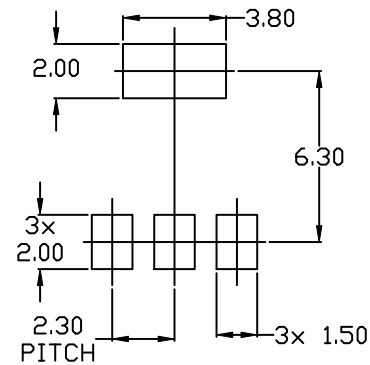
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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<b>DESCRIPTION:</b>	<b>SOT-223 (TO-261)</b>	<b>PAGE 1 OF 2</b>

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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |                                                                              |                                                                             |                                                                               |                                                                       |                                                                       |
|------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED                                                  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |                                                                       |                                                                       |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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