Ordering number : ENA2124

LC79431KNE

ON Semiconductor®

http://onsemi.com

CMOS LSI

Dot-Matrix LCD Drivers

Overview

The LC79431KNE is a large-scale dot matrix LCD common driver LSI. The LC79431KNE contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79431KNE can be used in conjunction with segment driver LC79401KNE (QIP100E) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support a further increases in bit number
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include
  V_{DD} (Logic section) : 2.7 to 5.5V/-20 to +85°C
  V_{DD}-V_{EE} (LCD section) : 12 to 32V/-20 to +85°C
- CMOS process
- 100-pin flat plastic package (QIP100E)

July, 2013

91912HKPC 20080310-S00005 No. A2124-1/7

Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (Logic)	V_{DD} max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max	*1	0 to 35	V
Maximum input voltage	V_I max		-0.3 to V_{DD}+0.3	V
Storage temperature	Tstg		-40 to +125	°C

Note *1 The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, V_{DD}-V2≤7V, V5-V_{EE}≤7V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = -20 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (Logic)	V_{DD}		2.7		5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, 3	12		32	V
Input high level voltage	V_{IH}	DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISPOFF}}$	0.8V_{DD}			V
Input low level voltage	V_{IL}	DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISPOFF}}$			0.2V_{DD}	V
CP Shift clock	f_{CP}	CP			1	MHz
CP pulse width	t_{WC}	CP	63			ns
Setup time	t_{SETUP}	DIO1 → CP, DIO80 → CP	100			ns
Hold time	t_{HOLD}	DIO1 → CP, DIO80 → CP	100			ns
CP rise time	t_R	CP			50	ns
CP fall time	t_F	CP			50	ns

Note *2 The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, V_{DD}-V2≤7V, V5-V_{EE}≤7V

*3 When the power supply is turned on, power to the LCD driver is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

Electrical Characteristics at Ta = 25±2°C, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	I_{IH}	V_{IN}=V_{DD}, V_{DD}=5.5V, DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISPOFF}}$			1	μA
Input low level current	I_{IL}	V_{IN}=V_{SS}, V_{DD}=5.5V, DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISPOFF}}$	-1			μA
Output high level voltage	V_{OH}	I_{OH}=-0.4mA, DIO1, DIO80	V_{DD}-0.4			V
Output low level voltage	V_{OL}	I_{OL}=0.4mA, DIO1, DIO80			0.4	V
Driver on resistance	R_{ON}(1)	V_{DD}-V_{EE}=30V, $\lvert V_{DE}$-$V_O \rvert$=0.5V V_{DD}=4.5V, O1 to O80 *4			1.0	kΩ
	R_{ON}(2)	V_{DD}-V_{EE}=20V, $\lvert V_{DE}$-$V_O \rvert$=0.5V V_{DD}=4.5V, O1 to O80 *4			1.0	kΩ
Consumable current drain (1)	I_{SS}	V_{DD}-V_{EE}=30V, CP=14kHz no-load, V_{DD}=5.5V ; V_{SS}			100	μA
Consumable current drain (2)	I_{EE}	V_{DD}-V_{EE}=30V, CP=14kHz no-load, V_{DD}=5.5V ; V_{EE}			100	μA
Input capacitance	CI	f=1MHz ; CP		6		pF

Note *4 V_{DE} = V1 or V2 or V5 or V_{EE}, V1 = V_{DD}, V2 = 16/17 (V_{DD}-V_{EE}), V5 = 1/17 (V_{DD}-V_{EE})

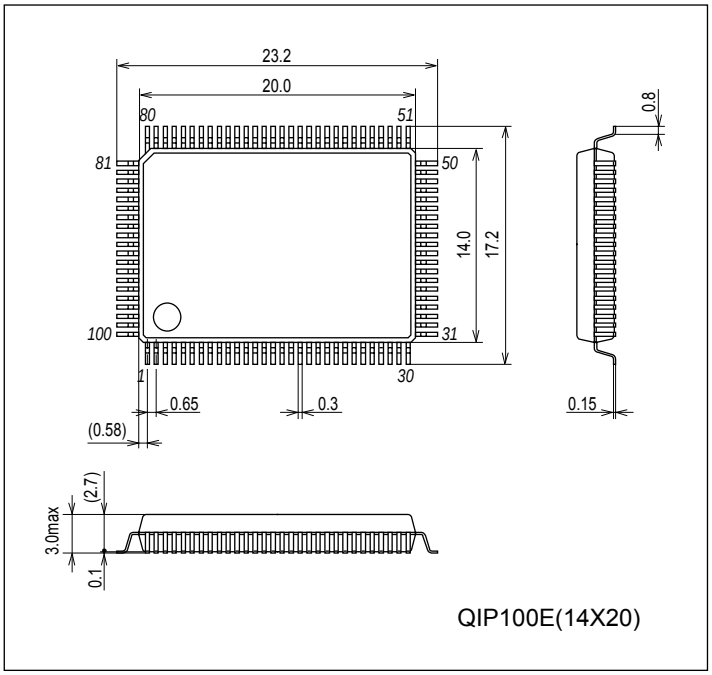
Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Output delay time	t_{PLH}	CL=15pF ; CP → DIO1, CP → DIO80			250	ns
	t_{PHL}	CL=15pF ; CP → DIO1, CP → DIO80			250	ns

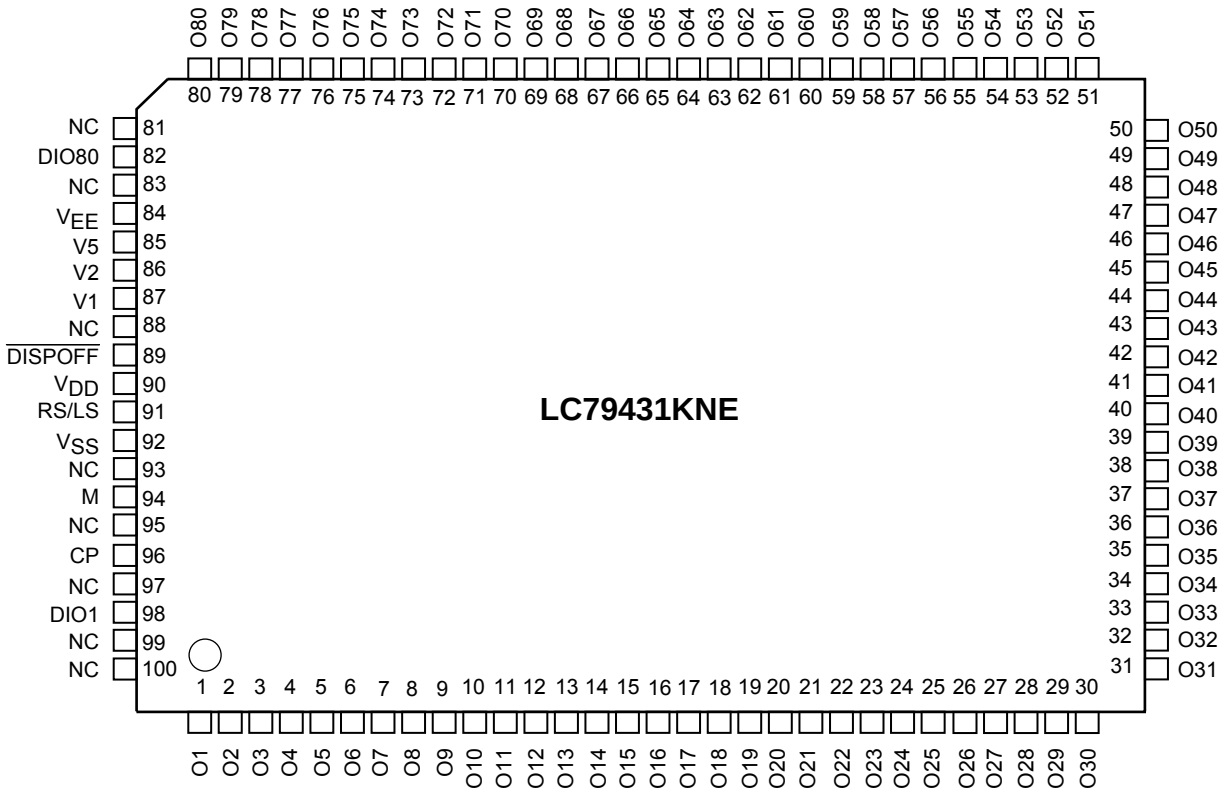
Package Dimensions

unit:mm (typ)

3151A

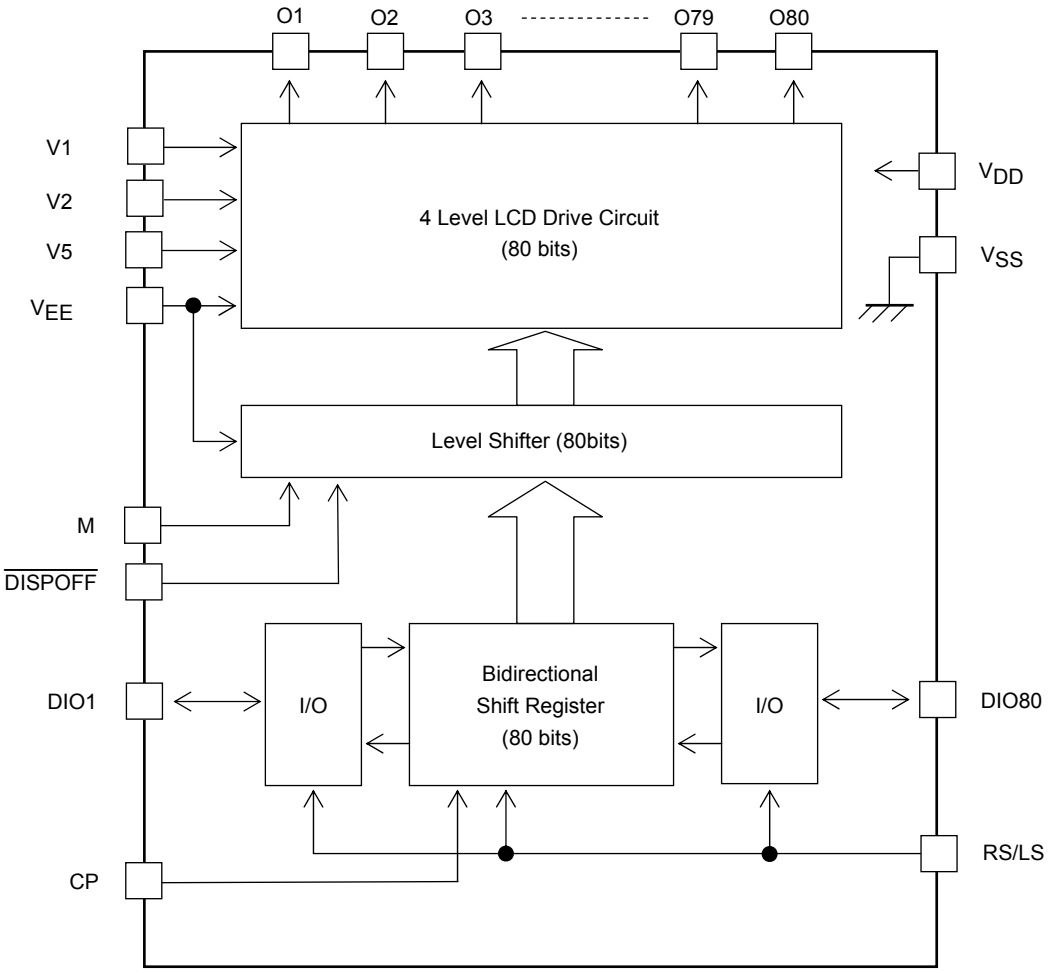


Pin Assignment



Top view

Equivalent Circuit Block Diagram



Pin Function

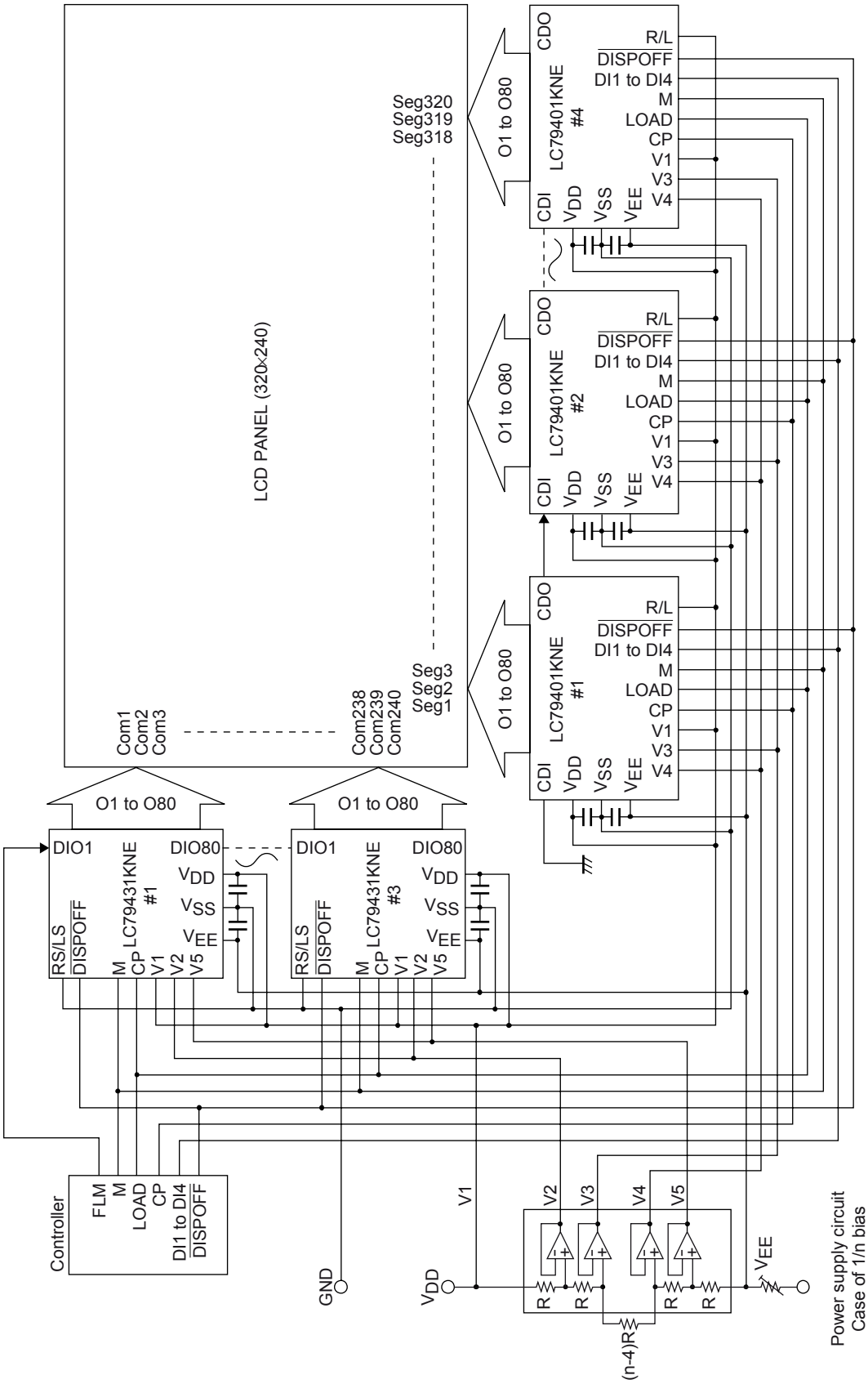
<table>
<tr><th>Pin No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>90
92
84</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Supply</td><td>V_{DD}-V_{SS} : Logic power supply
V_{DD}-V_{EE} : LCD drive circuit power supply</td></tr>
<tr><td>87
86
85</td><td>V1
V2
V5</td><td>Supply</td><td>LCD drive level power supply
V1, V_{EE} : Selected level
V2, V5 : Unselected level</td></tr>
<tr><td>96</td><td>CP</td><td>I</td><td>Bidirectional shift register shift clock (falling edge trigger)</td></tr>
<tr><td>98
82

91</td><td>DIO1
DIO80

RS/LS</td><td>I/O
I/O

I</td><td>
<table>
<tr><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th></tr>
<tr><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td></tr>
<tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td></tr>
</table>
</td></tr>
<tr><td>94</td><td>M</td><td>I</td><td>LCD drive output alternation signal</td></tr>
<tr><td>89</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>O1 to O80 output controlling input pins.</td></tr>
<tr><td>1
⋮
80</td><td>O1
⋮
O80</td><td>O</td><td>LCD drive outputs
The output levels are determined by the combination of the output the data,
The M signal, and the $\overline{\text{DISPOFF}}$ pin as shown in the table.
<table>
<tr><th>M</th><th>Data</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don’t care (May be set to either “H” or “L”)</td></tr>
<tr><td>81
83
88
93
95
97
99
100</td><td>NC</td><td>-</td><td>Must be left open.</td></tr>
</table>

Application Example (LC79401KNE/LC79431KNE)



Switching Characteristics Diagram