

# CAT25640

## 64-Kb SPI Serial CMOS EEPROM

### Description

The CAT25640 is a 64-Kb Serial CMOS EEPROM device internally organized as 8Kx8 bits. This features a 64-byte page write buffer and supports the Serial Peripheral Interface (SPI) protocol. The device is enabled through a Chip Select ( $\overline{CS}$ ) input. In addition, the required bus signals are clock input (SCK), data input (SI) and data output (SO) lines. The  $\overline{HOLD}$  input may be used to pause any serial communication with the CAT25640 device. The device features software and hardware write protection, including partial as well as full array protection.

### Features

- 10 MHz SPI Compatible
- 1.8 V to 5.5 V Supply Voltage Range
- SPI Modes (0,0) & (1,1)
- 64-byte Page Write Buffer
- Self-timed Write Cycle
- Hardware and Software Protection
- Block Write Protection
  - Protect  $1/4$ ,  $1/2$  or Entire EEPROM Array
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- PDIP, SOIC, TSSOP 8-lead, TDFN and UDFN 8-pad Packages
- This Device is Pb-Free, Halogen Free/BFR Free, and RoHS Compliant

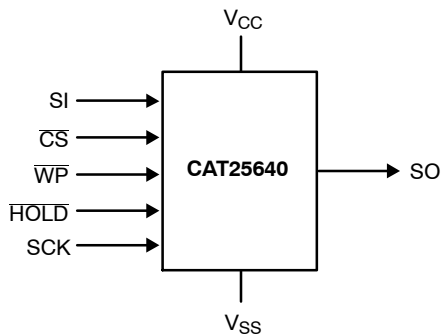


Figure 1. Functional Symbol



ON Semiconductor®

<http://onsemi.com>



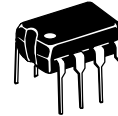
SOIC-8  
V SUFFIX  
CASE 751BD



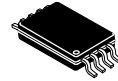
UDFN-8  
HU3 SUFFIX  
CASE 517AX



TDFN-8  
VP2 SUFFIX  
CASE 511AK

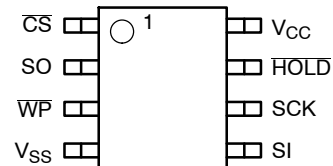


PDIP-8  
L SUFFIX  
CASE 646AA



TSSOP-8  
Y SUFFIX  
CASE 948AL

### PIN CONFIGURATION



PDIP (L), SOIC (V), TSSOP (Y),  
TDFN (VP2), UDFN (HU3)

### PIN FUNCTION

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock
$\overline{HOLD}$	Hold Transmission Input
VCC	Power Supply

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

# CAT25640

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Operating Temperature	-45 to +130	°C
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- The DC input voltage on any pin should not be lower than -0.5 V or higher than  $V_{CC} + 0.5$  V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than  $V_{CC} + 1.5$  V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS (Note 2)**

Symbol	Parameter	Min	Units
$N_{END}$ (Note 3)	Endurance	1,000,000	Program / Erase Cycles
$T_{DR}$	Data Retention	100	Years

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- Page Mode,  $V_{CC} = 5$  V, 25°C.

**Table 3. D.C. OPERATING CHARACTERISTICS**

( $V_{CC} = 1.8$  V to 5.5 V,  $T_A = -40$ °C to +85°C and  $V_{CC} = 2.5$  V to 5.5 V,  $T_A = -40$ °C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units	
$I_{CCR}$	Supply Current (Read Mode)	Read, $V_{CC} = 5.5$ V, SO open	10 MHz / -40°C to 85°C	2	mA	
			5 MHz / -40°C to 125°C	2		
$I_{CCW}$	Supply Current (Write Mode)	Write, $V_{CC} = 5.5$ V, SO open	10 MHz / -40°C to 85°C	3	mA	
			5 MHz / -40°C to 125°C	3		
$I_{SB1}$	Standby Current	$V_{IN} = GND$ or $V_{CC}$ , $\overline{CS} = V_{CC}$ , $\overline{WP} = V_{CC}$ , $V_{CC} = 5.5$ V	$T_A = -40$ °C to +85°C	1	μA	
			$T_A = -40$ °C to +125°C	2		
$I_{SB2}$	Standby Current	$V_{IN} = GND$ or $V_{CC}$ , $\overline{CS} = V_{CC}$ , $\overline{WP} = GND$ , $V_{CC} = 5.5$ V	$T_A = -40$ °C to +85°C	3	μA	
			$T_A = -40$ °C to +125°C	5		
$I_L$	Input Leakage Current	$V_{IN} = GND$ or $V_{CC}$	-2	2	μA	
$I_{LO}$	Output Leakage Current	$\overline{CS} = V_{CC}$ , $V_{OUT} = GND$ or $V_{CC}$	$T_A = -40$ °C to +85°C	-1	1	μA
			$T_A = -40$ °C to +125°C	-1	2	μA
$V_{IL}$	Input Low Voltage		-0.5	$0.3 V_{CC}$	V	
$V_{IH}$	Input High Voltage		$0.7 V_{CC}$	$V_{CC} + 0.5$	V	
$V_{OL1}$	Output Low Voltage	$V_{CC} \geq 2.5$ V, $I_{OL} = 3.0$ mA		0.4	V	
$V_{OH1}$	Output High Voltage	$V_{CC} \geq 2.5$ V, $I_{OH} = -1.6$ mA	$V_{CC} - 0.8$ V		V	
$V_{OL2}$	Output Low Voltage	$V_{CC} < 2.5$ V, $I_{OL} = 150$ μA		0.2	V	
$V_{OH2}$	Output High Voltage	$V_{CC} < 2.5$ V, $I_{OH} = -100$ μA	$V_{CC} - 0.2$ V		V	

**Table 4. PIN CAPACITANCE (Note 2)**

( $T_A = 25$ °C,  $f = 1.0$  MHz,  $V_{CC} = +5.0$  V)

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{OUT}$	Output Capacitance (SO)	$V_{OUT} = 0$ V			8	pF
$C_{IN}$	Input Capacitance (CS, SCK, SI, WP, HOLD)	$V_{IN} = 0$ V			8	pF

# CAT25640

**Table 5. A.C. CHARACTERISTICS** (Notes 4, 7)

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial) and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (Extended).)

Symbol	Parameter	$V_{CC} = 1.8\text{ V} - 5.5\text{ V} / -40^\circ\text{C}$ to $+85^\circ\text{C}$		$V_{CC} = 2.5\text{ V} - 5.5\text{ V}$		Units
		$V_{CC} = 2.5\text{ V} - 5.5\text{ V} / -40^\circ\text{C}$ to $+125^\circ\text{C}$		$-40^\circ\text{C}$ to $+85^\circ\text{C}$		
		Min	Max	Min	Max	
$f_{\text{SCK}}$	Clock Frequency	DC	5	DC	10	MHz
$t_{\text{SU}}$	Data Setup Time	40		20		ns
$t_{\text{H}}$	Data Hold Time	40		20		ns
$t_{\text{WH}}$	SCK High Time	75		40		ns
$t_{\text{WL}}$	SCK Low Time	75		40		ns
$t_{\text{LZ}}$	HOLD to Output Low Z		50		25	ns
$t_{\text{RI}}$ (Note 5)	Input Rise Time		2		2	$\mu\text{s}$
$t_{\text{FI}}$ (Note 5)	Input Fall Time		2		2	$\mu\text{s}$
$t_{\text{HD}}$	HOLD Setup Time	0		0		ns
$t_{\text{CD}}$	HOLD Hold Time	10		10		ns
$t_{\text{V}}$	Output Valid from Clock Low		75		40	ns
$t_{\text{HO}}$	Output Hold Time	0		0		ns
$t_{\text{DIS}}$	Output Disable Time		50		20	ns
$t_{\text{HZ}}$	HOLD to Output High Z		100		25	ns
$t_{\text{CS}}$	$\overline{\text{CS}}$ High Time	50		20		ns
$t_{\text{CSS}}$	$\overline{\text{CS}}$ Setup Time	20		15		ns
$t_{\text{CSH}}$ (Note 7)	$\overline{\text{CS}}$ Hold Time	30		20		ns
$t_{\text{CNS}}$	$\overline{\text{CS}}$ Interactive Setup Time	20		15		ns
$t_{\text{CNH}}$	$\overline{\text{CS}}$ Interactive Hold Time	20		15		ns
$t_{\text{WPS}}$	$\overline{\text{WP}}$ Setup Time	10		10		ns
$t_{\text{WPH}}$	$\overline{\text{WP}}$ Hold Time	100		60		ns
$t_{\text{WC}}$ (Note 6)	Write Cycle Time		5		5	ms

4. AC Test Conditions:

Input Pulse Voltages:  $0.3 V_{CC}$  to  $0.7 V_{CC}$

Input rise and fall times:  $\leq 10\text{ ns}$

Input and output reference voltages:  $0.5 V_{CC}$

Output load: current source  $I_{OL\text{ max}}/I_{OH\text{ max}}$ ;  $C_L = 50\text{ pF}$

5. This parameter is tested initially and after a design or process change that affects the parameter.

6.  $t_{\text{WC}}$  is the time from the rising edge of  $\overline{\text{CS}}$  after a valid write sequence to the end of the internal write cycle.

7. **All Chip Select (CS) timing parameters are defined relative to the positive clock edge (Figure 2).  $t_{\text{CSH}}$  timing specification is valid for die revision E and higher. The die revision E is identified by letter "E" or a dedicated marking code on top of the package. For previous product revision (Rev. D) the  $t_{\text{CSH}}$  is defined relative to the negative clock edge (please refer to data sheet [Doc. No. MD-1128 Rev. D](#)).**

**Table 6. POWER-UP TIMING** (Notes 5, 8)

Symbol	Parameter	Max	Units
$t_{\text{PUR}}$	Power-up to Read Operation	1	ms
$t_{\text{PUW}}$	Power-up to Write Operation	1	ms

8.  $t_{\text{PUR}}$  and  $t_{\text{PUW}}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.

# CAT25640

## Pin Description

**SI:** The serial data input pin accepts op-codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

**SO:** The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

**SCK:** The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT25640.

**$\overline{CS}$ :** The chip select input pin is used to enable/disable the CAT25640. When  $\overline{CS}$  is high, the SO output is tri-stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). *Every communication session between host and CAT25640 must be preceded by a high to low transition and concluded with a low to high transition of the  $\overline{CS}$  input.*

**$\overline{WP}$ :** The write protect input pin will allow all write operations to the device when held high. When  $\overline{WP}$  pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to "1", writing to the Status Register is disabled.

**HOLD:** The HOLD input pin is used to pause transmission between host and CAT25640, without having to retransmit the entire sequence at a later time. To pause, HOLD must be taken low and to resume it must be taken back high, with the SCK input low during both transitions. When not used for pausing, the HOLD input should be tied to  $V_{CC}$ , either directly or through a resistor.

## Functional Description

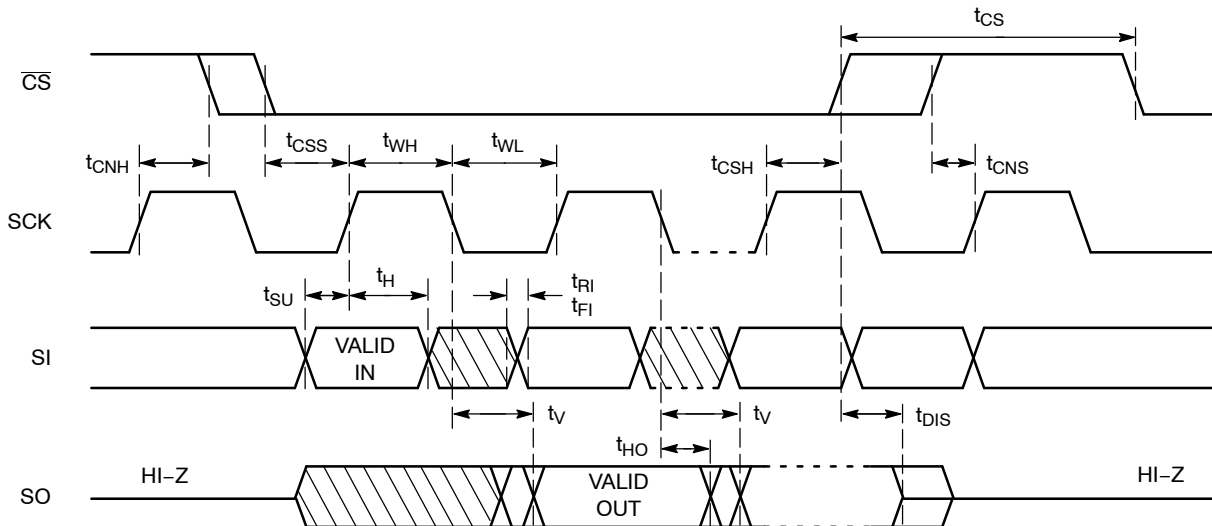
The CAT25640 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 7.

Reading data stored in the CAT25640 is accomplished by simply providing the READ command and an address. Writing to the CAT25640, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the  $\overline{CS}$  input pin, the CAT25640 will accept any one of the six instruction op-codes listed in Table 7 and will ignore all other possible 8-bit combinations. The communication protocol follows the timing from Figure 2.

**Table 7. INSTRUCTION SET**

Instruction	Op-code	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory



**Figure 2. Synchronous Data Timing**

**Status Register**

The Status Register, as shown in Table 8, contains a number of status and control bits.

The  $\overline{\text{RDY}}$  (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non-volatile. The user is

allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read-only.

The WPEN (Write Protect Enable) bit acts as an enable for the  $\overline{\text{WP}}$  pin. Hardware write protection is enabled when the  $\overline{\text{WP}}$  pin is low and the WPEN bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the  $\overline{\text{WP}}$  pin is high or the WPEN bit is 0. The WPEN bit,  $\overline{\text{WP}}$  pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 10.

**Table 8. STATUS REGISTER**

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	$\overline{\text{RDY}}$

**Table 9. BLOCK PROTECTION BITS**

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	1800-1FFF	Quarter Array Protection
1	0	1000-1FFF	Half Array Protection
1	1	0000-1FFF	Full Array Protection

**Table 10. WRITE PROTECT CONDITIONS**

WPEN	$\overline{\text{WP}}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

# CAT25640

## WRITE OPERATIONS

The CAT25640 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

### Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the CAT25640. Care must be taken to take the  $\overline{CS}$  input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 3. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 4. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

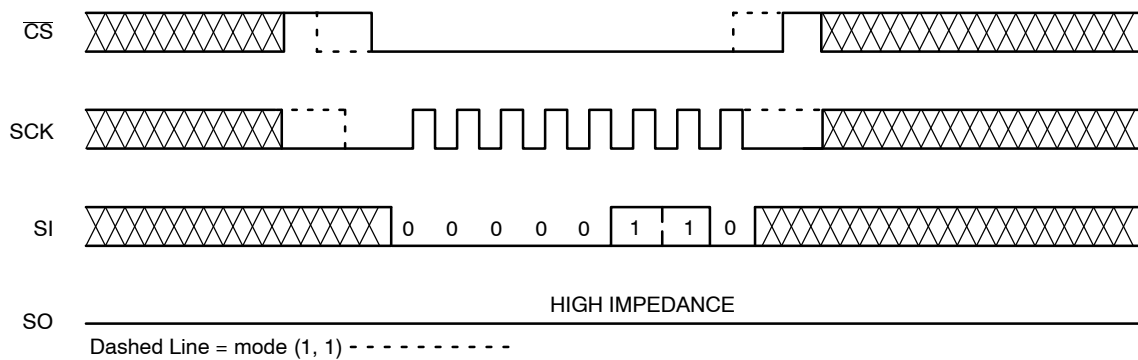


Figure 3. WREN Timing

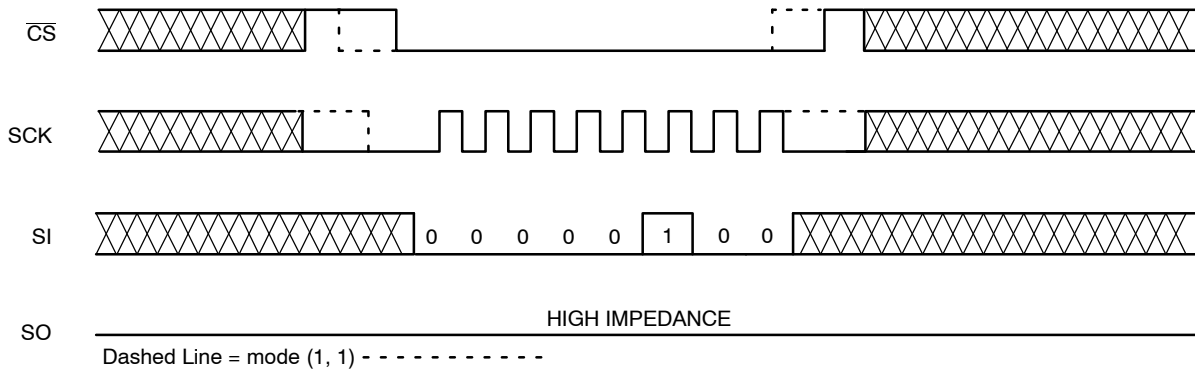


Figure 4. WRDI Timing

# CAT25640

## Byte Write

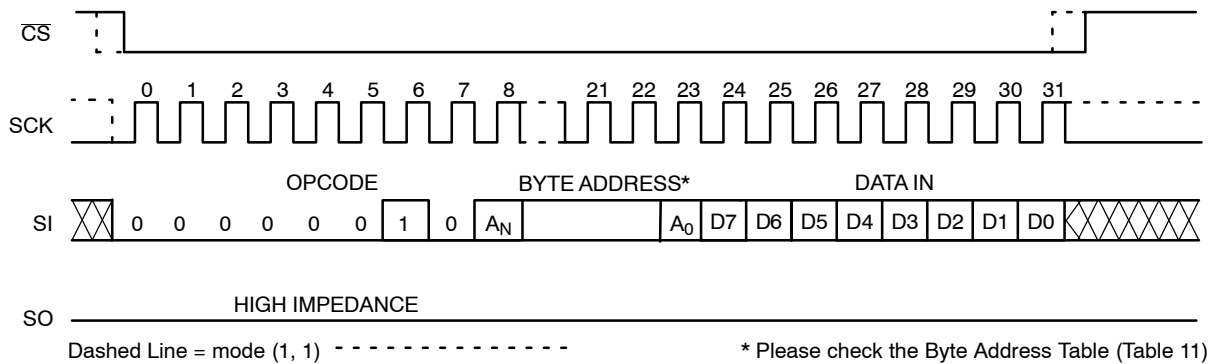
Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16-bit address and data as shown in Figure 5. Only 13 significant address bits are used by the CAT25640. The rest are don't care bits, as shown in Table 11. Internal programming will start after the low to high  $\overline{CS}$  transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The  $\overline{RDY}$  bit will indicate if the internal write cycle is in progress ( $\overline{RDY}$  high), or the device is ready to accept commands ( $\overline{RDY}$  low).

## Page Write

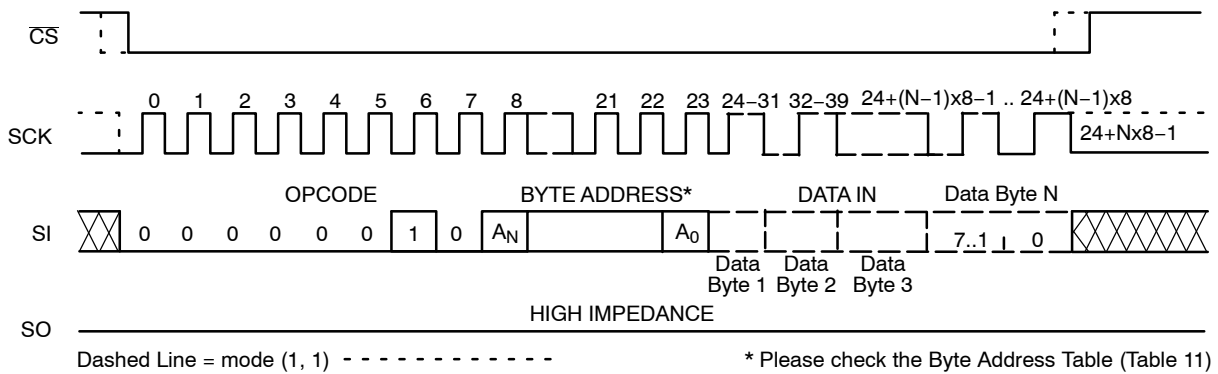
After sending the first data byte to the CAT25640, the host may continue sending data, up to a total of 64 bytes, according to timing shown in Figure 6. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the CAT25640 is automatically returned to the write disable state.

**Table 11. BYTE ADDRESS**

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulses
CAT25640	A12 – A0	A15 – A13	16



**Figure 5. Byte WRITE Timing**



**Figure 6. Page WRITE Timing**

# CAT25640

## Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 7. Only bits 2, 3 and 7 can be written using the WRSR command.

## Write Protection

The Write Protect ( $\overline{WP}$ ) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When  $\overline{WP}$  is low and the WPEN bit is set to "1", write operations to the Status Register are inhibited.  $\overline{WP}$  going low while  $\overline{CS}$  is still low will interrupt a write to the status register. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no effect on any write operation to the Status Register. The  $\overline{WP}$  pin function is blocked when the WPEN bit is set to "0". The  $\overline{WP}$  input timing is shown in Figure 8.

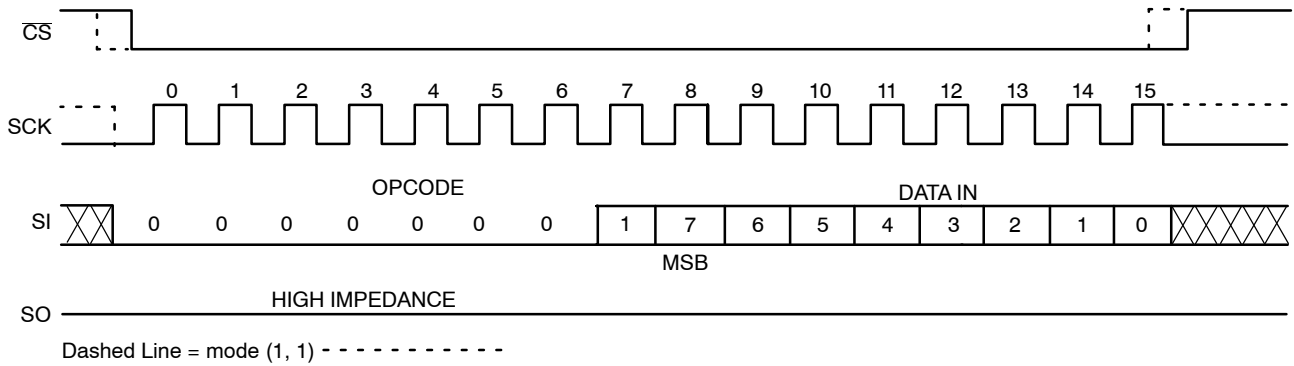


Figure 7. WRSR Timing

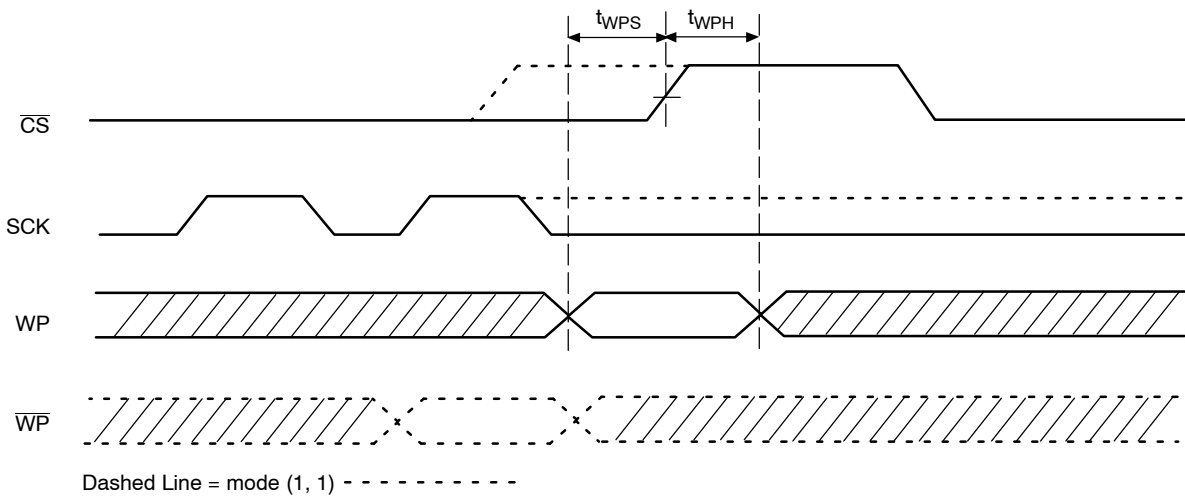


Figure 8.  $\overline{WP}$  Timing



# CAT25640

## READ OPERATIONS

### Read from Memory Array

To read from memory, the host sends a READ instruction followed by a 16-bit address (see Table 11 for the number of significant address bits).

After receiving the last address bit, the CAT25640 will respond by shifting out data on the SO pin (as shown in Figure 9). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory

address, and the read cycle can be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high.

### Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT25640 will shift out the contents of the status register on the SO pin (Figure 10). The status register may be read at any time, including during an internal write cycle. While the internal write cycle is in progress, the RDSR command will output the  $\overline{RDY}$  (Ready) bit status only (i.e. data out = FFh).

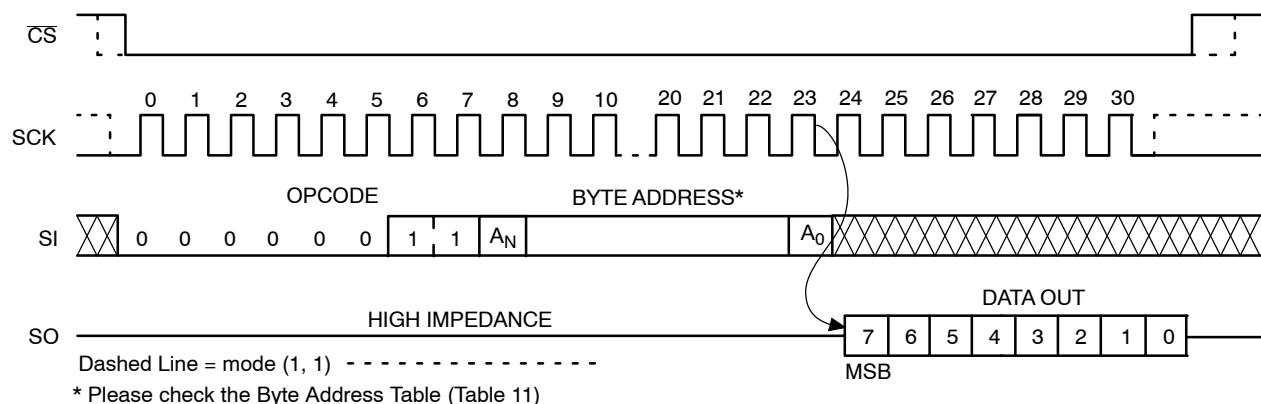


Figure 9. READ Timing

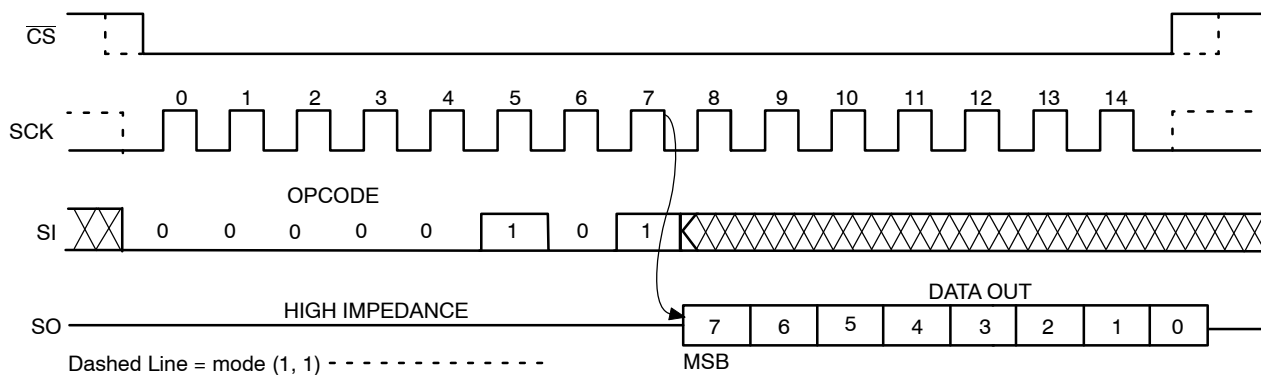


Figure 10. RDSR Timing

**Hold Operation**

The  $\overline{\text{HOLD}}$  input can be used to pause communication between host and CAT25640. To pause,  $\overline{\text{HOLD}}$  must be taken low while SCK is low (Figure 11). During the hold condition the device must remain selected ( $\overline{\text{CS}}$  low). During the pause, the data output pin (SO) is tri-stated (high impedance) and SI transitions are ignored. To resume communication,  $\overline{\text{HOLD}}$  must be taken high while SCK is low.

**Design Considerations**

The CAT25640 device incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after  $V_{CC}$  exceeds the POR trigger level and will power down into Reset mode when  $V_{CC}$  drops

below the POR trigger level. This bi-directional POR behavior protects the device against ‘brown-out’ failure following a temporary loss of power.

The CAT25640 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the  $\overline{\text{CS}}$  pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The  $\overline{\text{CS}}$  input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op-code will be ignored and the serial output pin (SO) will remain in the high impedance state.

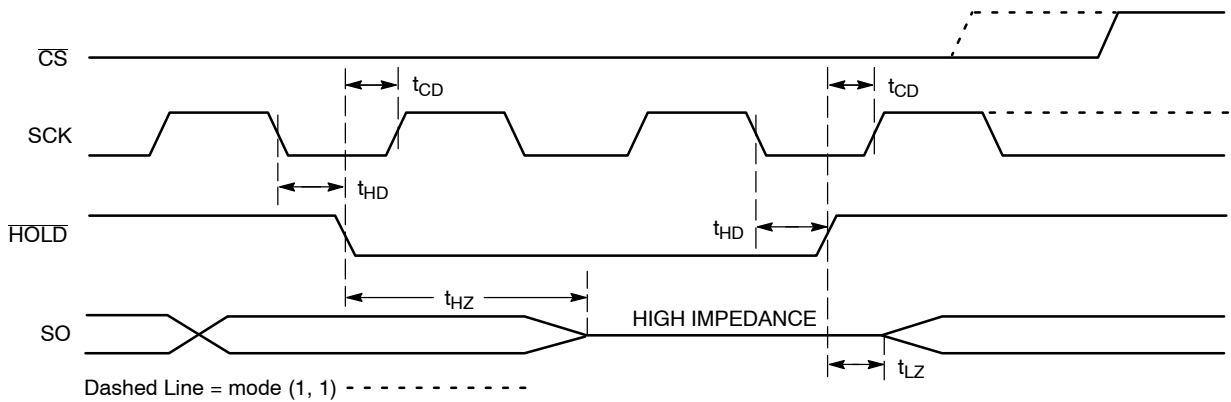


Figure 11.  $\overline{\text{HOLD}}$  Timing

# CAT25640

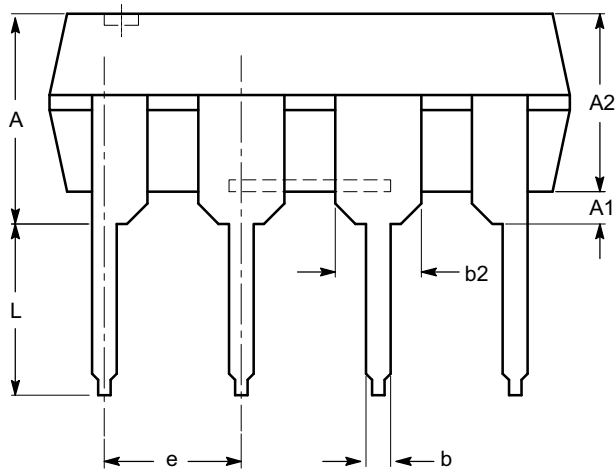
## PACKAGE DIMENSIONS

PDIP-8, 300 mils  
CASE 646AA-01  
ISSUE A

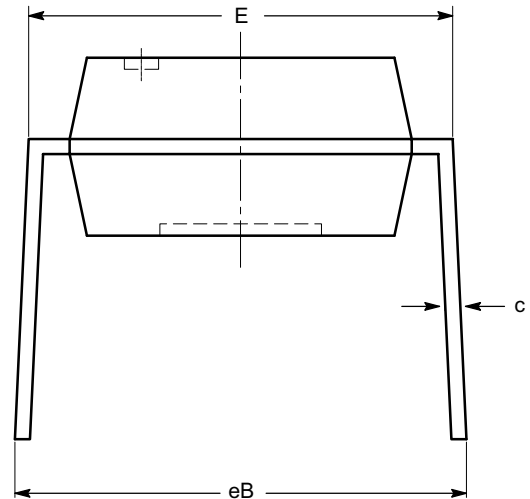


SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80

TOP VIEW



SIDE VIEW



END VIEW

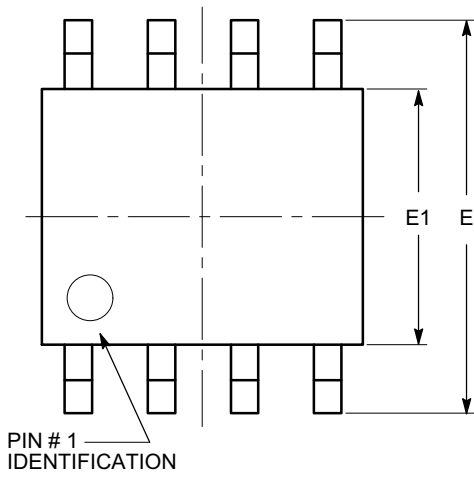
**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

# CAT25640

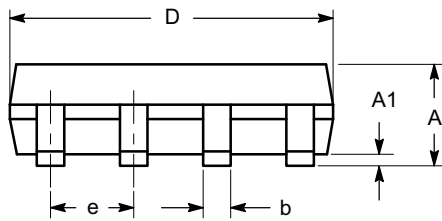
## PACKAGE DIMENSIONS

SOIC 8, 150 mils  
CASE 751BD-01  
ISSUE O

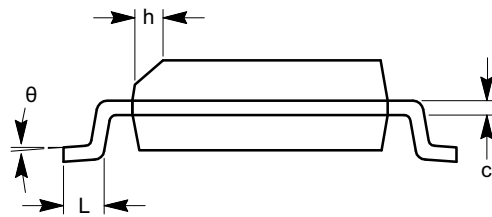


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW



END VIEW

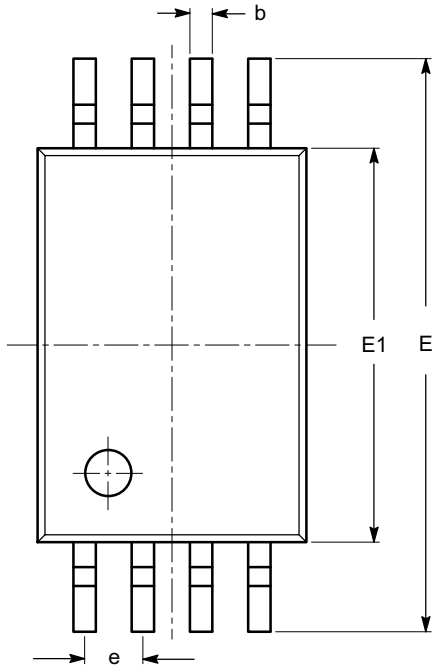
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

# CAT25640

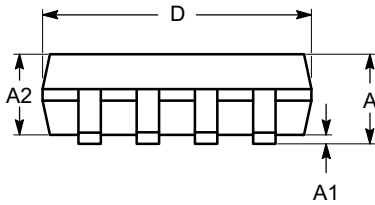
## PACKAGE DIMENSIONS

TSSOP8, 4.4x3  
CASE 948AL-01  
ISSUE O

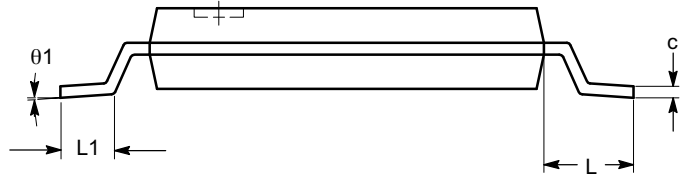


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

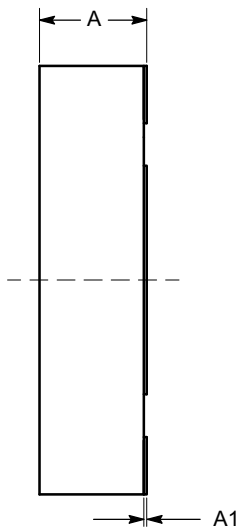
# CAT25640

## PACKAGE DIMENSIONS

TDFN8, 2x3  
CASE 511AK-01  
ISSUE A



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3	0.20 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e	0.50 TYP		
L	0.20	0.30	0.40



FRONT VIEW

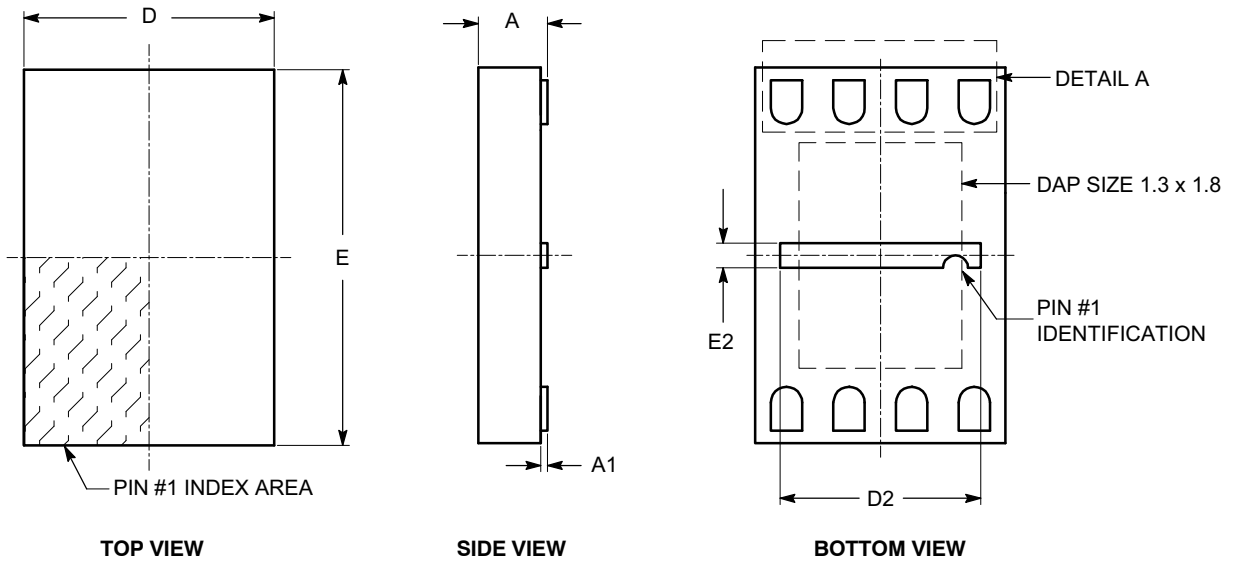
**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

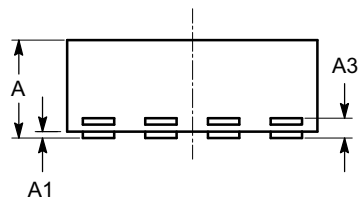
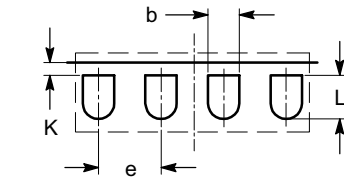
# CAT25640

## PACKAGE DIMENSIONS

UDFN8, 2x3  
CASE 517AX-01  
ISSUE O



SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
e	0.50 TYP		
K	0.10 REF		
L	0.30	0.35	0.40



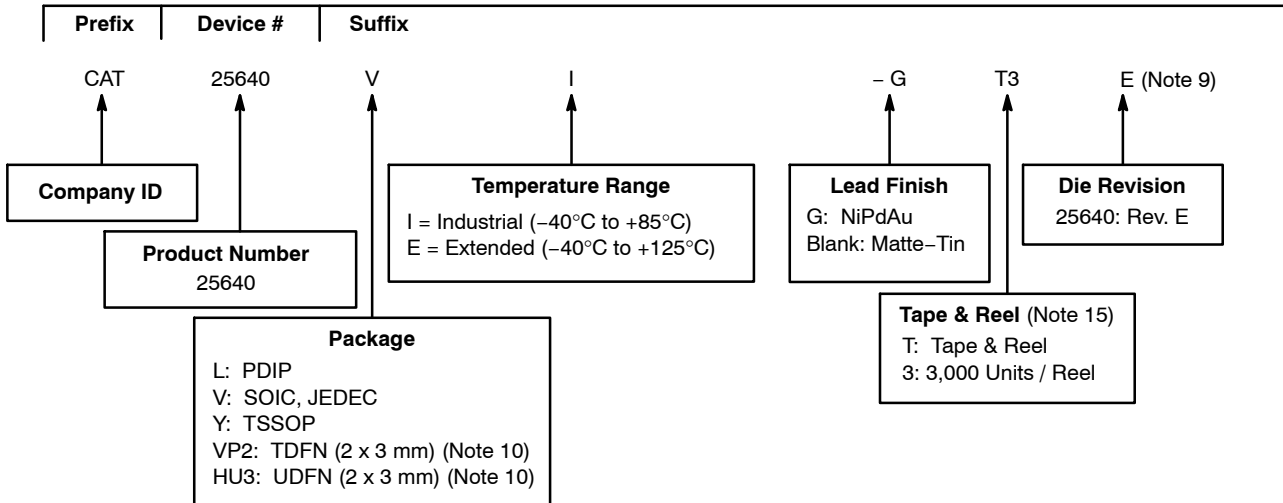
**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

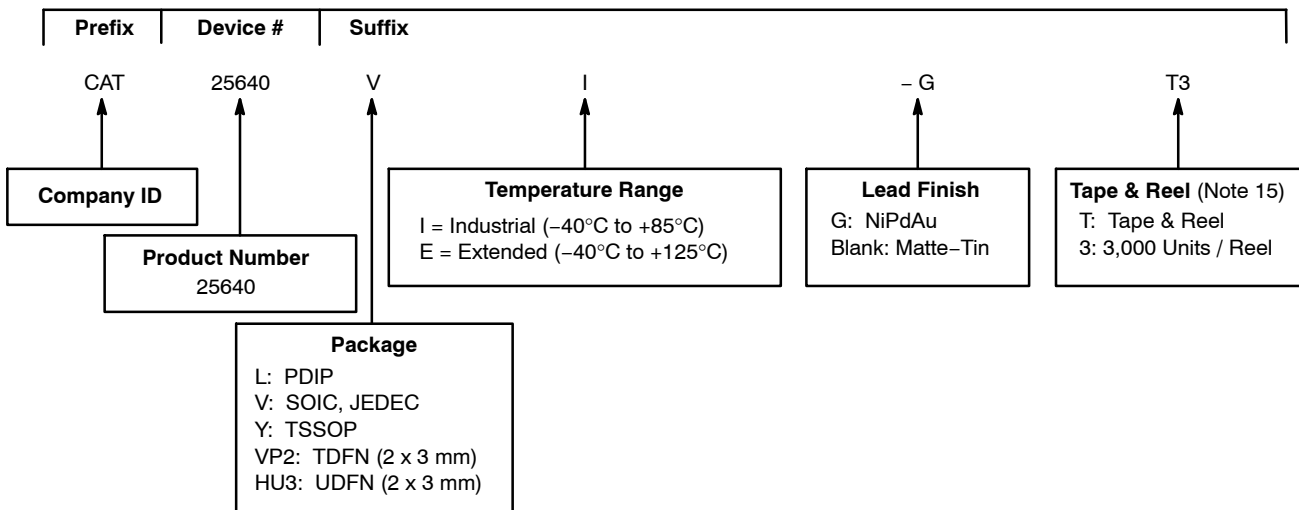
# CAT25640

## Example of Ordering Information

### CAT25640, Die Rev. E



### CAT25640, Die Rev. D (please refer to data sheet [Doc. No. MD-1128 Rev. D](#))



9. Letter "E" is required for product revision E only.

10. For the TDFN (VP2) and UDFN (HU3) packages, there is NO hyphen in the orderable part number. (Example: CAT25640HU3IGT3E)

11. All packages are RoHS-compliant (Lead-free, Halogen-free).

12. The standard lead finish is NiPdAu.

13. The device used in the above example is a CAT25640VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).

14. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

15. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative