L6360

IO-Link communication master transceiver IC

Datasheet – production data

Features

- Supply voltage from 18 to 32.5 V
- Programmable output stages: high-side, low-side or push-pull (< 2 Ω)
- Up to 500 mA L+ protected high-side driver
- Supports COM1, COM2 and COM3 mode
- Additional IEC61131-2 type-1 input
- Short-circuit and overcurrent output protection through current limitation and programmable cutoff current
- 3.3 V / 5 V, 50 mA linear regulator
- 5 mA IO-Link digital input
- Fast mode I^2C for IC control, configuration and diagnostic
- Diagnostic dual LED sequence generator and driver
- 5 V and 3.3 V compatible I/Os
- Overvoltage protection (> 36 V)
- Overtemperature protection
- ESD protection
- Miniaturized: VFQFPN-26L 3.5 x 5 x 1 mm package

Applications

- Industrial sensors
- Factory automation
- Process control

Description

The L6360 is a monolithic IO-Link master port compliant with PHY2 (3 wires) supporting COM1 (4.8 kbaud), COM2 (38.4 kbaud) and COM3 (230.4 kbaud) modes.

The C/Q_O output stage is programmable: high-side, low-side or push-pull; also cutoff current, cutoff current delay time, and restart delay are programmable.

VFQFPN-26L 3.5 x 5 x 1 mm

Cutoff current and cutoff current delay time, combined with thermal shutdown and automatic restart protect the device against overload and short-circuit.

C/Q_O and L+ output stages are able to drive resistive, inductive and capacitive loads. Inductive loads up to 10 mJ can be driven.

Supply voltage is monitored and low voltage conditions are detected.

The L6360 transfers, through the PHY2(C/Q_O pin), data received from a host microcontroller through the USART (IN C/Q_O pin), or to the USART (OUT C/Q_I pin) data received from PHY2 (C/Q_I pin).

To enable full IC control, configuration and monitoring (i.e. fault conditions stored in the status register), the communication between the system microcontroller and the L6360 is based on a Fast mode 2-wire I^2C.

The L6360 has nine registers to manage the programmable parameters and the status of the IC.

Monitored fault conditions are: L+ line, overtemperature, C/Q overload, linear regulator undervoltage, and parity check.

Internal LED driver circuitries, in open drain configuration, provide two programmable sequences to drive two LEDs.

This is information on a product in full production. www.st.com

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1 Block diagram

Figure 1. Block diagram

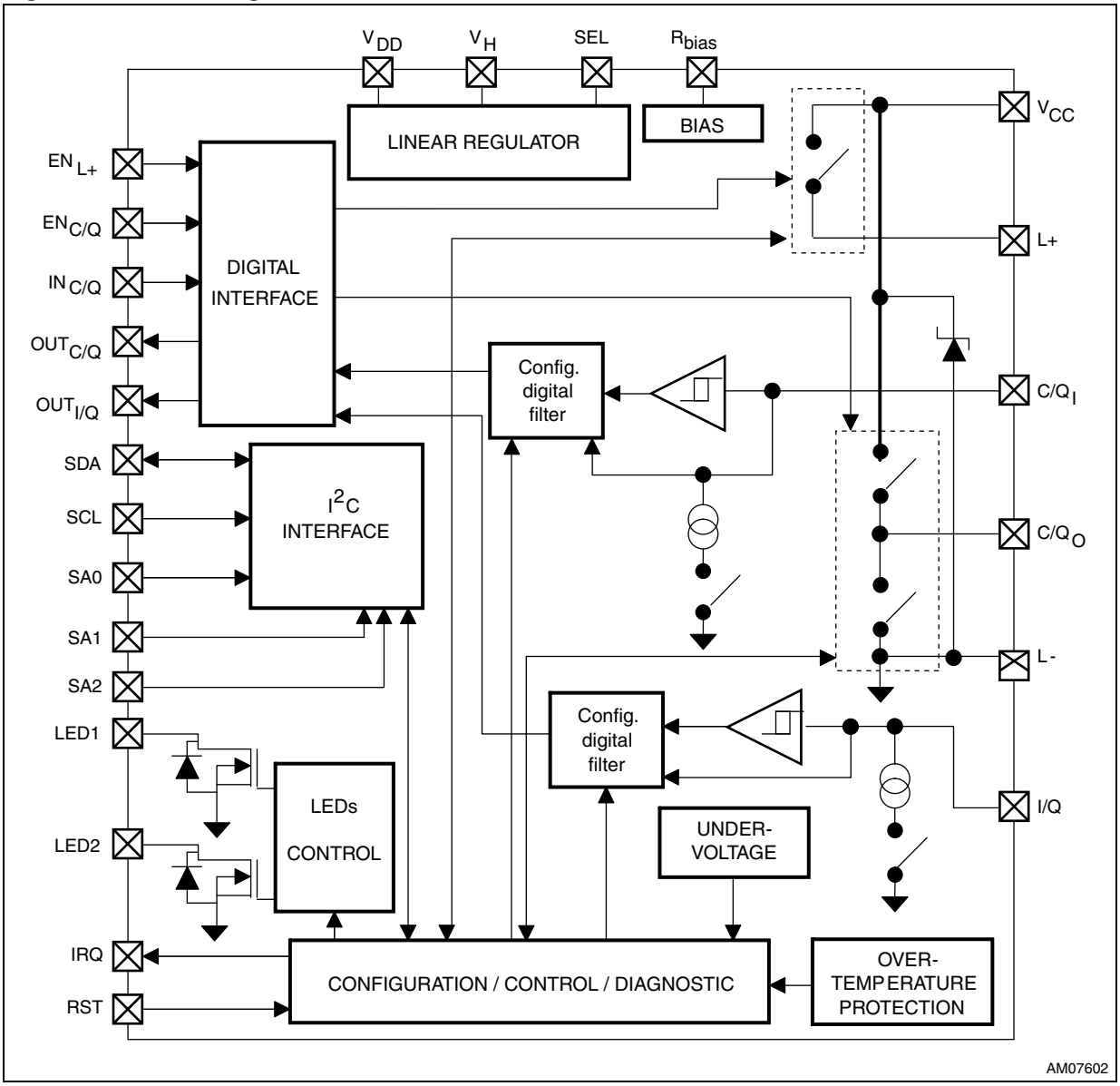


Table 1. Device summary

Order code	Package	Packaging
L6360	VFQFPN 3.5 x 5 x 1 - 26 leads	Tray
L6360TR	VFQFPN 3.5 x 5 x 1 - 26 leads	Tape and reel

2 Pin connections

Figure 2. Pin connections (top view)

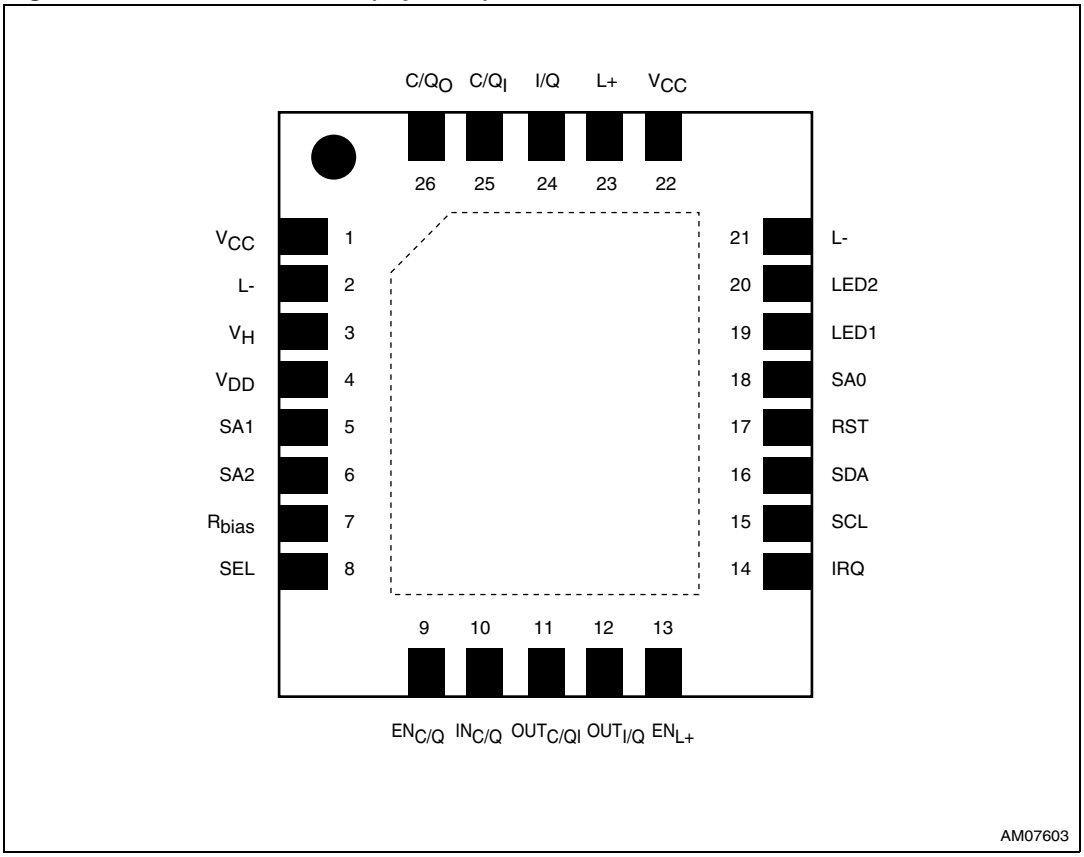


Table 2. Pin description

Pin	Name	Description	Type
1	V_{CC}	IC power supply	Supply
2	L-	L- line (IC ground)	Supply
3	V_H	Linear regulator supply voltage	Supply
4	V_{DD}	Linear regulator output voltage	Output
5	SA1	Serial address 1	Input
6	SA2	Serial address 2	Input
7	R_{bias}	External resistor for internal reference generation	Input
8	SEL	Linear regulator 3.3 V/5 V voltage selection. Output is 5 V when SEL pin is pulled to GND.	Input
9	$EN_{C/Q}$	C/Q output enable	Input
10	$IN_{C/Q}$	C/Q channel logic input	Input
11	$OUT_{C/Q}$	C/Q channel logic output	Output
12	$OUT_{I/Q}$	I/Q channel logic output	Output

Table 2. Pin description (continued)

Pin	Name	Description	Type
13	EN_{L+}	L+ switch enable. When EN_{L+} is high the switch is closed	Input
14	IRQ	Interrupt request signal (open drain)	Output
15	SCL	Serial clock line	Input
16	SDA	Serial data line	Input/output
17	RST	Reset - active low	Input
18	SA0	Serial address 0	Input
19	LED1	Status/diagnostic LED (open drain)	Output
20	LED2	Status/diagnostic LED (open drain)	Output
21	L-	L- line (IC ground)	Supply
22	V_{CC}	IC power supply	Supply
23	L+	L+ line	Supply
24	I/Q	I/Q channel line	Input
25	C/Q_I	Transceiver (C/Q channel) line	Input
26	C/Q_O	Transceiver (C/Q channel) line	Output

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	V_{CLAMP}	V
V_{SEL}	Linear regulator selection pin voltage	-0.3 to 4	V
V_{DD}	Linear regulator output voltage	5.5	V
V_H	Linear regulator input voltage	V_{CC}	V
$V_{INC/Q}$, $_{ENC/Q}$, $_{ENL+}$	$IN_{C/Q}$, $EN_{C/Q}$, EN_{L+} voltage	-0.3 to V_{DD} + 0.3	V
V_{SDA}, $_{SCL}$, $_{SA0}$, $_{1}$, $_{2}$	I^2C voltage	-0.3 to V_{DD} + 0.3	V
V_{LED1}, $_{2}$	LED1, 2 voltage	-0.3 to V_{DD} + 0.3	V
$V_{C/QI}$, $V_{I/Q}$	C/Q_I, I/Q voltage	-0.3 to V_{CC} + 0.3	V
V_{RST}	Reset voltage	-0.3 to V_{DD} + 0.3	V
V_{IRQ}	IRQ voltage	-0.3 to V_{DD} + 0.3	V
V_{Rbias}	External precision resistance voltage	-0.3 to 4	V
V_{ESD}	Electrostatic discharge (human body model)	2000	V
I_{CLAMP}	Current through V_{CLAMP} in surge test (1 kV, 500 Ω) condition	2	A
$I_{C/QO}$, I_{L+}	C/Q_O, L+ current (continuous)	Internally limited	A
$I_{OUTC//Q}$, $I_{OUTI/Q}$	$OUT_{C/Q}$, $OUT_{I/Q}$ output current	± 5	mA
I_{SDA}	I^2C transmission data current (open drain pin)	10	mA
I_{IRQ}	Interrupt request signal current	10	mA
I_{LED1}, $_{2}$	LED1, 2 current	10	mA
E_{load}	L+ demagnetization energy	10	mJ
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
P_{LR}	Linear regulator power dissipation	200	mW
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature	-55 to 150	°C

4 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	-	18		32.5	V
V_H	Linear regulator input voltage		7		V_{CC}	V
f_{SCL}	SCL clock frequency				400	kHz
R_{bias}	Precision resistance		-0.1%	124	0.1%	kΩ
T_J	Junction temperature		-40		125	°C

Table 5. Thermal data

Symbol	Parameter	Typ.	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction-to-case	6	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient(1)	50	°C/W

1. Mounted on FR4 PCB with 2 signal Cu layers and 2 power Cu layers interconnected through vias.

5 Electrical characteristics

(18 V < V_{CC} < 30 V; -25 °C < T_J < 125 °C; V_{DD} = 5 V; unless otherwise specified.)

Table 6. Electrical characteristics - power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CLAMP}	Voltage clamp	I = 5 mA	36			V
V_{UV}	Undervoltage ON-threshold		16	17	18	V
V_{UVH}	Undervoltage hysteresis		0.3	1		V
$V_{REGLN5H}$	Linear regulator undervoltage high threshold	SEL = L	4.3		4.7	V
$V_{REGLN5L}$	Linear regulator undervoltage low threshold	SEL = L	3.6		4.2	V
$V_{REG5HYS}$	Linear regulator undervoltage hysteresis	SEL = L	0.1			V
$V_{REGLN33H}$	Linear regulator undervoltage high threshold	SEL = H	2.8		3.1	V
$V_{REGLN33L}$	Linear regulator undervoltage low threshold	SEL = H	2.5		2.7	V
$V_{REG33HYS}$	Linear regulator undervoltage hysteresis	SEL = H	0.1			V
V_{QTHH}	C/Q_I and I/Q upper voltage threshold		10.5		12.9	V
V_{QTHL}	C/Q_I and I/Q lower voltage threshold		8		11.4	V
V_{QHY}	C/Q and I/Q hysteresis voltage		1			V
V_{demag}	L+ demagnetization voltage	I = 5 mA	-8.5	-6.5	-4.8	V
V_{fHS}	C/Q high-side freewheeling diode forward voltage	I = 10 mA		0.5		V
V_{fLS}	C/Q low-side freewheeling diode forward voltage	I = 10 mA		0.5		V
V_{LTHOFF}	L+ line diagnostic lower threshold		9	10	11	V
V_{LTHY}	L+ line diagnostic hysteresis		0.1	1		V
V_{LTHON}	L+ line diagnostic upper threshold		10	11	12	V
I_S	Supply current	OFF-state		100		µA
		ON-state V_{CC} at 32.5 V		4		mA
I_{OFFCQ}	OFF-state C/Q_O current	$EN_{C/Q}$ = 0, $V_{C/Q}$ = 0 V			1	µA
I_{COQ}	C/Q_O low- and high-side cutoff current	Programmable (see *Control register 1*)	70	115	190	mA
			150	220	300	mA
			290	350	440	mA
			430	580	720	mA

Table 6. Electrical characteristics - power section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{LIMQ}	C/Q_O low- and high-side limitation current		500		1600	mA
I_{OFFL}	L+ OFF-state current	EN_{L+} = 0, V_{L+} = 0 V	0		200	µA
I_{COL}	L+ cutoff current		480	580	730	mA
I_{LIML}	L+ limitation current		500		1600	mA
$I_{INC/Qi}$	C/Q_I pull-down current	Programmable (see section *Control register 2*)	5		6.5	mA
			2		3.3	mA
$I_{INI/Q}$	I/Q pull-down current	(see *Control register 2*)	2		3	mA
R_{ONL}	L+ high-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		1		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			2	Ω
R_{ONCQH}	C/Q_O high-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		1		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			2	Ω
R_{ONCQL}	C/Q_O low-side ON-state resistance	I_{OUT} = 0.2 A at T_J = 25 °C		0.6		Ω
		I_{OUT} = 0.2 A at T_J = 125 °C			1.2	Ω
$t_{dINC/Q}$	$IN_{C/Q}$ to C/Q_O propagation delay time	Push-pull (CQ_O rising edge)		140		ns
		Push-pull (CQ_O falling edge)		160		ns
$t_{ENC/Q}$	$EN_{C/Q}$ to C/Q_O propagation delay time	Push-pull (CQ_O rising edge)		110		ns
		Push-pull (CQ_O falling edge)		225		ns
t_{rPP}	C/Q rise time in push-pull configuration	10% to 90%. See *Figure 3*	250		860	ns
t_{fPP}	C/Q fall time in push-pull configuration	10% to 90%. See *Figure 3*	290		860	ns
t_{rHS}	C/Q rise time in high-side configuration			410		ns
t_{fHS}	C/Q fall time in high-side configuration			700		ns
t_{rLS}	C/Q rise time in low-side configuration			750		ns
t_{fLS}	C/Q fall time in low-side configuration			530		ns
t_{ENL}	EN_L to L+ propagation delay time			1		µs
t_{rL+}	L+ rise time			3		µs
t_{fL+}	L+ fall time			25		µs
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ (falling) propagation delay time			40		ns
	C/Q_I to $OUT_{C/Q}$ (rising) propagation delay time			100		ns
$t_{dI/Q}$	I/Q to $OUT_{I/Q}$ (falling) propagation delay time			40		ns
	I/Q to $OUTI_{/Q}$ (rising) propagation delay time			100		ns

Table 6. Electrical characteristics - power section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{dcoq}	C/Q_O low- and high-side cutoff current delay time	Programmable (see *Control register 1*)		100		µs
				150		µs
				200		µs
				250		µs
t_{rcoq}	C/Q_O restart delay time	Programmable (see *Control register 1*)		255 × t_{dcoq}		
				Latched(1)		
t_{dbq}	C/Q_I de-bounce time	Programmable (see *Control register 1*)		0		µs
				5		µs
				20		µs
				100		µs
t_{dbl}	I/Q de-bounce time	Programmable (see *Control register 2*)		0		µs
				5		µs
				20		µs
				100		µs
t_{dcol}	L+ cutoff current delay time	Programmable (see *Control register 2*)		500		µs
				0		µs
t_{rcol}	L+ restart delay time	Programmable (see *Control register 2*)		64		ms
				Latched(1)		
T_{JSD}	Junction temperature shutdown			150		°C
T_{JHYST}	Junction temperature thermal hysteresis			20		°C
T_{JRST}	Junction temperature restart threshold			130		°C

1. Unlatch through I^2C communication.

Table 7. Electrical characteristics - linear regulator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Linear regulator output voltage	SEL = L	4.84	5	5.13	V
		SEL = H	3.22	3.3	3.37	V
I_{LIMLR}	Linear regulator output current limitation		65			mA

Table 8. Electrical characteristics - logic inputs and outputs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level voltage				0.8	V
V_{IH}	Input high-level voltage		2.2			V
V_{IHIS}	Input hysteresis voltage			0.2		V
I_{IN}	Input current	V_{IN} = 5 V			1	µA
V_{OL}	Output low-level voltage	I_{OUT} = -2 mA			0.5	V
V_{OH}	Output high-level voltage	I_{OUT} = 2 mA	V_{DD} - 0.5 V			V
V_{LIRQ}	Open drain output low-level voltage	I_{OUT} = 2 mA			0.5	V

Table 9. Electrical characteristics - LED driving

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{LED1, 2}$	Open drain output low-level voltage	I_{LED} = 2 mA	-		0.5	V
I_{LED}	LED1, 2 leakage current	$V_{LED1} = V_{LED2}$ = 5 V		3		nA

Table 10. Electrical characteristics - I^2C (Fast mode)(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
$V_{IL(SDA)}$	SDA low-level input voltage			0.3	V
$V_{IH(SDA)}$	SDA high-level input voltage		0.7 x V_{DD}		V
$V_{IL(SCL)}$	SCL low-level input voltage			0.3	V
$V_{IH(SCL)}$	SCL high-level input voltage		0.7 x V_{DD}		V
I_{IN}	I^2C SDA, SCL input current	(0.1 x V_{DD}) <V_{IN} < (0.9 x V_{DD})	-10	10	µA
$t_{r(SDA)}$	I^2C SDA rise time		20 + 0.1 C_b	300	ns
$t_{r(SCL)}$	I^2C SCL rise time		20 + 0.1 C_b	300	ns
$t_{f(SDA)}$	I^2C SDA fall time		20 + 0.1 C_b	300	ns
$t_{f(SCL)}$	I^2C SCL fall time		20 + 0.1 C_b	300	ns
$t_{su(SDA)}$	SDA setup time		100		ns
$t_{h(SDA)}$	SDA hold time			0.9	µs

Table 10. Electrical characteristics - I²C (Fast mode)(1) (continued)

Symbol	Parameter	Test condition	Min.	Max.	Unit
$t_{su(STA)}$	Repeated START condition setup		0.6		µs
$t_{su(STO)}$	STOP condition setup time		0.6		µs
$t_{w(START/STOP)}$	STOP to START condition time (bus free)		1.3		µs
$t_{w(SCLL)}$	SCL clock low time		1.3		µs
$t_{w(SCLH)}$	SCL clock high time		0.6		µs
C_b	Capacitance for each bus line			400	pF
C_I	Capacitance for each I/O pin			10	pF

1. Values based on standard I²C protocol requirement.

Figure 3. Rise/fall time test setup

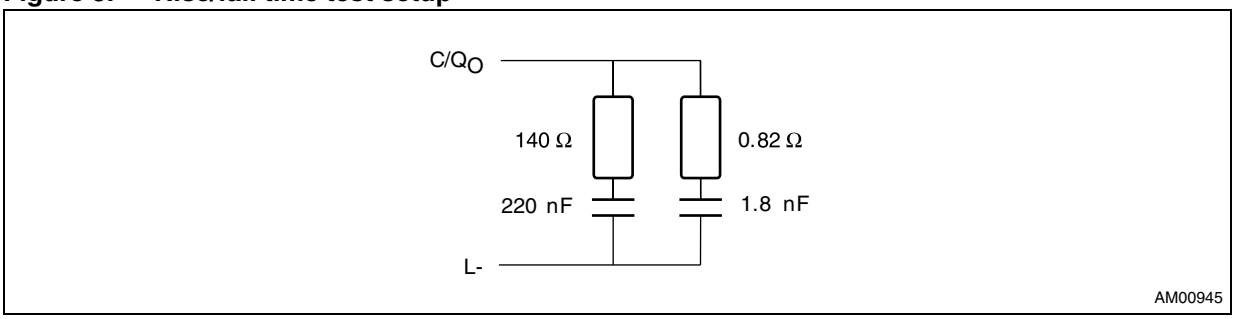


Figure 4. Normalized rise and fall time vs. output capacitor value (typ. values in push-pull configuration)

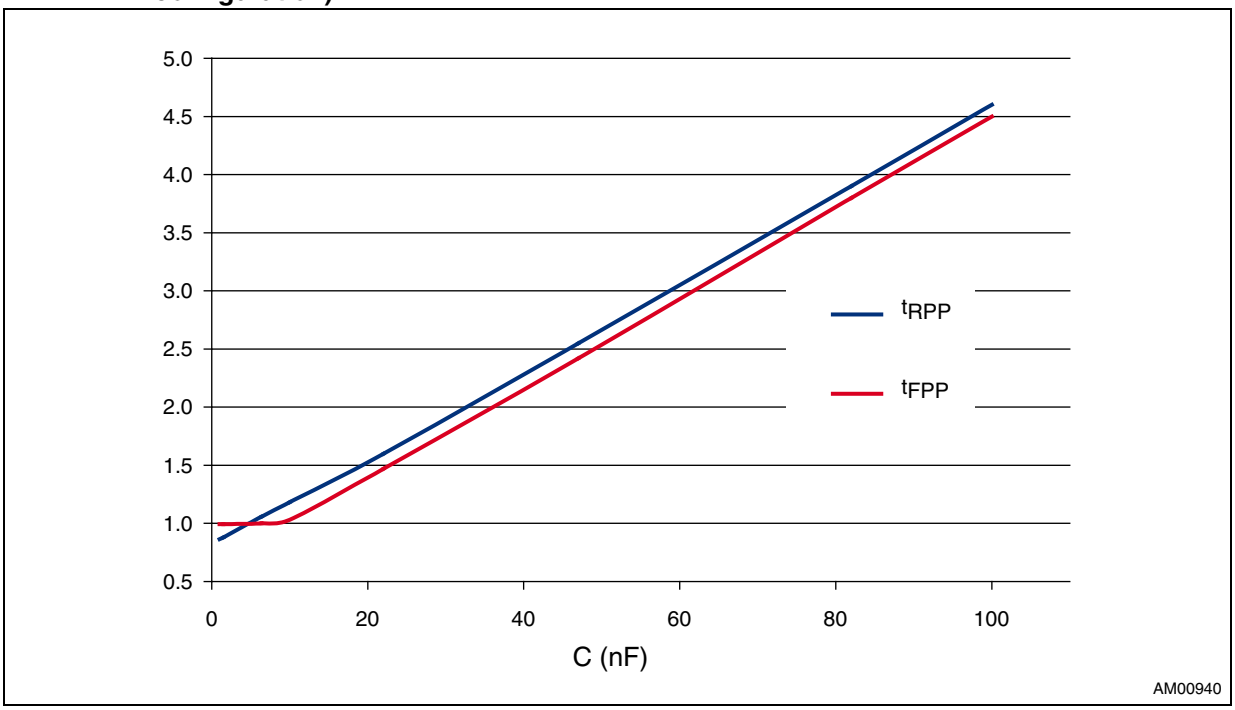


Table 11. Main parameter typical variation vs. +/- 1% variation of R_{bias} value

Symbol	Parameter	Typ. variation vs. R_{bias}		
		R_{bias} [kΩ]		
		122.74	124	125.24
I_s	Supply current	0.76%	0	-0.50%
$I_{INC/Qi}$	Input current C/Q_I pin (5.5 mA)	0.93%	0	-0.93%
$I_{INC/Qi}$	Input current C/Q_I pin (2.5 mA)	0.75%	0	-1.13%
$I_{INI/Q}$	Input current I/Q pin (2.5 mA)	0.85%	0	-0.85%
t_{dcoq}	C/Q_O low- and high-side cutoff current delay time	-2.44%	0	2.00%
I_{COQ}	C/Q_O low- and high-side cutoff current (115 mA)	1.19%	0	-1.28%
t_{dcol}	L+ cutoff current delay time (500 µs)	-0.95%	0	0.47%
I_{COL}	L+ cutoff current	1.36%	0	-0.91%
t_{rcol}	L+ restart delay time	-0.93%	0	0.97%
V_{UV}	Undervoltage ON-threshold	0.00%	0	0.00%
V_{DD}	Linear regulator output voltage (3.3 V)	-0.03%	0	0.03%
V_{DD}	Linear regulator output voltage (5 V)	-0.02%	0	0.02%
I_{LIMQ}	C/Q_O high-side limitation current	0.64%	0	-0.71%
I_{LIMQ}	C/Q_O low-side limitation current	0.28%	0	-1.47%
I_{LIML}	L+ limitation current	0.47%	0	-2.09%
V_{QTHH}	C/Q_I and I/Q upper voltage threshold	0.00%	0	0.00%
V_{QTHL}	C/Q_I and I/Q lower voltage threshold	0.00%	0	0.00%
V_{QHY}	C/Q and I/Q hysteresis voltage	0.00%	0	0.00%
t_{rPP}	C/Q rise time in push-pull configuration	-1.59%	0	1.18%
t_{fPP}	C/Q fall time in push-pull configuration	-2.14%	0	0.94%
$t_{dINC/Q}$	$I_{NC/Q}$ to C/Q_O propagation delay time	-1.44%	0	0.75%
$t_{dINC/Q}$	$IN_{C/Q}$ to C/Q_O propagation delay time	-2.36%	0	0.18%
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ propagation delay time	0.49%	0	1.13%
$t_{dC/Qi}$	C/Q_I to $OUT_{C/Q}$ propagation delay time	1.82%	0	0.03%
t_{dbq}	C/Q_I de-bounce time (100 µs)	-1.76%	0	1.50%
t_{dcoq}	C/Q_O low- and high-side cutoff current delay time (200 µs)	-1.27%	0	2.00%
I_{COQ}	C/Q_O low-side cutoff current (220 mA)	0.39%	0	-1.56%
I_{COQ}	C/Q_O low-side cutoff current (350 mA)	0.36%	0	-1.43%
I_{COQ}	C/Q_O low-side cutoff current (580 mA)	0.65%	0	-1.72%
t_{rcoq}	C/Q_O restart delay time	-0.90%	0	0.97%
I_{COQ}	C/Q_O high-side cutoff current (220 mA)	0.84%	0	-0.84%
I_{COQ}	C/Q_O high-side cutoff current (350 mA)	1.38%	0	-0.69%
I_{COQ}	C/Q_O high-side cutoff current (580 mA)	1.08%	0	-1.08%

6 Device configuration

SDA and SCL configure the L6360 device through I^2C.

6.1 I^2C single master bus interface

6.1.1 Introduction

The I^2C bus interface serves as an interface between the microcontroller and the serial I^2C bus.

It provides single master functions, and controls all I^2C bus-specific sequencing, protocol and timing.

It supports fast I^2C mode (400 kHz).

6.1.2 Main features

- Parallel bus / I^2C protocol converter
- Interrupt generation
- Fast I^2C mode
- 7-bit addressing.

6.1.3 General description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa.

The interface is connected to the I^2C bus by a data pin (SDA) and a clock pin (SCL).

6.1.4 SDA/SCL line control

SDA is a bi-directional line, SCL is the clock input. SDA should be connected to a positive supply voltage via a current-source or pull-up resistor. When the bus is free, both lines are HIGH.

The output stages of devices connected to the bus must have an open drain or open collector output to perform the wired AND function. Data on the I^2C bus can be transferred at rates up to 400 Kbit/s in fast mode.

The number of interfaces connected to the bus is limited by the bus capacitance.

For a single master application, the master's SCL output can be a push-pull driver provided that there are no devices on the bus which would stretch the clock.

Transmitter mode: the microcontroller interface holds the clock line low before transmission.

Receiver mode: the microcontroller interface holds the clock line low after reception.

When the I^2C microcontroller cell is enabled, the SDA and SCL ports must be configured as floating inputs.

In this case, the value of the external pull-up resistors used depends on the application.

When the I^2C microcontroller cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

On the L6360, the SDA output is an open drain pin.

6.1.5 Mode selection

Possible data transfer formats are:

- The master transmitter transmits to the slave receiver. The transfer direction is not changed (see *Figure 5*).
- The slave receiver acknowledges each byte.
- The master reads data from the slave immediately after the first byte (see *Figure 6*). At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.

This first acknowledge is still generated by the slave.

Subsequent acknowledges are generated by the master. The STOP condition is generated by the master which sends a not-acknowledge ($\overline{A}$) just prior to the STOP condition.

Figure 5. A master transmitter addressing a slave receiver with a 7-bit address (the transfer is not changed)

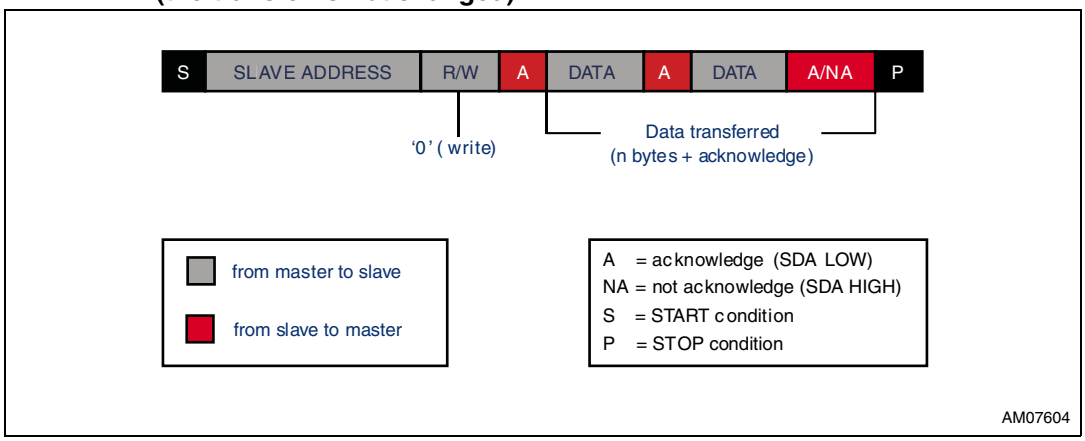
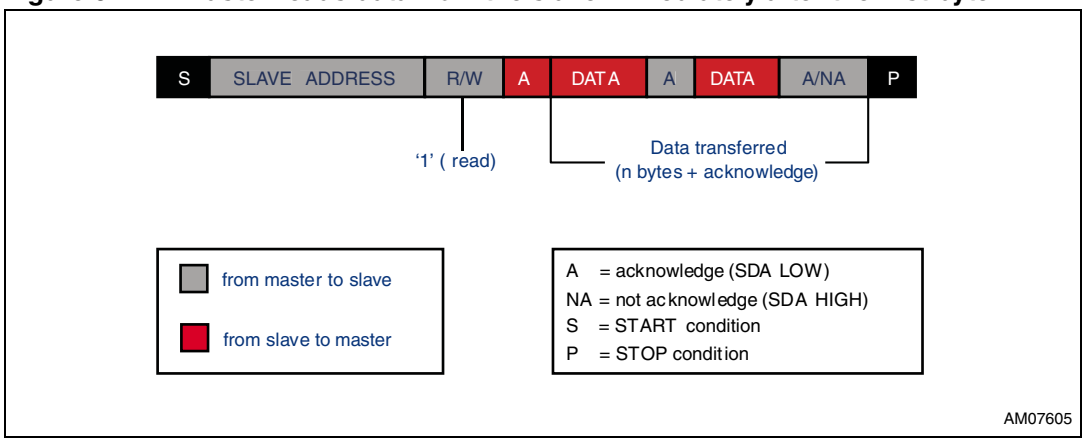


Figure 6. A master reads data from the slave immediately after the first byte



On the microcontroller, the interface can operate in the two following modes:

- Master transmitter/receiver
- Idle mode (default state)

The microcontroller interface automatically switches from idle to master receiver after it detects a START condition and from master receiver to idle after it detects a STOP condition.

On the L6360 the interface can operate in the two following modes:

- Slave transmitter/receiver
- Idle mode (default state)

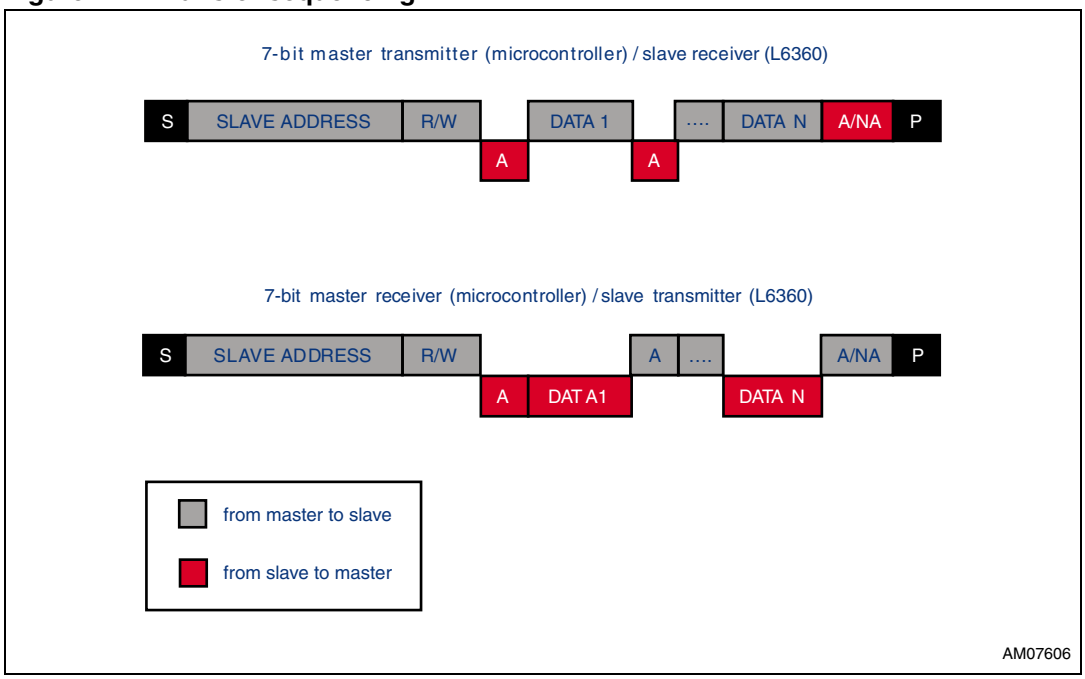
The interface automatically switches from idle to slave transmitter after it detects a START condition and from slave transmitter to idle after it detects a STOP condition.

6.1.6 Functional description

By default, the I^2C microcontroller interface operates in idle; to switch from default Idle mode to Master mode a START condition generation is needed.

The transfer sequencing is shown in *Figure 7*.

Figure 7. Transfer sequencing



6.1.7 Communication flow

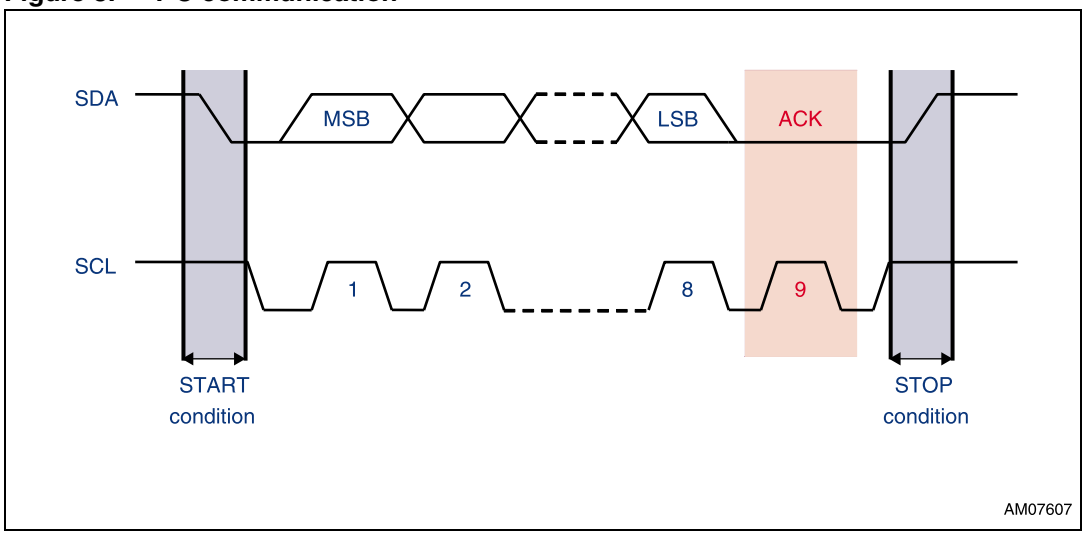
The communication is managed by the microcontroller that generates the clock signal.

A serial data transfer always begins with a START condition and ends with a STOP condition.

Data is transferred as 8-bit bytes, MSB first.

The first byte following the START condition contains the address (7 bits). A 9th clock pulse follows the 8th clock cycle of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter.

Figure 8. I^{2}C communication



Each byte is followed by an acknowledgment bit as indicated by the A or A blocks in the sequence. A START condition immediately followed by a STOP condition (void message) is a prohibited format.

6.1.8 I^{2}C address

Each I^{2}C connected to the bus is addressable by a unique address.

The I^{2}C address is 7 bits long, and there is a simple master/slave relationship.

The LSB of the L6360 address can be programmed by means of dedicated IC pins (SA0, SA1 and SA2, which can be hard wired to V_{DD} or GND, or handled by µC outputs): the microcontroller can interface up to 8 L6360 ICs.

The I^{2}C inside the device has 5 pins:

- SDA: data
- SCL: clock
- SA0: LSB of L6360 address
- SA1: bit 1 of L6360 address
- SA2: bit 2 of L6360 address

The I^2C L6360 IC address is:

- Fixed part (4 MSBits): set to “1100”
- Programmable part (3 LSBits) by hardware: from “000 to 111" connecting SAx pins to GND or V_{DD}.

In L6360 the SDA is an open drain pin.

6.1.9 Internal registers

The L6360 has some internal registers to perform control, configuration, and diagnostic operations.

These registers are listed below:

- Status register
- Configuration register
- Control register 1
- Control register 2
- LED1 register MSB
- LED1 register LSB
- LED2 register MSB
- LED2 register LSB
- Parity register.

Each register is addressable:

Table 12. Register addresses

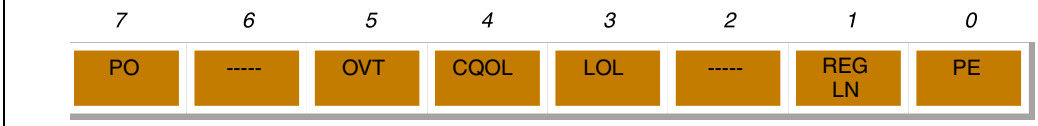
Address	Register name
0000	Status register
0001	Configuration register
0010	Control register 1
0011	Control register 2
0100	LED1 MSB
0101	LED1 LSB
0110	LED2 MSB
0111	LED2 LSB
1000	Parity register

Status register

Read only

Reset Value: [00000000]

Figure 9. Status register



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The status register stores diagnostic information. It can be read to check the status of the run-time of the device (faults, warning, transmission corrupted, etc.).

When a fault condition occurs, a bit (corresponding to the fault condition) in the status register is set and an interrupt (via the IRQ pin) is generated.

If there is no persistent fault condition, the status register is cleared after a successful *current read*.

Bit 7 = **PO**: *Power-on (L+ line)*.

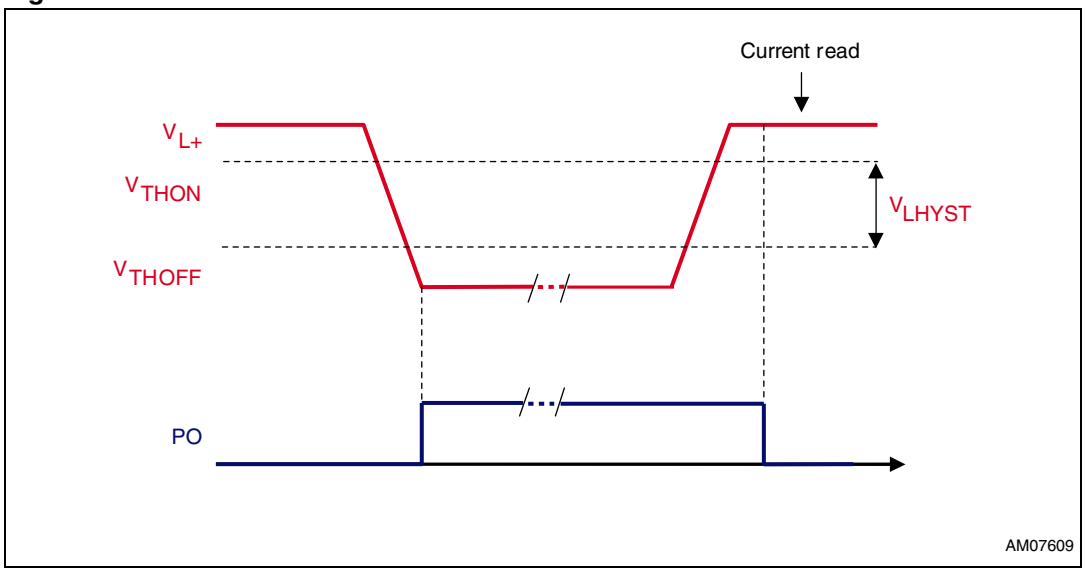
This bit indicates the status of L+ line voltage.

If the voltage goes under the lower threshold (V_{LTHOFF}) and EN_{L+} is high, the PO bit is set. It is reset after a successful *current read* if the L+ voltage has returned above the upper threshold V_{LTHON} and the read operation has begun after the bit has been set.

When the PO bit is high, IRQ is generated.

During EN_{L+} transition (from low-level to high-level) and during L+ line voltage transition, a fault condition is reported setting the PO bit and activating the IRQ pin. To reset the fault a successful *current read* is necessary.

Figure 10. Power-on bit behavior



Bit 6 = ***not used: always at zero***

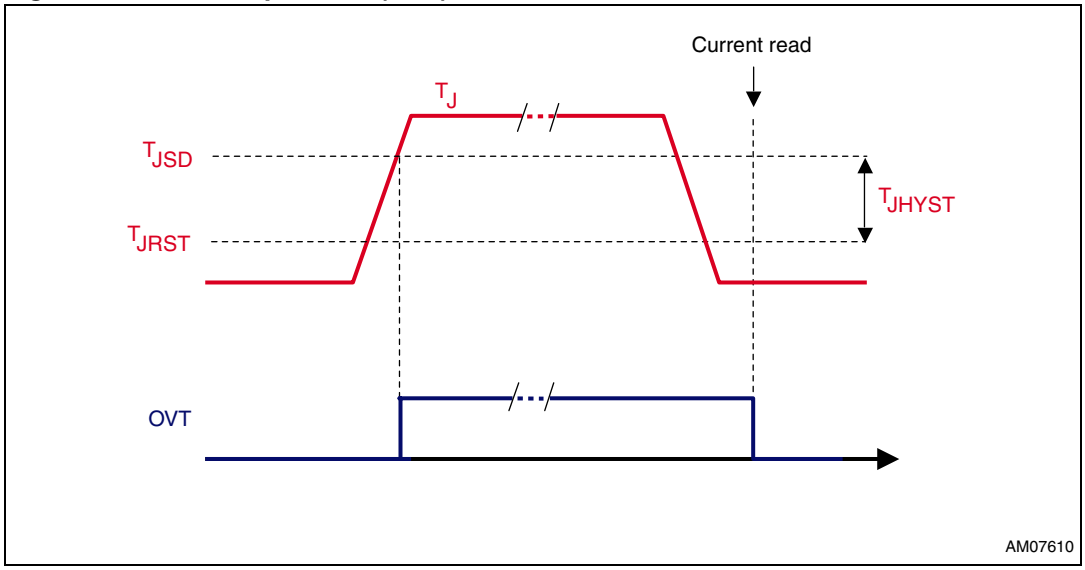
Bit 5 = **OVT**: *Overtemperature fault*

This bit indicates the status of the IC internal temperature.

If the temperature goes above the thermal shutdown threshold ($T > T_{JSD}$) the OVT bit is set. It is reset after a successful *current read* if the temperature has returned below the thermal restart threshold ($T_{JDS} - T_{JHIST}$) and the read operation has begun after the bit has been set.

When OVT bit is high, the power outputs are disabled and IRQ is generated.

Figure 11. Overtemperature (OVT) bit behavior



Bit 4 = **CQOL**: *C/Q overload*

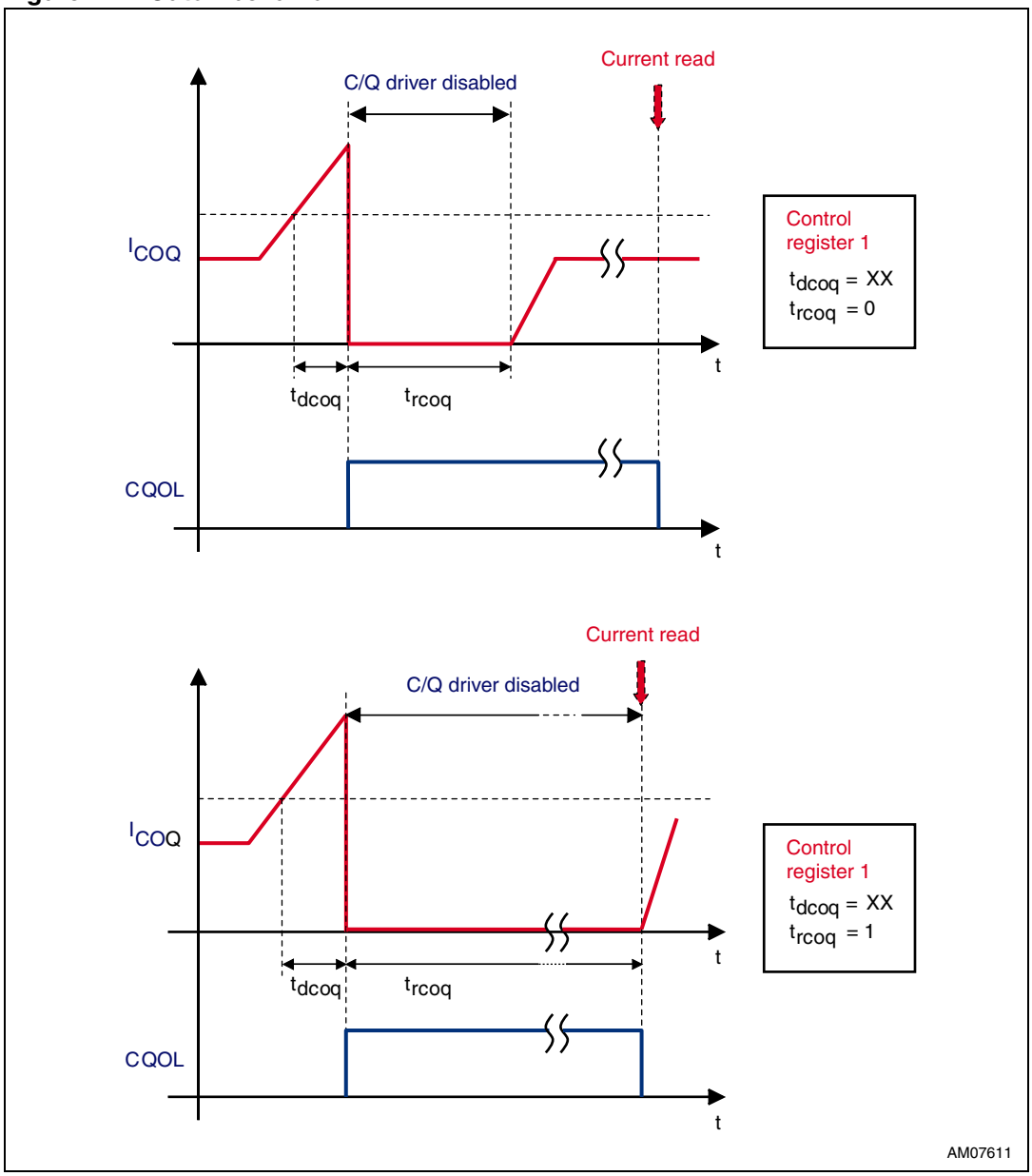
This bit is set if a cutoff occurs on the C/Q channel.

It is reset after a successful *current read* if the restart delay time (t_{rcoq}) has elapsed or the protection is latched (bit t_{rcoq} = 1 in *Control register 1*). The read operation should begin after the CQOL bit has been set. See also the *Control register 1* and *Transceiver* sections.

When **CQOL** bit is high, IRQ is generated.

When **CQOL** bit is high and the protection is latched (bit t_{rcoq} = 1 in *Control register 1*), the C/Q power output is disabled. See *Figure 12*.

Figure 12. Cutoff behavior



Bit 3 = **LOL**: *L+ overload*

This bit is set if a cutoff occurs on the L+ driver.

It is reset after a successful *current read* if the restart delay time (t_{rcol}) has elapsed or the protection is latched (bit t_{rcol} = 1 in *Control register 2*). The read operation should begin after the LOL bit has been set. See also the *Control register 2* and *Transceiver* sections.

When **LOL** bit is high, IRQ is generated.

When **LOL** bit is high and the protection is latched (bit t_{rcol} = 1 in *Control register 2*), the L+ power output is disabled.

The behavior is the same as the C/Q driver (see *Figure 12*).

Bit 2 = ***not used: always at zero***

Bit 1 = **REG LN**: *Linear regulator undervoltage fault*

This bit is set in case of undervoltage of the linear regulator output (V_{REGLNL}). It is reset after a successful *current read* if the linear regulator output has returned to normal operation and the read operation has begun after the bit has been set.

When REG LN bit is high, IRQ is generated.

Bit 0 = **PE**: *Parity check error*

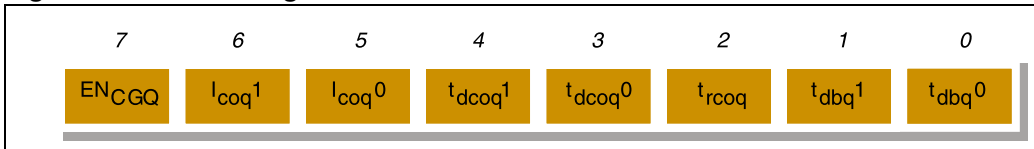
This flag is set if parity error occurs.

Control register 1

Read/write

Reset value: [00100001]

Figure 13. Control register 1



The control register holds the parameters to control the L6360. See also the *Transceiver* section.

Bit 7 = **EN_{CGQ}**: C/Q_I pull-down enable

Table 13. EN_{CGQ}: C/Q pull-down enable

EN_{CGQ}	Pull-down generator status	
0	Always OFF	
1	If $EN_{C/Q}$ = 0	ON
	If $EN_{C/Q}$ = 1	OFF

Bit 6:5 = **I_{COQ} [1:0]**: C/Q_O HS and LS cutoff current

This bit is used to configure the cutoff current value on the C/Q channel, as shown in *Table 14*.

Table 14. I_{COQ}: C/Q_O HS and LS cutoff current

I_{coq} [1]	I_{coq}[0]	Typ.
0	0	115 mA
0	1	220 mA
1	0	350 mA
1	1	580 mA

Bit 4:3 = **t_{dcoq} [1:0]**: C/Q_O HS and LS cutoff current delay time

The channel output driver is turned off after a delay (t_{dcoq}) programmable by means of these two bits:

Table 15. t_{dcoq}: C/Q_O HS and LS cutoff current delay time

t_{dcoq} [1]	t_{dcoq}[0]	Typ.
0	0	100 µs
0	1	150 µs
1	0	200 µs
1	1	250 µs(1)

1. According to power dissipation at 2 kHz switching, C < 1 µF, power dissipation 0.7 W.

Bit 2 = **t_{rcoq}**: C/Q_O restart delay time

After a cutoff event, the channel driver automatically restarts after a delay (t_{rcoq}) programmable by means of this bit:

Table 16. t_{rcoq}: C/Q_O restart delay time

t_{rcoq}	Typ.
0	255 x t_{dcoq}
1	Latched(1)

1. Unlatch through I^2C communication (reading or writing any internal registers).

Bit 1:0 = **t_{dbq} [1:0]**: C/Q_I de-bounce time

De-bounce time is the minimum time that data must be in a given state after a transition.

It is a programmable time, and can be configured as shown in *Table 17*.

Table 17. t_{dbq}: C/Q_I de-bounce time

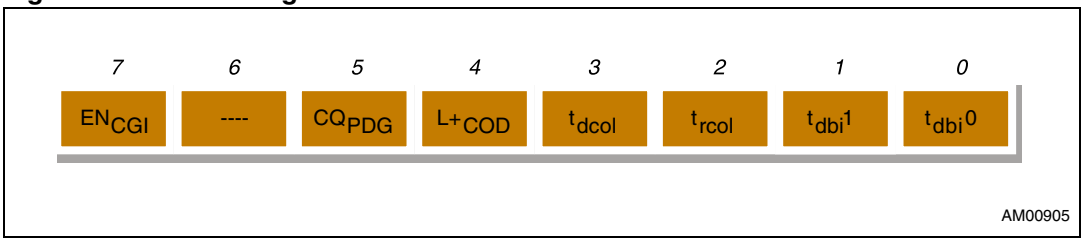
t_{dbq} [1]	t_{dbq} [0]	Typ.
0	0	0 µs
0	1	5 µs
1	0	20 µs
1	1	100 µs

Control register 2

Read/write

Reset value: [0x100001]

Figure 14. Control register 2



The control register holds the parameters to control the L6360. See also the *Transceiver* section.

Bit 7 = **EN_{CGI}**: *I/Q pull-down enable*

Table 18. EN_{CGI}: I/Q pull-down enable

EN_{CGI}	Pull-down generator status
0	Always OFF
1	Always ON

Bit 5 = **CQ_{PDG}**: *C/Q, channel pull-down generators*

In order to reduce consumption, it is possible to switch from default to low-power configuration by resetting the CQ_{PDG} bit.

Table 19. CQ_{PDG}: C/Q pull-down generator switching

CQ_{PDG}	Pull-down generator status
0	$I_{INI/Qi}$ (input current C/Q_I pin) = 2.5 mA
1	$I_{INC/Qi}$ (input current C/Q_I pin) = 5.5 mA

Bit 4 = **$L+_{COD}$**: *L+ cutoff disable*

The cutoff function on the L+ switch can be enabled or disabled according to the $L+_{COD}$ bit.

Table 20. $L+_{COD}$: L+ cutoff disable

$L+_{COD}$	L+ cutoff current status
0	Enabled
1	Disabled

As the cutoff function is intended to protect the integrated switches against overload and short-circuit, disabling the cutoff is not recommended.

Bit 3 = **t_{dcol}**: *L+ cutoff current delay time*

The channel output driver is turned off after a delay (t_{dcol}) programmable by means of this bit:

Table 21. t_{dcol}: L+ HS cutoff current delay time

t_{dcol}	Typ.
0	500 µs
1	0 µs

Bit 2 = t_{rcol}: *L+ restart delay time*

After a cutoff event, the channel driver automatically restarts again after a delay (t_{rcol}) programmable by means of this bit:

Table 22. t_{rcol}: L+ restart delay

t_{rcol}	Typ.
0	64 ms
1	Latched(1)

1. Unlatch through I^2C communication (reading or writing any internal registers).

Bit 1:0 = **t_{dbi} [1:0]**: *I/Q de-bounce time*

De-bounce time is the minimum time that data must be in a given state after a transition. It is a programmable time, and it can be configured as shown in *Table 23*.

Table 23. t_{dbi}: I/Q de-bounce time

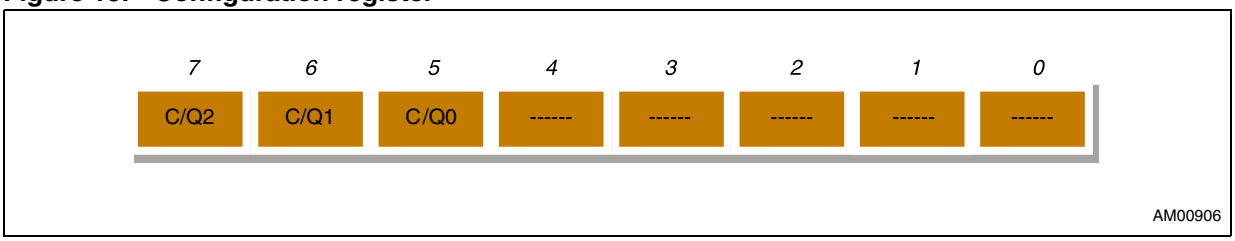
t_{dbi} [1]	t_{dbi} [0]	Typ.
0	0	0 µs
0	1	5 µs
1	0	20 µs
1	1	100 µs

Configuration register

Read/write

Reset value: [100xxxxx]

Figure 15. Configuration register



The configuration register holds data to configure the L6360 IC.

Bit 7:5 = **C/Q[2:0]**: *C/Q output stage configuration*

Table 24. C/Q output stage configuration

C/Q[2]	C/Q[1]	C/Q[0]	Configuration	Notes
0	0	0	OFF	HS and LS are OFF regardless of the state of $EN_{C/Q}$ and $IN_{C/Q}$. The receiver is OFF regardless of the state of $EN_{C/Q}$.
0	0	1	Low-side	HS is always disabled. LS is ON when $IN_{C/Q}$ is high and $EN_{C/Q}$ is high, OFF in all other cases. Slow asynchronous decay when the LS is turned off by $EN_{C/Q}$ or in case of cutoff. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.
0	1	0	High-side	LS is always disabled. HS is ON when $IN_{C/Q}$ is low and $EN_{C/Q}$ is high, OFF in all other cases. Slow asynchronous decay if the HS is turned off by $EN_{C/Q}$ or in case of cutoff. The internal pull-down current generator on C/Q_I should be disabled through *Control register 1*, unless C/Q_I is connected to C/Q_O through a 100 Ω (or more) resistor. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.

Table 24. C/Q output stage configuration (continued)

C/Q[2]	C/Q[1]	C/Q[0]	Configuration	Notes
0	1	1	Push-pull	$IN_{C/Q}$ low and $EN_{C/Q}$ high: HS ON and LS OFF. $IN_{C/Q}$ high and $EN_{C/Q}$ high: LS ON and HS OFF. If $EN_{C/Q}$ is low, both HS and LS are OFF. Slow asynchronous decay in case of cutoff or turn-off of both switches. An internal deadtime is generated between each LS turn-off and the following HS turn-on and between each HS turn-off and the following LS turn-on. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.
1	0	0	TRISTATE	HS and LS are OFF regardless of the state of $EN_{C/Q}$ and $IN_{C/Q}$. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.
1	0	1	Low-side ON	LS is ON regardless of the state of $EN_{C/Q}$ and $IN_{C/Q}$. Slow asynchronous decay in case of cutoff. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.
1	1	0	High-side ON	HS is ON regardless of the state of $EN_{C/Q}$ and $IN_{C/Q}$. Slow asynchronous decay in case of cutoff. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.
1	1	1	Push-pull inductive load	$IN_{C/Q}$ low and $EN_{C/Q}$ high: HS ON and LS OFF. $IN_{C/Q}$ high and $EN_{C/Q}$ high: LS ON and HS OFF. If $EN_{C/Q}$ is low, both HS and LS are OFF. Slow asynchronous decay in case of cutoff or turn-off of both switches. An internal deadtime is generated between each LS turn-off and the following HS turn-on and between each HS turn-off and the following LS turn-on. The receiver is OFF when $EN_{C/Q}$ is high: $OUT_{C/Q}$ is high. The receiver is ON when $EN_{C/Q}$ is low: if C/Q_I is high, $OUT_{C/Q}$ is low. if C/Q_I is low, $OUT_{C/Q}$ is high.

Note: See also the Demagnetization section.

In order to reduce the risk of damage to the output stage (e.g. switching from push-pull inductive load to any transceiver configuration while an inductive load has some residual energy), the user must not switch between any two “active” (low-side, high-side, push-pull, low-side ON, high-side ON, push-pull inductive load) configurations of the bridge.

For example, if the microcontroller needs to switch from push-pull to high-side configuration, it needs to modify the configuration register twice:

First-step: switch from push-pull to OFF (or TRISTATE)

Second-step: switch from OFF (or TRISTATE) to high-side

If the microcontroller asks for a forbidden jump between configurations, the IC remains in the previous configuration and reports a parity error to the microcontroller.

In case of sequential write, no parity error is generated if the microcontroller rewrites the configuration register with the previous value; if the operation, instead, requires a forbidden jump, all data are rejected also for other registers (and a parity error is raised).

The L+ switch is a high-side switch. HS is ON when EN_{L+} is high, otherwise it is OFF. Fast decay with active clamp ($-V_{demag}$) is operated when the HS is turned off or in the case of cutoff.

Receiver I/Q is always ON.

Bit 4:2 = **not used**

Bit 1:0 = **not used**

LED registers

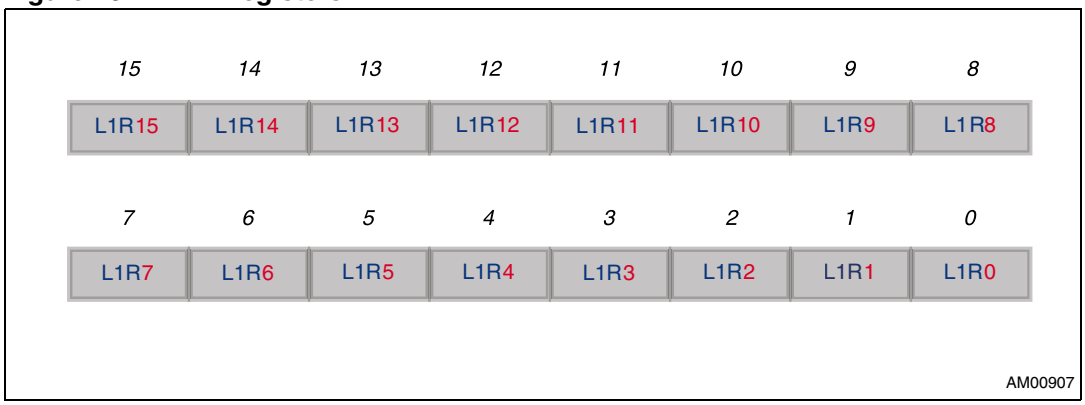
See also the *Diagnostic LED sequence generator and driver* section.

These registers are used to configure the two LED drivers integrated in the IC. Each LED driver has two associated registers and turns on or off the external LED according to the information stored in the registers, which are scanned with a rate of 63 ms per bit. LED drivers can be used for status or diagnostic information, or for other purposes, and should be configured by the host microcontroller.

LED1 registers

Reset value: [00000000]

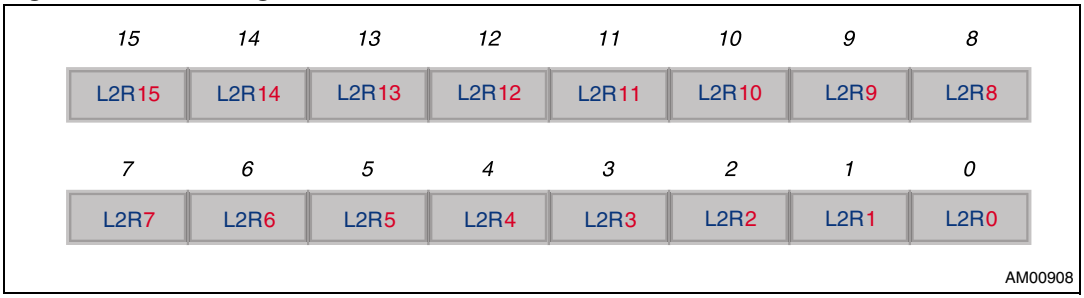
Figure 16. LED1 registers



LED2 registers

Reset value: [00000000]

Figure 17. LED2 registers

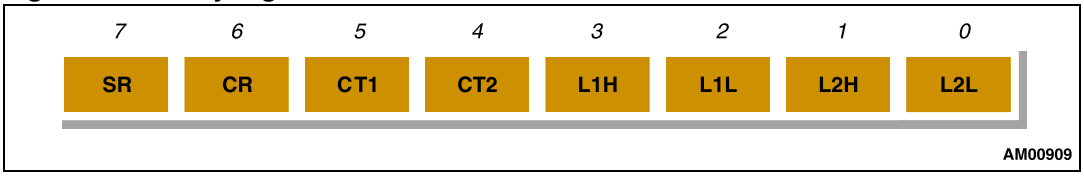


Parity register

Read only

Reset value: [00000000]

Figure 18. Parity register



This register stores the parity of each register, calculated after the L6360 receives data registers.

Bit 7 = **SR**: *Status register parity*

This bit is the parity of the status register.

Bit 6 = **CR**: *Configuration register parity*

This bit is the parity of the configuration register.

Bit 5 = **CT1**: *Control register 1 parity*

This bit is the parity of control register 1.

Bit 4 = **CT2**: *Control register 2 parity*

This bit is the parity of control register 2.

Bit 3 = **L1H**: *LED1 high register parity*

This bit is the parity of the LED1 MSB register (15 down to 8).

Bit 2 = **L1L**: *LED1 low register parity*

This bit is the parity of the LED1 LSB register (7 down to 0).

Bit 1 = **L2H**: *LED2 high register parity*

This bit is the parity of the LED2 MSB register (15 down to 8).

Bit 0 = **L2L**: *LED2 low register parity*

This bit is the parity of the LED2 LSB register (7 down to 0).

6.1.10 Startup default configuration

Table 25 and *Table 26* show the device registers default configuration.

Table 25. Parameter default configuration

Parameter	Default value
I_{coq}	220 mA
t_{dcoq}	100 µs
t_{rcoq}	25 ms
t_{dbq}	5 µs
t_{dcol}	0 µs
t_{rcol}	64 ms
t_{bdq}	5 µs
Output stage	TRISTATE

Table 26. Register default configuration

Registers	Bit position	Bit name	Reset value
Status register	Bit 7	PO	0
	Bit 6	Not used	x
	Bit 5	OVT	0
	Bit 4	CQOL	0
	Bit 3	IQOL	0
	Bit 2	Not used	x
	Bit 1	REG LN	0
	Bit 0	PE	0
Configuration register	Bit 7	C/Q2	1
	Bit 6	C/Q1	0
	Bit 5	C/Q0	0
	Bit 4	Not used	x
	Bit 3	Not used	x
	Bit 2	Not used	x
	Bit 1	Not used	x
	Bit 0	Not used	x

Table 26. Register default configuration (continued)

Registers	Bit position	Bit name	Reset value
Control register 1	Bit 7	EN_{CGQ}	0
	Bit 6	$I_{coq}1$	0
	Bit 5	$I_{coq}0$	1
	Bit 4	$t_{dcoq}1$	0
	Bit 3	$t_{dcoq}0$	0
	Bit 2	t_{rcoq}	0
	Bit 1	$t_{dbq}1$	0
	Bit 0	$t_{dbq}0$	1
Control register 2	Bit 7	EN_{CGI}	0
	Bit 6	Not used	x
	Bit 5	CQ_{PDG}	1
	Bit 4	$L+_{COD}$	0
	Bit 3	$t_{dcoi}0$	0
	Bit 2	t_{rcoi}	0
	Bit 1	$t_{dbi}1$	0
	Bit 0	$t_{dbi}0$	1
LED1 register MSB	Bit 7	L1R15	0
	Bit 6	L1R14	0
	Bit 5	L1R13	0
	Bit 4	L1R12	0
	Bit 3	L1R11	0
	Bit 2	L1R10	0
	Bit 1	L1R9	0
	Bit 0	L1R8	0
LED1 register LSB	Bit 7	L1R7	0
	Bit 6	L1R6	0
	Bit 5	L1R5	0
	Bit 4	L1R4	0
	Bit 3	L1R3	0
	Bit 2	L1R2	0
	Bit 1	L1R1	0
	Bit 0	L1R0	0

Table 26. Register default configuration (continued)

Registers	Bit position	Bit name	Reset value
LED2 register MSB	Bit 7	L2R15	0
	Bit 6	L2R14	0
	Bit 5	L2R13	0
	Bit 4	L2R12	0
	Bit 3	L2R11	0
	Bit 2	L2R10	0
	Bit 1	L2R9	0
	Bit 0	L2R8	0
LED2 register LSB	Bit 7	L2R7	0
	Bit 6	L2R6	0
	Bit 5	L2R5	0
	Bit 4	L2R4	0
	Bit 3	L2R3	0
	Bit 2	L2R2	0
	Bit 1	L2R1	0
	Bit 0	L2R0	0
Parity register	Bit 7	SR	0
	Bit 6	CR	0
	Bit 5	CT1	0
	Bit 4	CT2	0
	Bit 3	L1H	0
	Bit 2	L1L	0
	Bit 1	L2H	0
	Bit 0	L2L	0

6.2 Interrupt

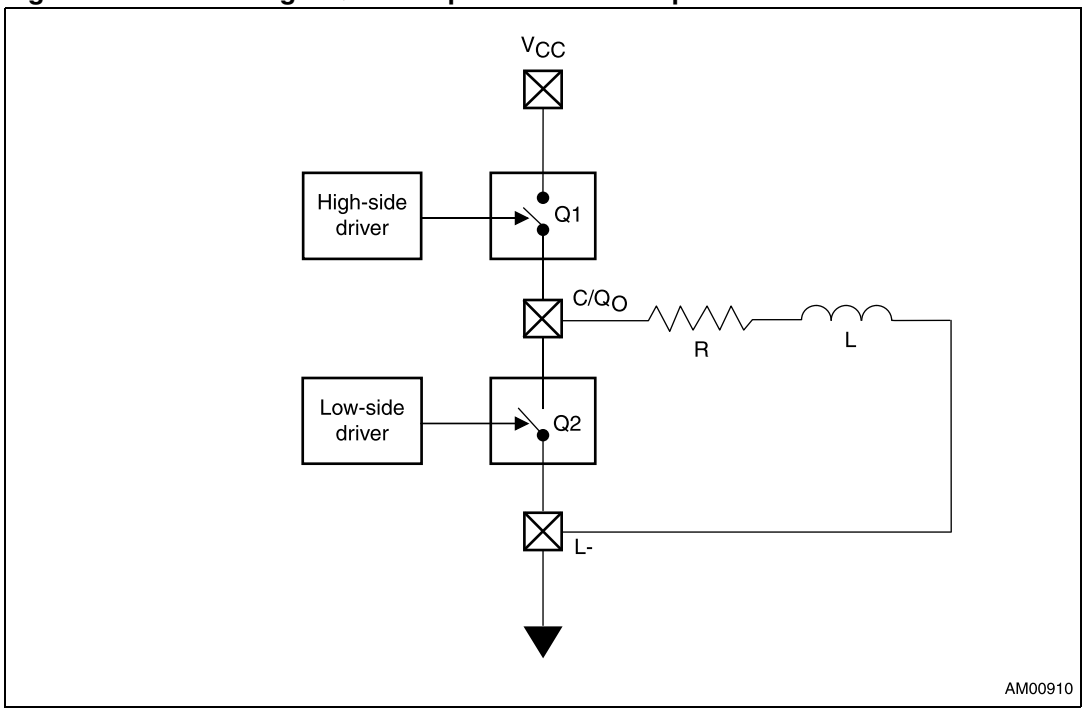
The IRQ pin (interrupt pin) should normally be held to a high logic level by an external pull-up resistor or microcontroller pin configuration. The internal structure is an open drain transistor.

It should be connected directly to the microcontroller so, in the case of a fault event (C/Q overload, power-on L+ line, overtemperature condition, etc.), it is pulled down to a low logic level, reporting the fault condition to the microcontroller. See also the *Status register* section.

6.3 Demagnetization

The power stage can be represented as in *Figure 19*.

Figure 19. Power stage. Q2 is not present on L+ output



When a power stage output (C/Q or L+) is connected to an inductance, the energy stored in the load is:

Equation 1

$$E = \frac{1}{2}LI^2$$

This energy must be properly dissipated at the switch-off. Without an appropriate circuitry the output voltage would be pulled to very negative values, therefore recovering the stored energy through the power transistor's breakdown.

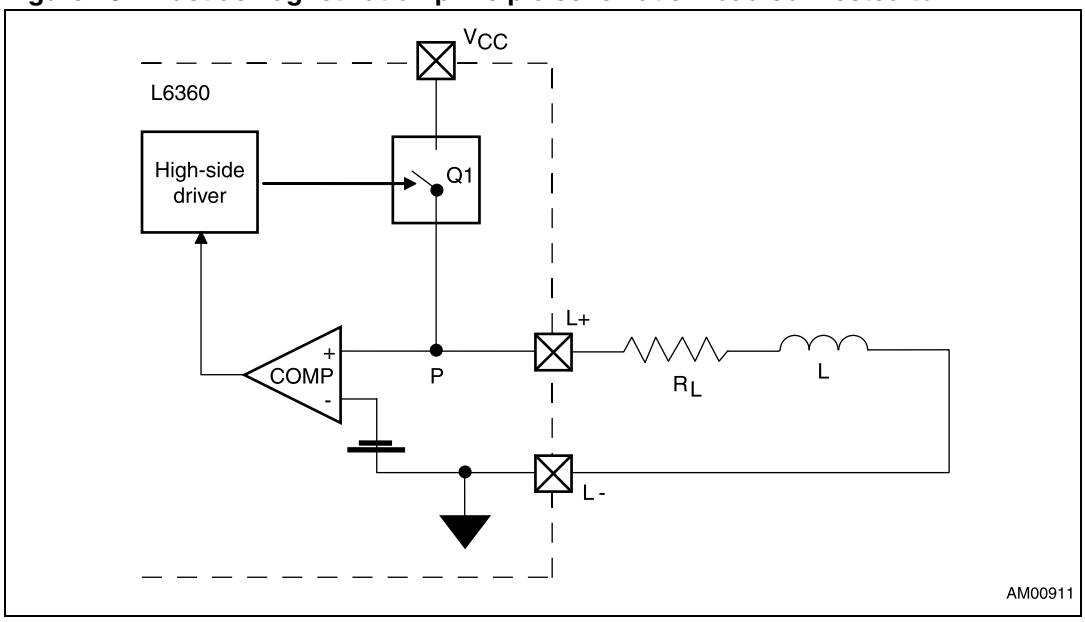
To avoid this, the output voltage must be clamped so that the voltage across the power switch does not exceed its breakdown voltage.

In the case of load connected between the C/Q_O pin and V_{CC}, at switch-off (of the low-side switch) the output is pushed to a voltage higher than V_{CC}.

6.3.1 Fast demagnetization

Applies to L+ channel only.

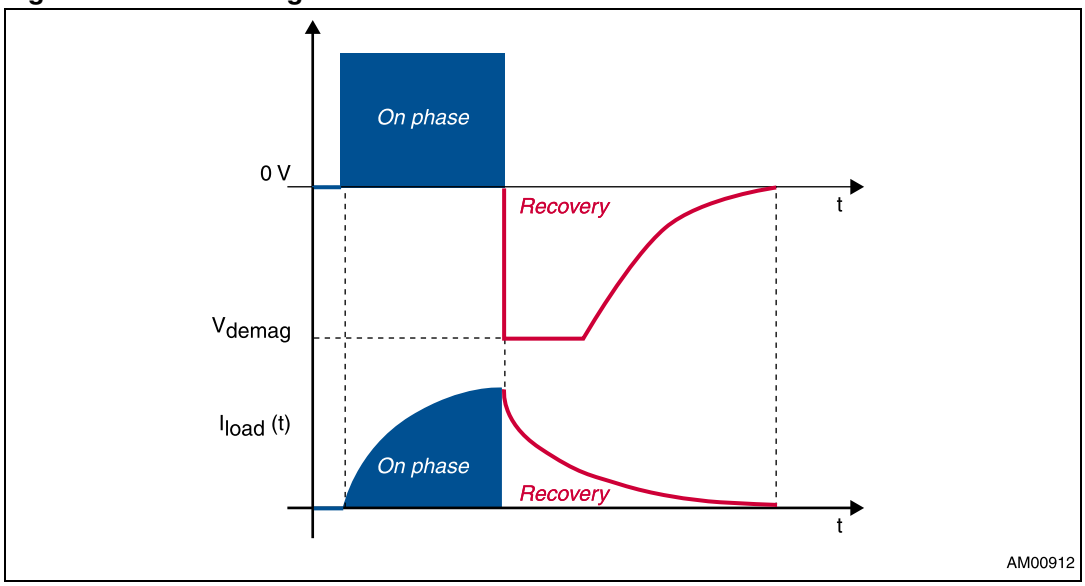
Figure 20. Fast demagnetization principle schematic. Load connected to L-



When a high-side driver turns off an inductance, a reversed polarity voltage appears across the load.

The output pin (L+) of the power switch becomes more negative than the ground until it reaches the demagnetization voltage, V_{demag}. The conduction state of the power switch Q1 is linearly modulated by an internal circuitry in order to keep the voltage at C/Q or the I/Q pin at about V_{demag} until the energy in the load has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

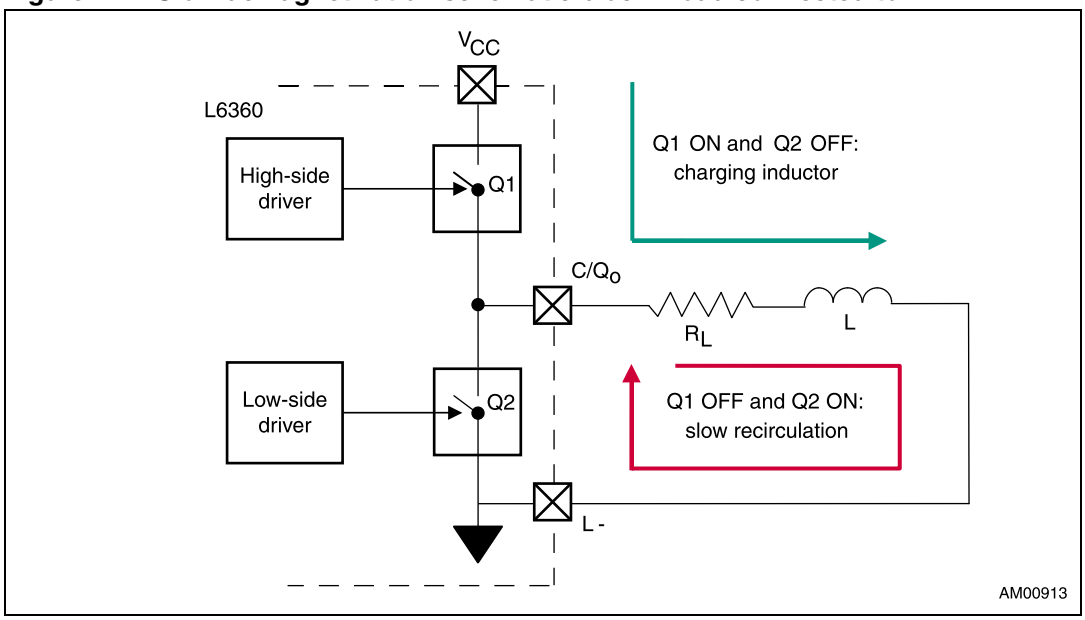
Figure 21. Fast demagnetization waveform. Load connected to L-



6.3.2 Slow demagnetization

Applies to C/Q channel.

Figure 22. Slow demagnetization schematic block. Load connected to L-

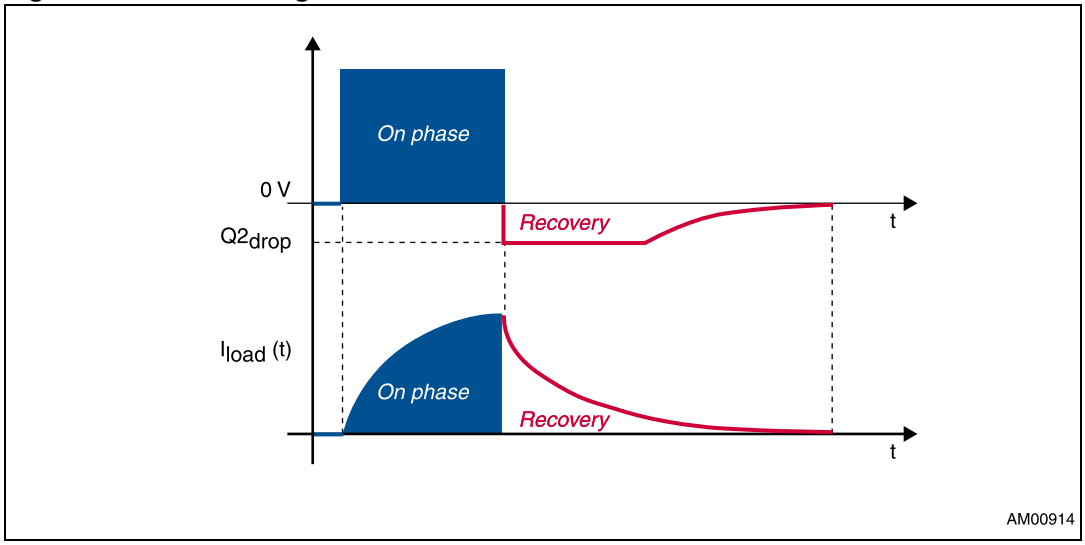


When a high-side driver turns off an inductance a reversed polarity voltage appears across the load.

In slow demagnetization configuration the low-side switch Q2 is ON and the C/Q pin is pulled at a voltage slightly (depending on Q2 drop) below the ground (L-). The energy is dissipated in both the IC internal switch and the load resistance.

In the case of load connected between the C/Q pin and V_{CC}, at switch-off (of the low-side switch Q2), the switch Q1 is ON and the output is pushed to a voltage slightly higher than V_{CC}.

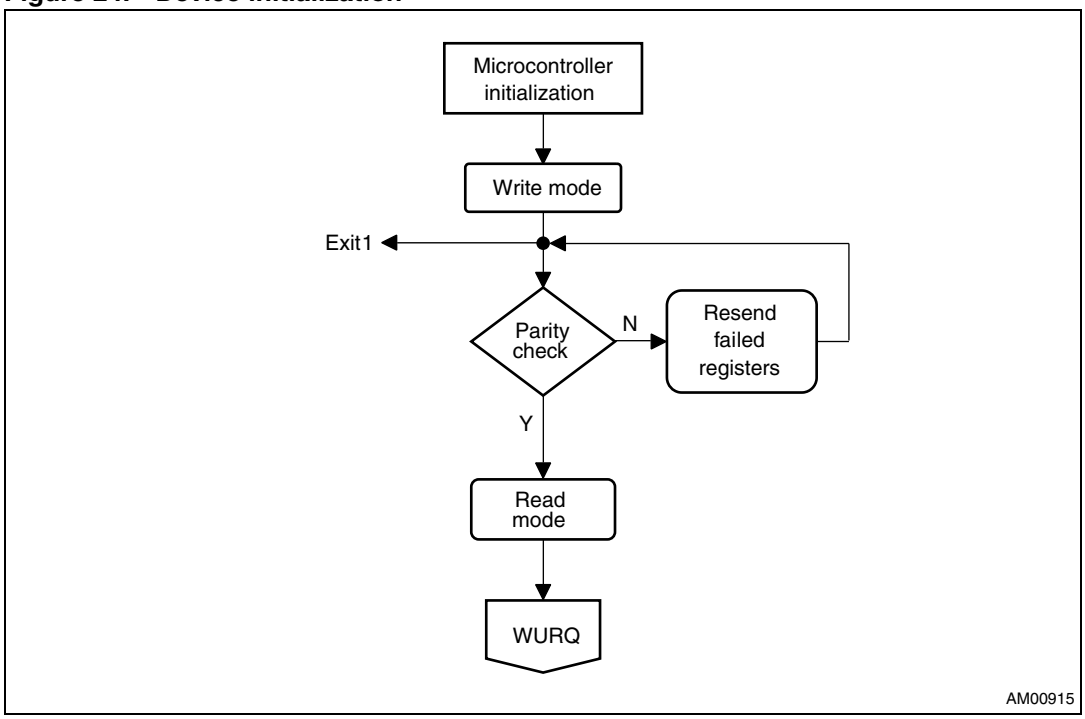
Figure 23. Slow demagnetization waveform. Load connected to GND



6.4 I²C protocol

6.4.1 Protocol configuration

Figure 24. Device initialization



Microcontroller initialization: Microcontroller initialization phase.

Write mode: The L6360 is configured by the microcontroller through I²C.

To configure the device, it is necessary to write its internal registers (see *Write modes* section).

Parity check: L6360 calculates the parity of each received register and stores it in the parity register. After which, it compares it with the parity transmitted together with the data.

If the parity check of one or more registers failed, the “parity error bit” in the status register is set and an interrupt is generated by the L6360.

The microcontroller can now read the status register and the parity register (*current read*). So the microcontroller can understand the interrupt cause and which register failed the transmission. If the parity check is ok, the flow goes on (*Read modes*).

Write register failed: The microcontroller can again write the register(s) that failed the check.

Read mode: Read status register to monitor if the configuration was good (*Read modes*).

6.4.2 Operating modes

Write modes

The L6360 is configured by the microcontroller through I^2C. To configure the device, it is necessary to write its internal registers.

There are two writing modes:

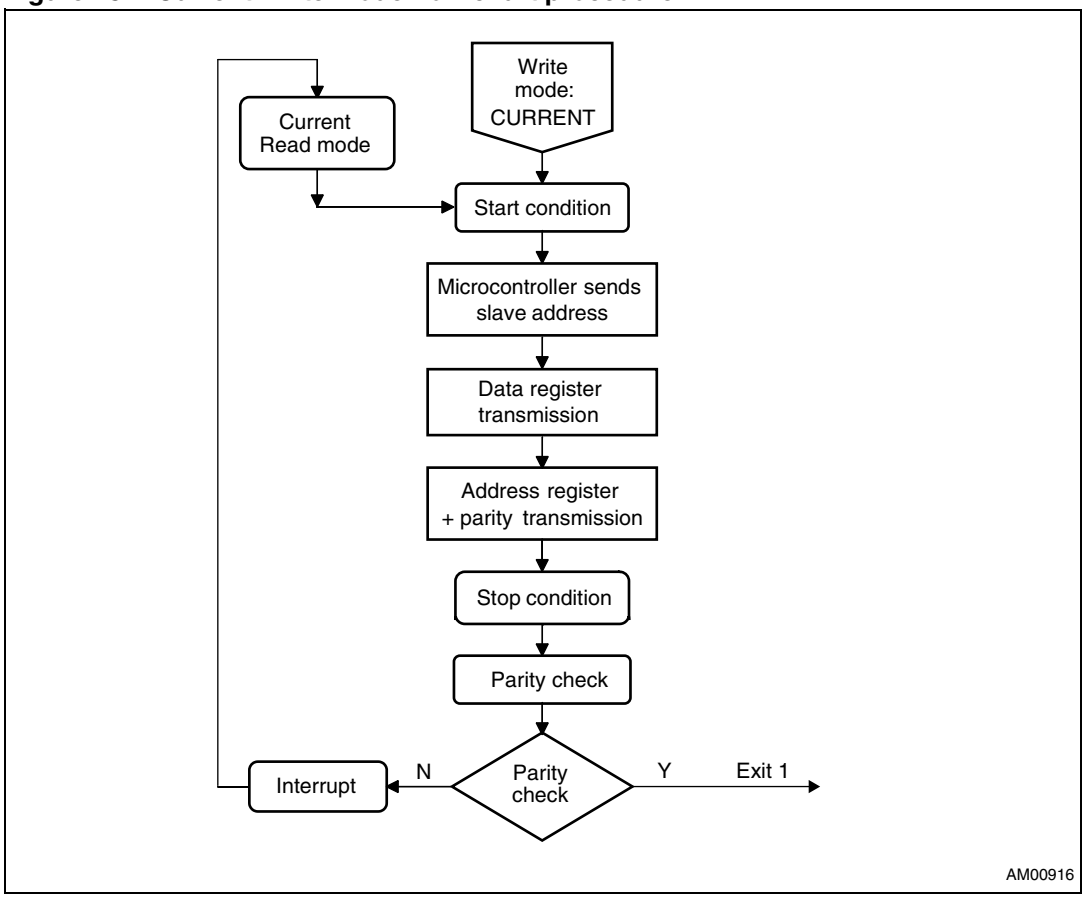
- **Current**: single register
- **Sequential**: all registers in sequence

Current Write mode

The microcontroller I^2C is configured as master transmitter.

The L6360 I^2C is configured as the slave receiver.

Figure 25. Current Write mode flow chart procedure



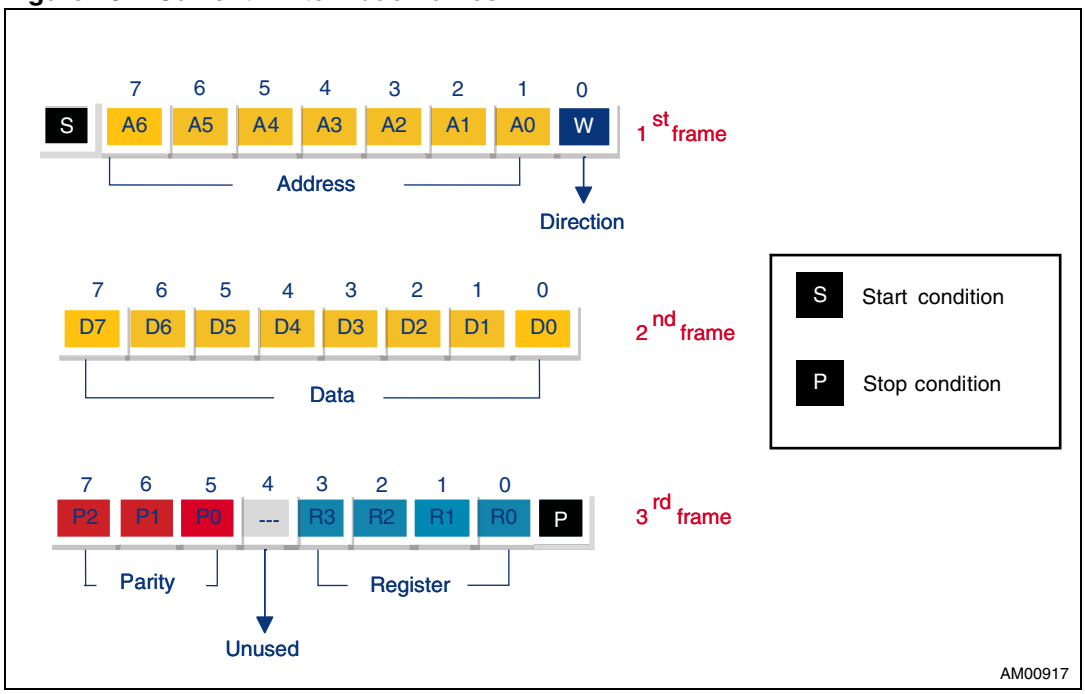
1. Microcontroller I^2C establishes the communication: START condition
2. Microcontroller I^2C sends the slave address on the I^2C bus to check if the slave is online (1^{st} frame)
3. After the address is matched, the microcontroller starts the data transmission: the 2^{nd} frame is the data to be written into the selected register (see *3^{rd} frame*)
4. The 3^{rd} frame is composed of the address of the register to be written and of the parity of the 2^{nd} frame.
5. Microcontroller I^2C finishes the communication: STOP condition
6. The L6360 calculates the parity of the data received
7. The L6360 compares its parity calculation with the parity bits in the 3^{rd} frame (sent by the microcontroller)
8. If the parities match, the protocol flow goes on (exit), otherwise the PE bit inside the L6360 status register is set and the flow goes to the next state.
9. The L6360 generates an interrupt to report the parity check error.
10. The microcontroller sends a read request to the device. The L6360 then sends the status and parity registers. The microcontroller can resend the corrupted data register.
11. Back to step 1.

The I^2C frame (configuration, control, diagnostic phases) must provide:

- Slave address (7 bits)
- Transmission direction (read/write)
- Data (8 bits: data register)
- Parity bits (P2, P1, P0)
- Registers address (4 bits: 16 registers addressable)

The three frames are shown in *Figure 26* and below:

Figure 26. Current Write mode frames



1st frame

Bit 7÷1: L6360 address

Bit 0: Direction

Table 27. Current Write mode direction bit

W bit	Master	Slave
0	Write mode	Read mode
1	Read mode	Write mode

2nd frame

Bit 7÷0: Data register

3rd frame

Bit 7÷5: Parity bits

Bit 4: Unused

Bit 3÷0: Register address

The parity check bits are calculated as shown in *Equation 2*:

Equation 2

$$P0 = D7 \oplus D6 \oplus D5 \oplus D4 \oplus D3 \oplus D2 \oplus D1 \oplus D0$$

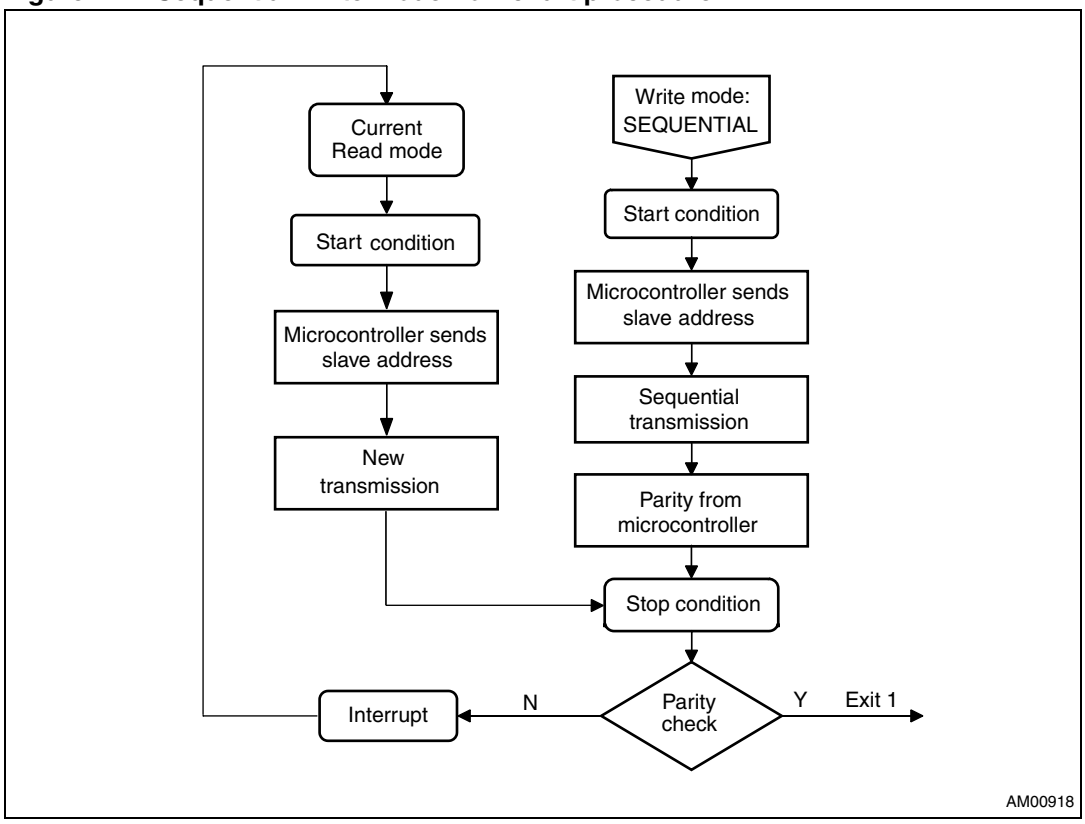
$$P1 = D7 \oplus D5 \oplus D3 \oplus D1 \text{ (odd parity)}$$

$$P2 = D6 \oplus D4 \oplus D2 \oplus D0 \text{ (even parity)}$$

If parity error occurs, the register are not overwritten.

Sequential Write mode

Figure 27. Sequential Write mode flow chart procedure



1. The microcontroller I^2C establishes the communication: START condition.
2. The microcontroller I^2C sends the slave address on the I^2C bus to check if the slave is online (1^{st} frame).
3. After the address is matched, the microcontroller starts the sequential transmission ($2^{nd} \div 8$th frame).
4. The microcontroller sends its parity register (last frame: 9^{th} frame).
5. Microcontroller I^2C finishes the communication: STOP condition.
6. The L6360 calculates the parity of the registers received, and stores the results in the parity register.
7. The L6360 compares its parity register with the parity register sent by the microcontroller (9^{th} frame).
8. If the parities match, the protocol flow goes on (EXIT), otherwise the PE bit inside the L6360 status register is set, and the flow goes to the next state.
9. The L6360 generates an interrupt to report the parity check error.
10. The microcontroller sends a read request to the device. In this phase the L6360 sends the status register and the parity register allowing the microcontroller to verify which register failed the configuration.

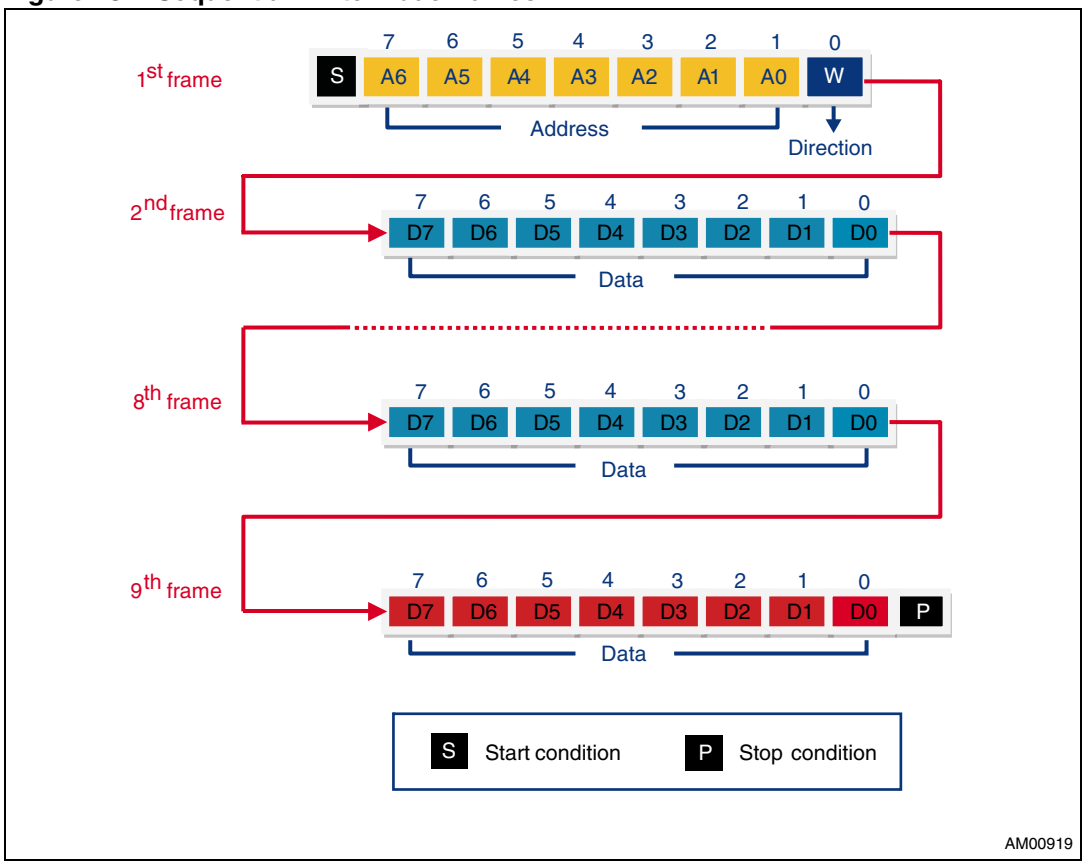
11. Now the microcontroller can perform a new write sequential procedure.
12. Microcontroller I^2C establishes the communication: START condition.
13. Microcontroller I^2C sends the slave address on the I^2C bus to check if the slave is online.
14. The microcontroller resends the data registers.
15. Back to step 5.

The I^2C frame (configuration, control, diagnostic phases) must provide:

- Slave address (7 bits)
- Transmission direction (read/write)
- Data (8 bits: data registers)

The 9 frames are shown below:

Figure 28. Sequential Write mode frames



1st frame

Bit 7÷1: L6360 address

Bit 0: Direction (write/read)

Table 28. Sequential Write mode direction bit

W	Master	Slave
0	Write mode	Read mode
1	Read mode	Write mode

2nd ÷ 8th frame

Bit 7÷0: Data register

9th frame

Bit 7÷0: Microcontroller parity register

The microcontroller parity check (for each register) calculus performed is shown below:

Figure 29. Microcontroller parity check calculus

Bit 6 = **P6**: *Microcontroller configuration register parity*

This bit is the parity of the configuration register.

Bit 5 = **P5**: *Microcontroller control register 1 parity*

This bit is the parity of control register 1.

Bit 4 = **P4**: *Microcontroller control register 2 parity*

This bit is the parity of control register 2.

Bit 3 = **P3**: *Microcontroller LED1 register high parity*

This bit is the parity of the LED1 MSB register (15 down to 8).

Bit 2 = **P2**: *Microcontroller LED1 register low parity*

This bit is the parity of the LED1 LSB register (7 down to 0).

Bit 1 = **P1**: *Microcontroller LED2 register high parity*

This bit is the parity of the LED2 MSB register high (15 down to 8).

Bit 0 = **P0**: *Microcontroller LED2 register low parity*

This bit is the parity of the LED2 LSB register high (7 down to 0).

For each register, a parity check is calculated as shown in *Equation 3*, in general formulas:

Equation 3

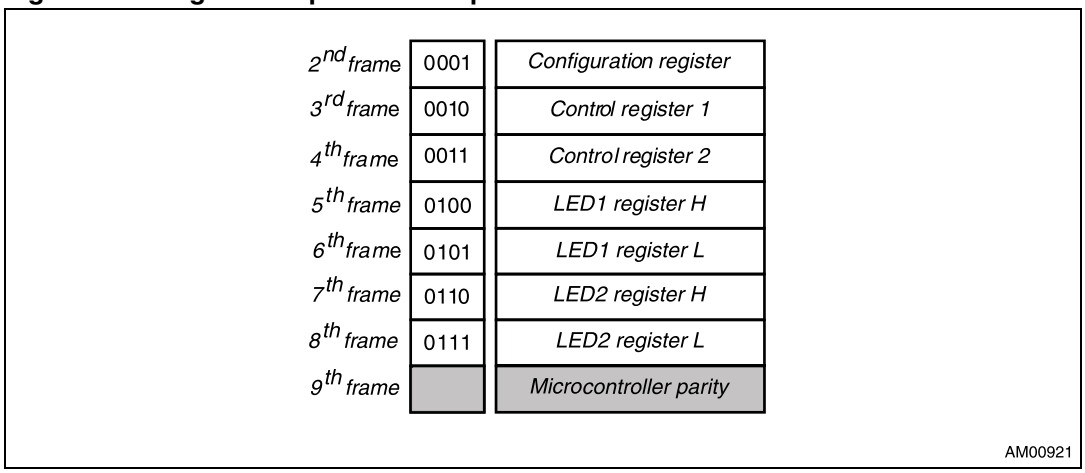
$$PX = D7 \oplus D6 \oplus D5 \oplus D4 \oplus D3 \oplus D2 \oplus D1 \oplus D0 \ (X = 0 \text{ to } 6)$$

D7 ÷ D0 indicates bits inside each register.

If parity error occurs, the registers are not overwritten.

In this writing mode, all writable registers and the microcontroller parity register are sent.

Figure 30. Register sequence in sequential Write mode



Read modes

The status register and parity check register are read only.

The other registers are readable/writable (by microcontroller).

There are three reading modes:

- **Current**: status register only
- **Sequential**: all registers in sequence
- **Random**: to read registers in sequence starting from a register address fixed by the microcontroller.

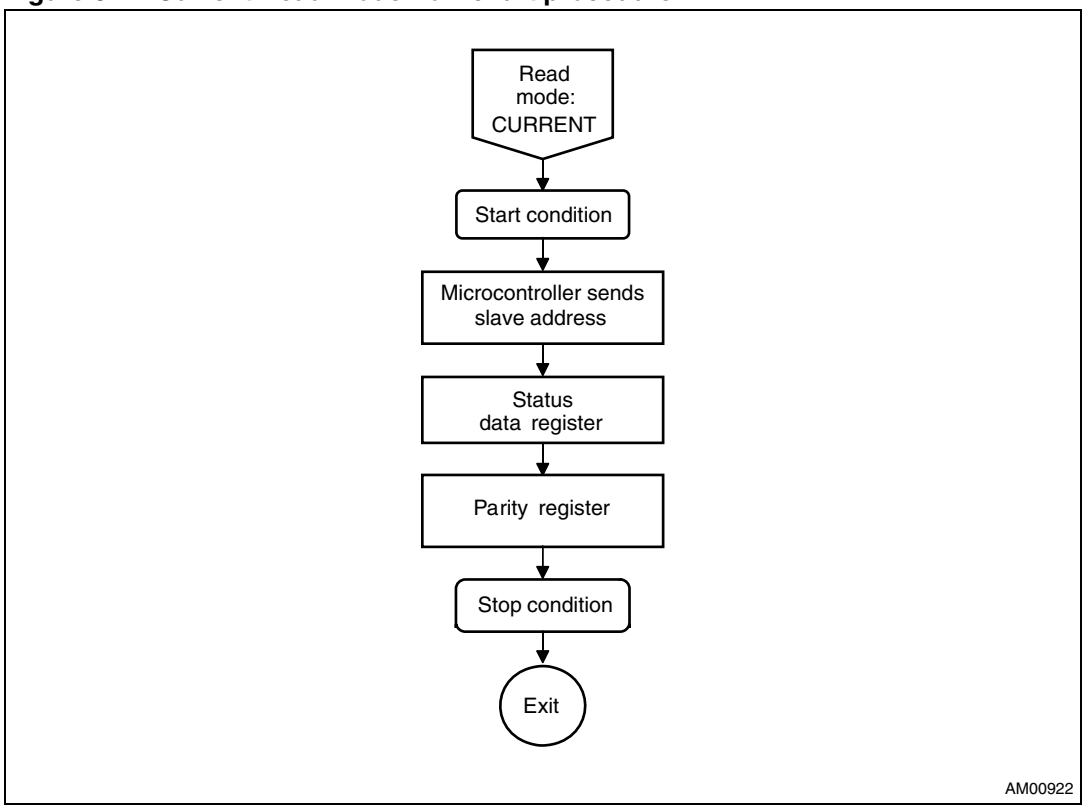
All registers are addressed as shown in *Table 30*:

Table 29. Read mode: register address

Address	Register name
0000	Status register
0001	Configuration register
0010	Control register 1
0011	Control register 2
0100	LED1 register MSB
0101	LED1 register LSB
0110	LED2 register MSB
0111	LED2 register LSB
1000	Parity register

Current Read mode

Figure 31. Current Read mode flow chart procedure



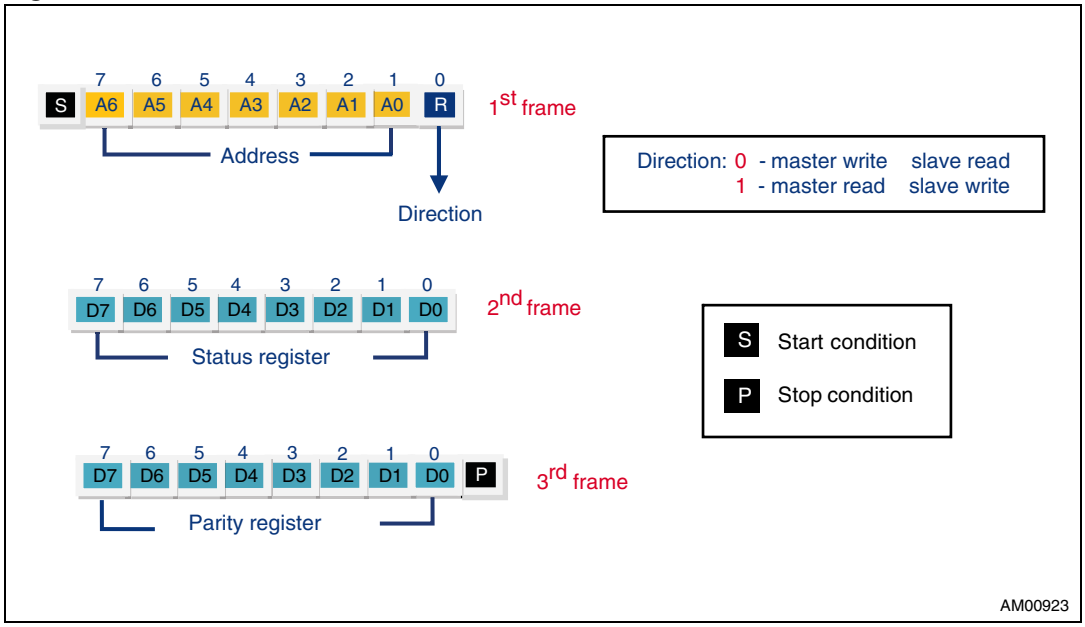
1. Microcontroller I^2C establishes the communication: START condition
2. Microcontroller I^2C sends slave address on the I^2C bus to check if the slave is online (1^{st} frame)
3. After the address is matched, the L6360 sends its status register (2^{nd} frame)
4. The L6360 sends its parity register (3^{rd} frame)
5. Microcontroller I^2C finishes the communication: STOP condition.

The I^2C frame (configuration, control, diagnostic phases) must provide:

- *Slave address (7 bits)*
- *Transmission direction (read/write)*
- *Data (8-bit data registers): status and parity registers.*

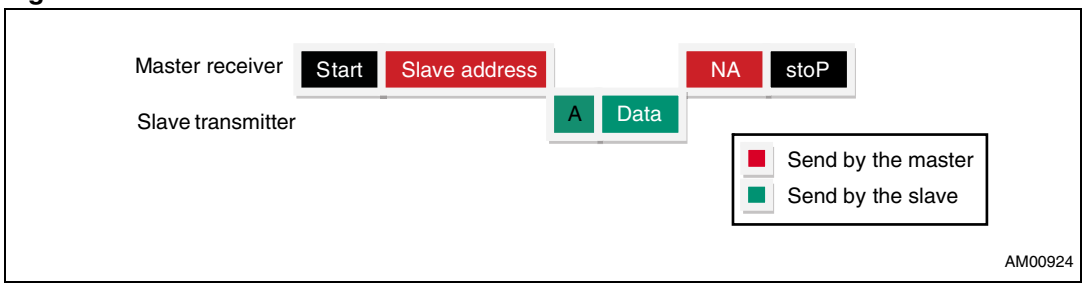
The three frames are shown in *Figure 32*.

Figure 32. Current Read mode frames



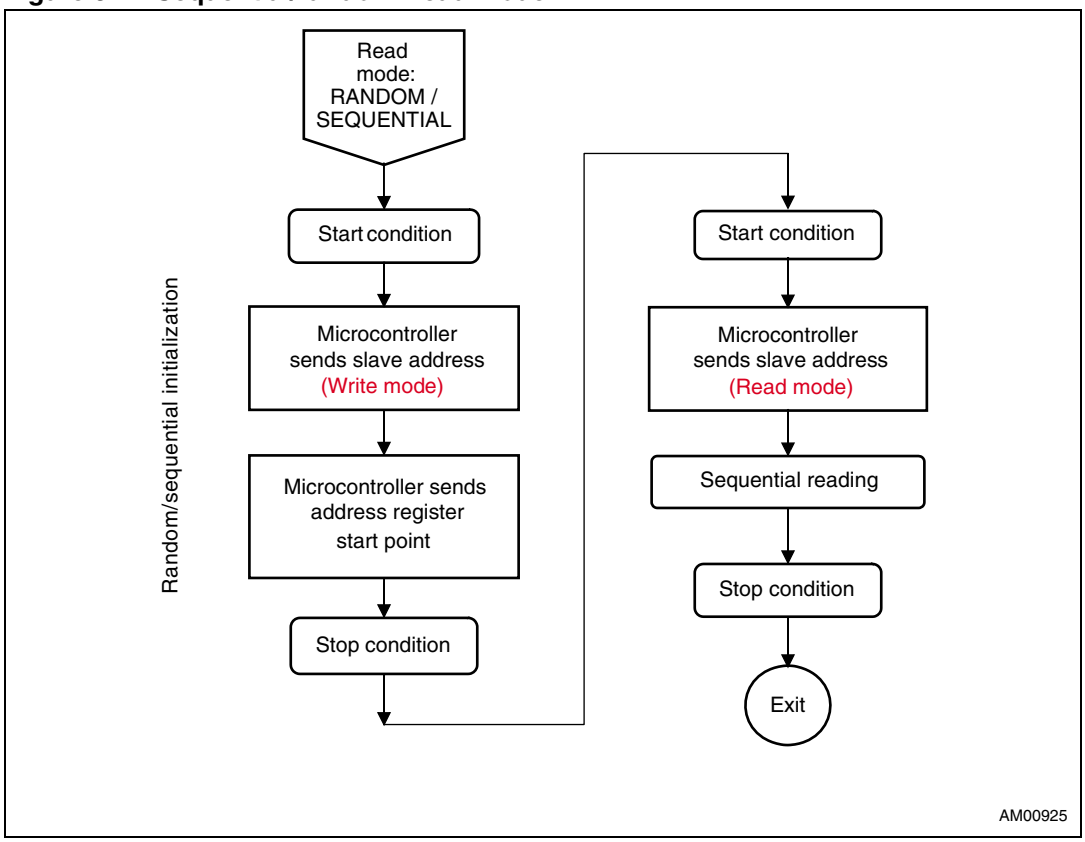
When a “read request” comes from the microcontroller (it is configured as master receiver), the IC (slave transmitter) sends the contents of the status and parity registers.

Figure 33. Current Read communication flow



Sequential/random Read modes

Figure 34. Sequential/random Read mode



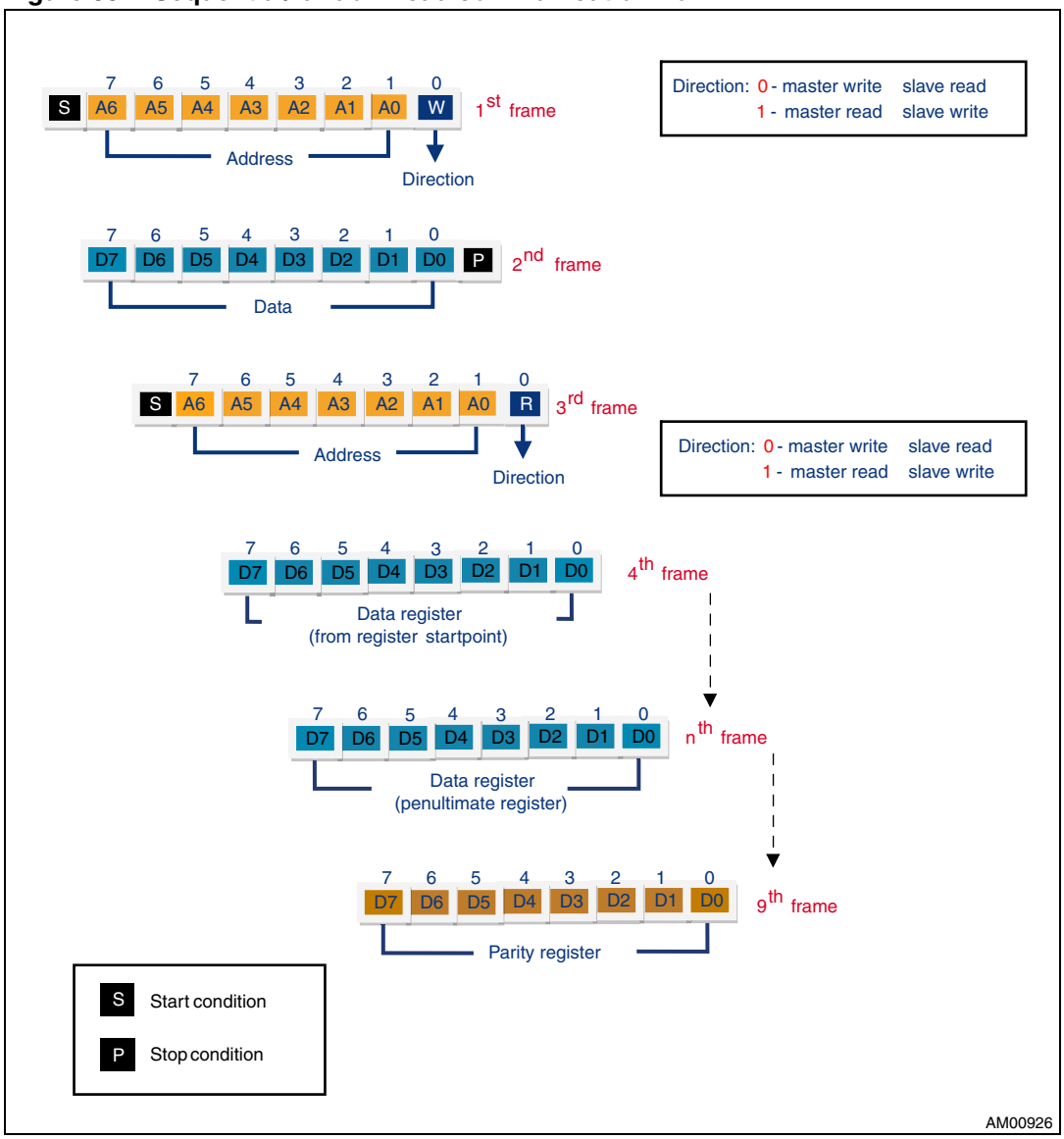
1. Random/sequential Read mode initialization: Microcontroller I^2C establishes the communication: START condition.
2. Microcontroller I^2C sends the slave address, in Write mode, on the I^2C bus to check if the slave is online (1^{st} frame).
3. Microcontroller I^2C sends the register address start point, which sets the first register to read in sequence (2^{nd} frame).
4. Microcontroller I^2C finishes the communication: STOP condition.
5. Microcontroller I^2C sends the slave address, in Read mode, on the I^2C bus to check if the slave is online (3^{rd} frame).
6. After the address is matched, the L6360 sends its registers in sequential mode, starting from the register set in the 2^{nd} frame.
7. Microcontroller I^2C finishes the communication: STOP condition.

The I^2C frame (configuration, control, diagnostic phases) must provide:

- *Slave address (7 bits)*
- *Transmission direction (read/write)*
- *Data (8-bit data register)*

The frames structure is shown in *Figure 35*:

Figure 35. Sequential/random read communication flow



1st frame

Bit 7 ÷ 1: L6360 address

Bit 0: Direction (write)

2nd frame

Bit 7 ÷ 0: Address register starting point

Table 30. Address register

Address	Register name
0000	Status register
0001	Configuration register
0010	Control register 1
0011	Control register 2
0100	LED1 register MSB
0101	LED1 register LSB
0110	LED2 register MSB
0111	LED2 register LSB
1000	Parity register

3rd frame

Bit 7 ÷ 1: L6360 address

Bit 0: Direction (read)

4th÷ n th frame

Bit 7÷0: Data register (from address register starting point to penultimate address register)

9th frame

Bit 7÷0: Parity register (the last register)

7 Physical layer communication

The IC transfers the data received (on the $IN_{C/Q}$ digital input pin) at the C/Q_O output. The $EN_{C/Q}$ pin allows the C/Q_O line to be put into TRISTATE.

Data received from the line (C/Q_I and I/Q pins) is transferred to the digital output pins $OUT_{C/Q}$ and $OUT_{I/Q}$.

Figure 36. Block diagram communication mode

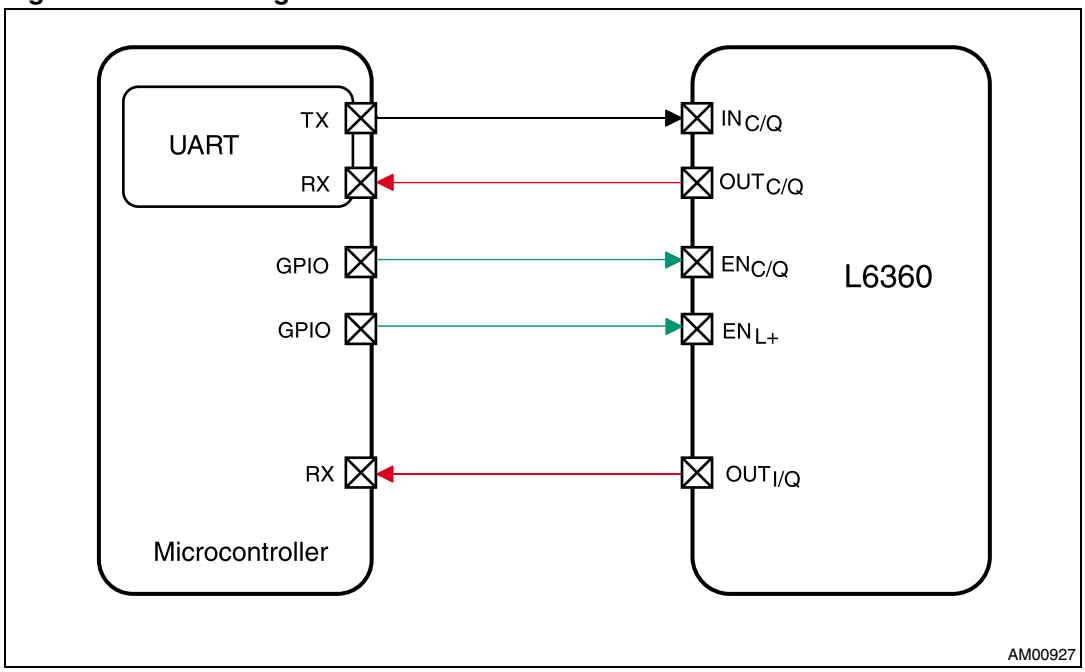
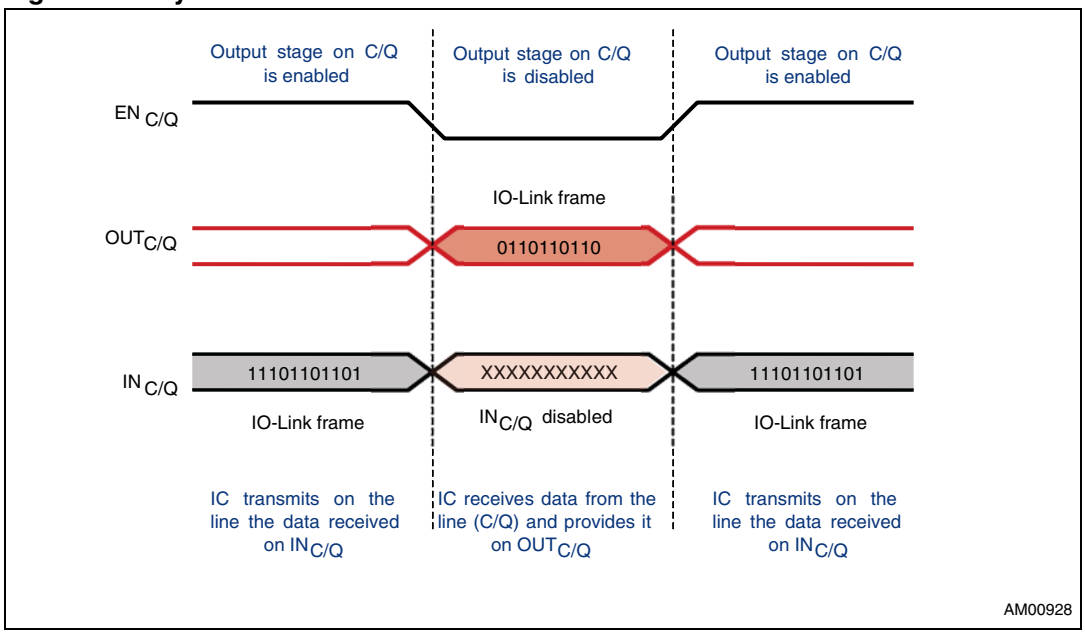


Figure 37. System communication mode



7.1 Transceiver

Output drivers (C/Q_O and L+) are protected against short-circuit or overcurrent by means of two different functions.

One is the current limiting function: output current is linearly limited to $I_{LIMQ/L}$.

The cutoff protection, on the other side, is intended to turn off the drivers when the output current exceeds a (programmable for the C/Q_O driver) threshold ($I_{COL/I}$). When the current reaches the (programmed) cutoff value the channel output driver is turned off after a programmable delay ($t_{dcoq/I}$). The channel output driver automatically restarts again after a programmable delay time ($t_{rcoq/I}$). See *Figure 38*.

Figure 38. C/Q or L+ channel cutoff protection

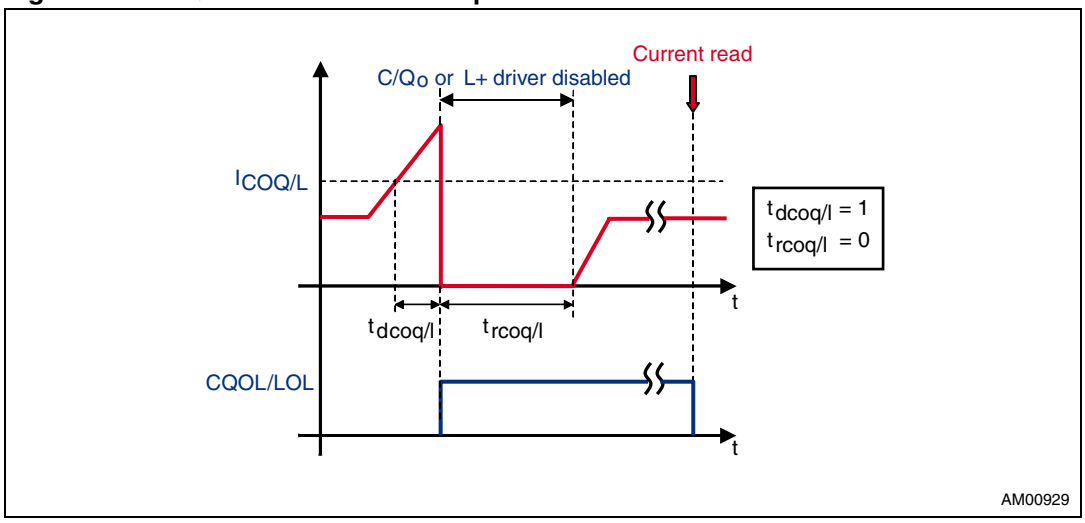
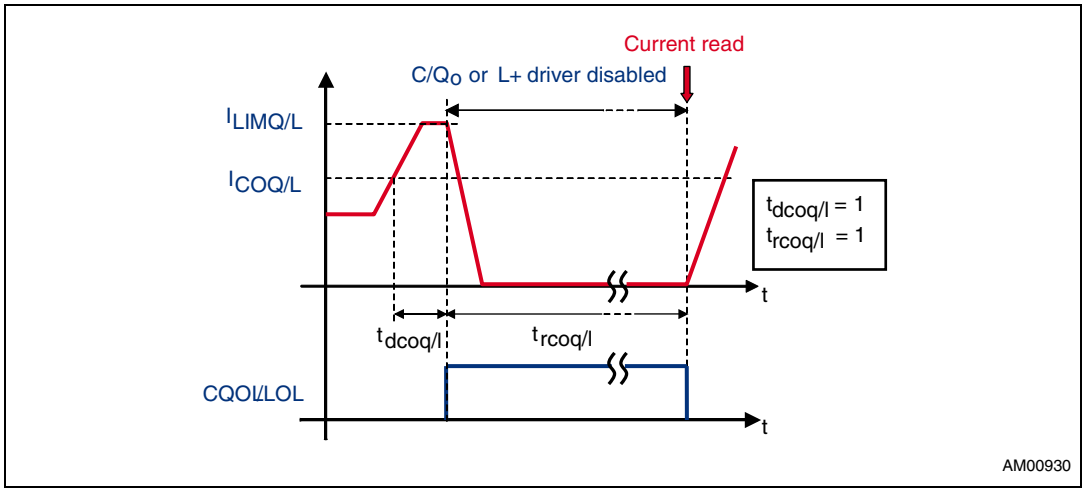


Figure 39. C/Q or L+ channel current limitation and cutoff protection with latched restart



For CQOL/LOL bit reset see the related *Status register* section.

7.2 IEC 61131-2 type 1 digital inputs

Two IEC61131-2 type 1 inputs are provided: one is available on C/Q_I (as per IO-Link specification to support SIO mode) and one on the I/Q pin.

Both are provided with a programmable de-bounce filter (t_{dbq} and t_{dbi}, see *Table 17* and *Table 23*) to prevent false triggering.

8 Diagnostic LED sequence generator and driver

Each LED indication block can drive, through open drain output, one external LED.

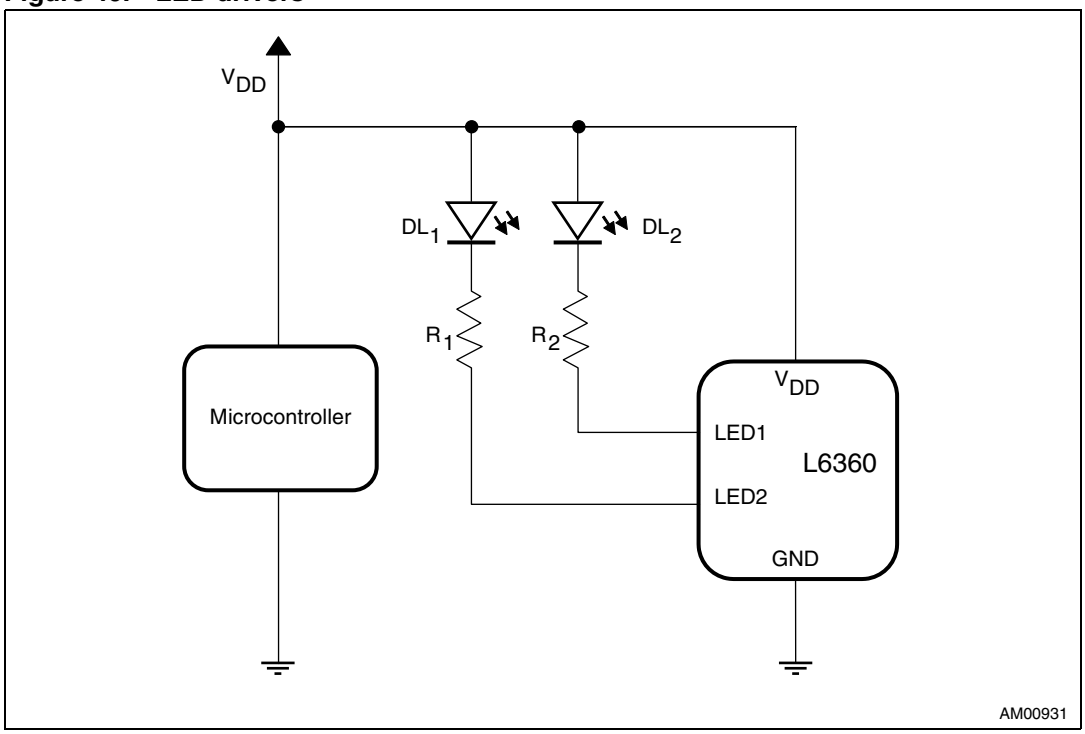
LED drivers can be used for status or diagnostic information, or for other purposes, and should be configured by the host microcontroller.

Two sequences of 16 bits can be programmed (through I^2C) to generate user specific sequences; each LED driver has two associated registers and turns the external LED on or off according to the information stored in the registers, which are scanned at a rate of 63 ms per bit; total sequence time of each LED is approximately 1 s.

See also the *LED registers* section.

Figure 40 shows how to wire up the two LEDs:

Figure 40. LED drivers



9 Linear regulator

The L6360 embeds a linear regulator with output voltage selectable (by the SEL pin) at 3.3 V or 5 V.

The input voltage is V_H (see *Table 3*) and the maximum power dissipation is 200 mW.

The linear regulator minimum limitation current value is I_{LIMLR} (see *Table 7*).

Figure 41. Linear regulator

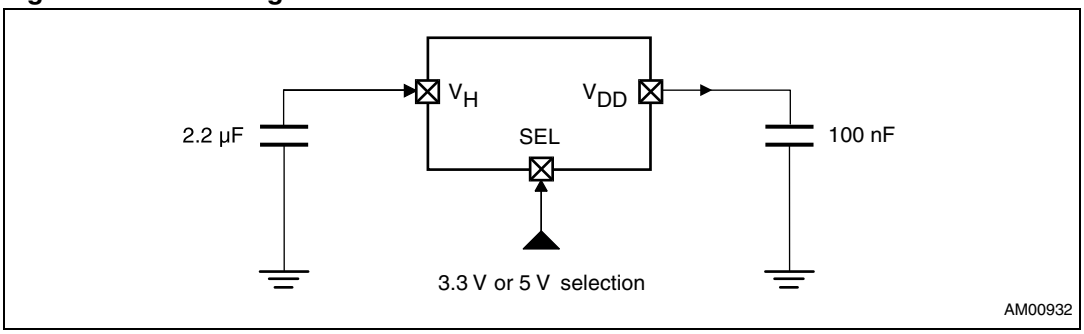


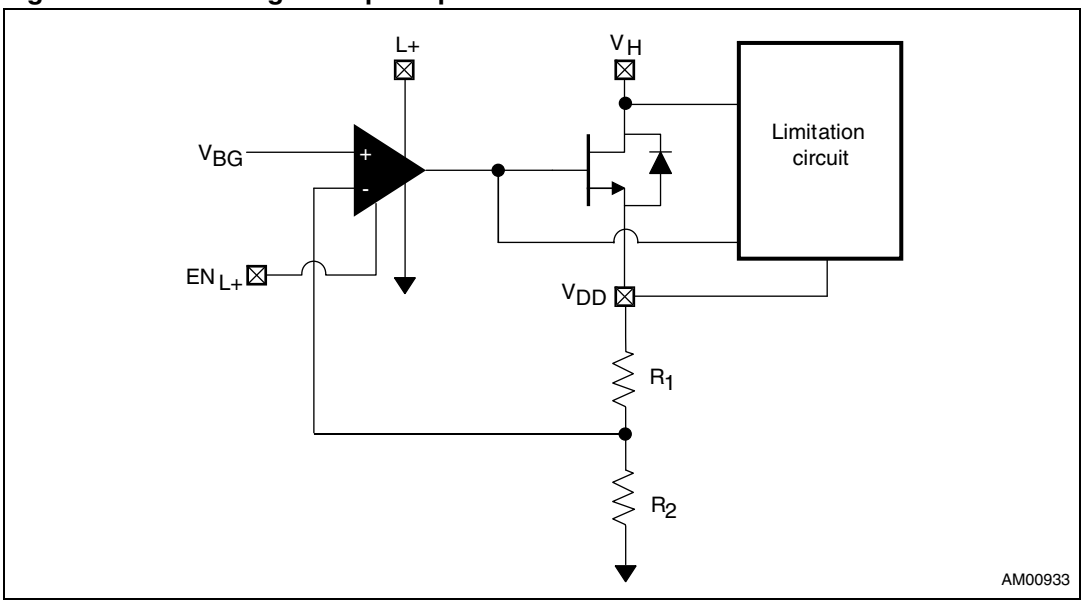
Table 31. Linear regulator selection pin

SEL	V_{DD}
0	5 V ± 2.5%
1	3.3 V ± 2%

The linear regulator cannot be turned off as it is necessary to supply (through V_{DD} pin) internal circuitries.

It can also be used to supply external circuitry (e.g. the microcontroller).

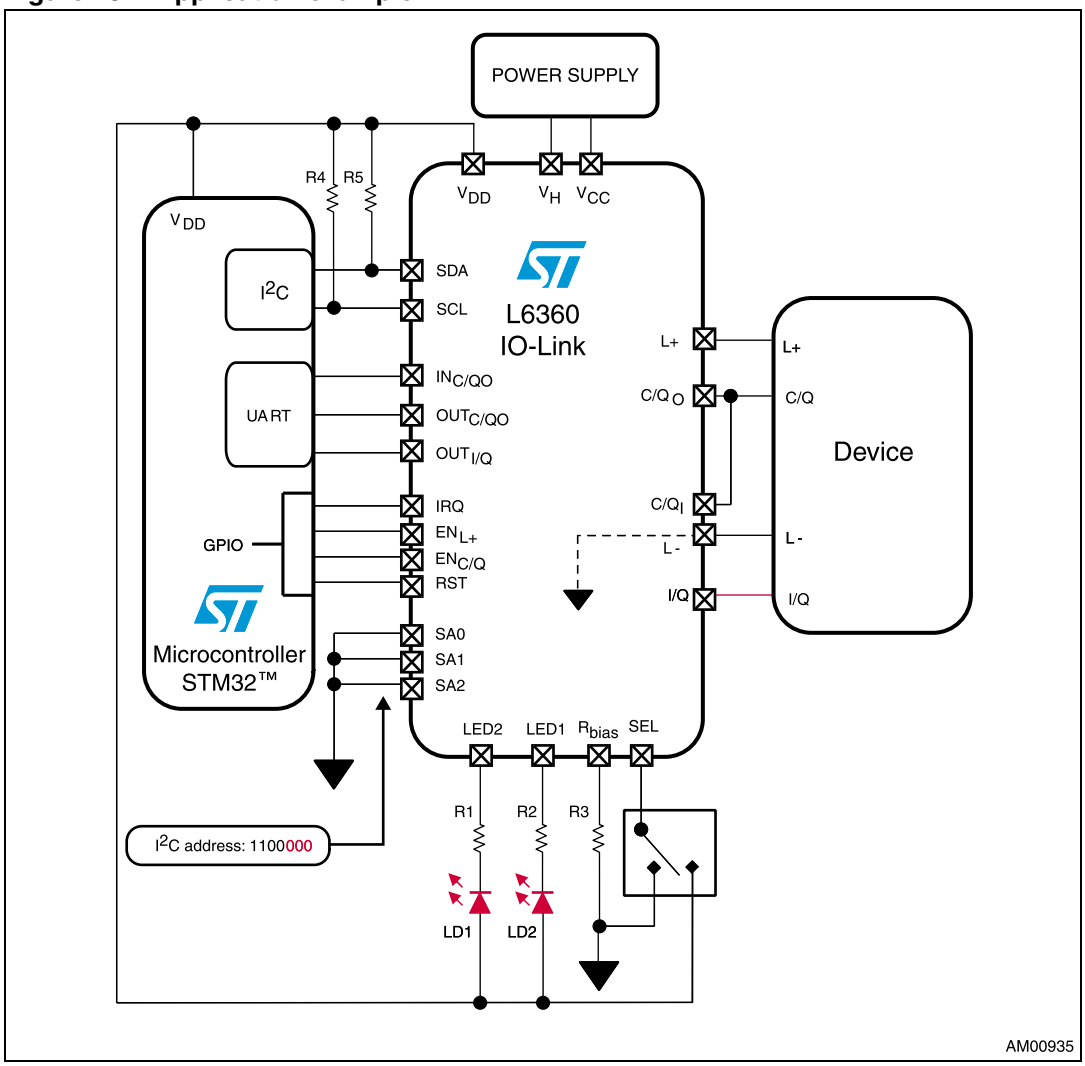
Figure 42. Linear regulator principle schematic



10 Application example

The IO-Link master system typically consists of a microcontroller and physical layer and it communicates with an IO-Link device. The principle connection can be seen in *Figure 43*.

Figure 43. Application example



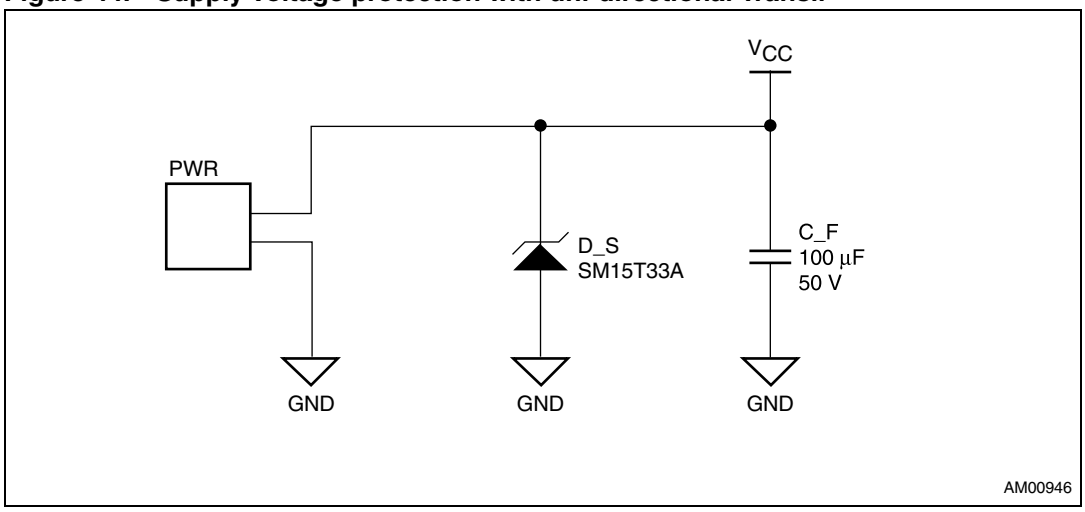
11 EMC protection considerations

Depending on final product use and environmental conditions, the master application may require additional protection.

11.1 Supply voltage protection

In order to avoid overvoltages on a system supply, a voltage suppressor such as Transil™ can be added. A simple protection diagram example is shown in *Figure 44*.

Figure 44. Supply voltage protection with uni-directional Transil



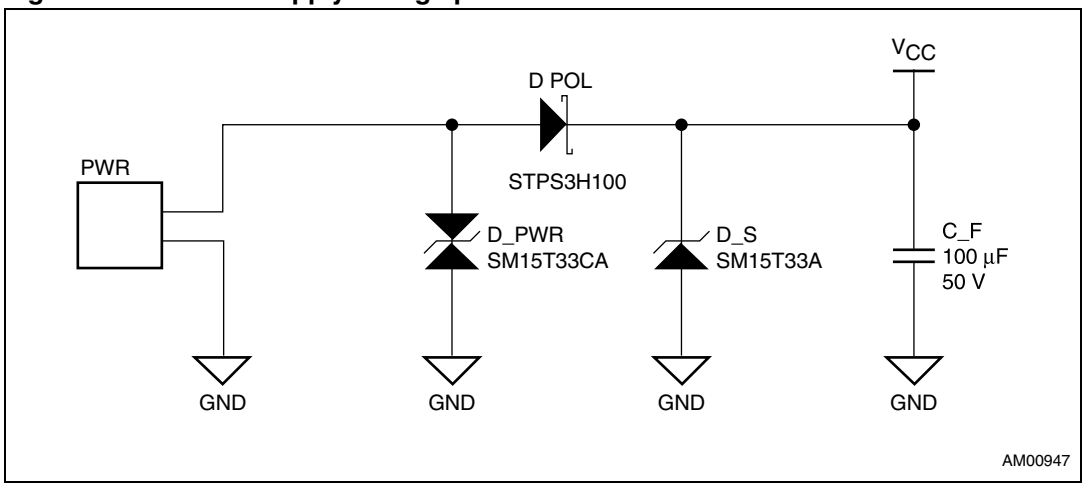
Performance of the above mentioned example is limited and does not include reverse polarity protection. It is just a cost-effective solution.

Table 32. Supply voltage protection component description

Part	Function	Description
D_S	Supply overvoltage protection	Works as a primary overvoltage clamp to limit supply line distortions - like surge pulses, oscillations caused by line parasitic parameters (inductance) during plug-in phase, etc. 1500 W is recommended to provide reliable protection, uni-directional type helps to avoid negative stress of the L6360.
C_F	Filtering bulk capacitor	An energy buffer for application supply, filters the application supply to avoid high ripple during power driver switching, etc.

A more sophisticated solution can be seen in *Figure 45*.

Figure 45. Refined supply voltage protection



The above reference diagram provides an extended level of protection in both polarities as well as the reverse polarity protection.

Table 33. Refined supply voltage protection component description

Part	Function	Description
D_PWR	Primary overvoltage protection	Works as a primary overvoltage clamp to limit supply line distortions - like surge pulses, oscillations caused by line parasitic parameters (inductance) during plug-in phase, etc. 1500 W is recommended to provide reliable protection, uni-directional type is chosen to cover reverse polarity protection.
D_POL	Reverse polarity protection	Avoids reverse direction current flow and negative voltage stress of the L6360. Its current rating (3 A) is chosen in accordance with the maximum driving capabilities of the L6360 power stages. Schottky type is recommended to limit power dissipation (low VF). Voltage rating (100 V) comes from negative surge to the supply condition.
D_S	D_PWR support and IO overvoltage protection	a) Shares a positive surge current with the primary protection and limits the overvoltage amplitude. b) clamps surges applied to the L6360 C/Q and L+ lines.
C_F	Filtering bulk capacitor	An energy buffer for application supply, filters the application supply to avoid high ripple during power driver switching, etc.

If the V_H pin of the L6360 is supplied from a separate power supply or if it is decoupled from the main power supply and blocked by bulk capacitors, an additional circuit may be required to ensure the V_H voltage is always lower than (or equal to) the main supply voltage (V_{CC}). A possible solution with diode is shown in *Figure 46*.

Figure 46. V_H protection vs. V_{CC}

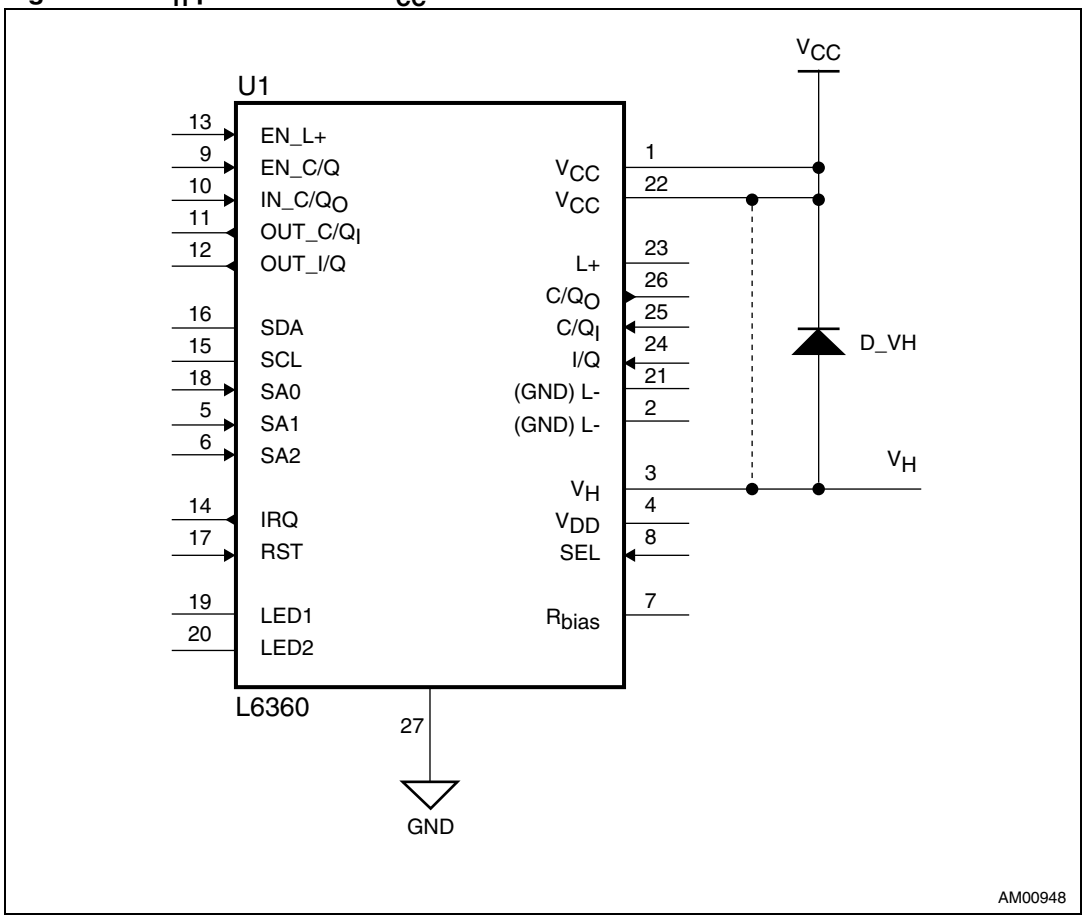


Table 34. V_H protection component description

Part	Function	Description
D_VH	VH overvoltage protection	V_H voltage must be always lower than (or equal to) V_{CC}. Even during the powering-up and down of an application. This fact must be taken into consideration if V_H is supplied from another source (V_{CC} and V_H not connected together), charged capacitors, etc. In some cases a diode placed between V_{CC} and V_H may help to avoid this violation.

11.2 I/O lines protection

Figure 47 shows external components (capacitors) suitable for IO-Link communication - protection level in accordance with specification.

Figure 47. Typical protection in IO-Link applications

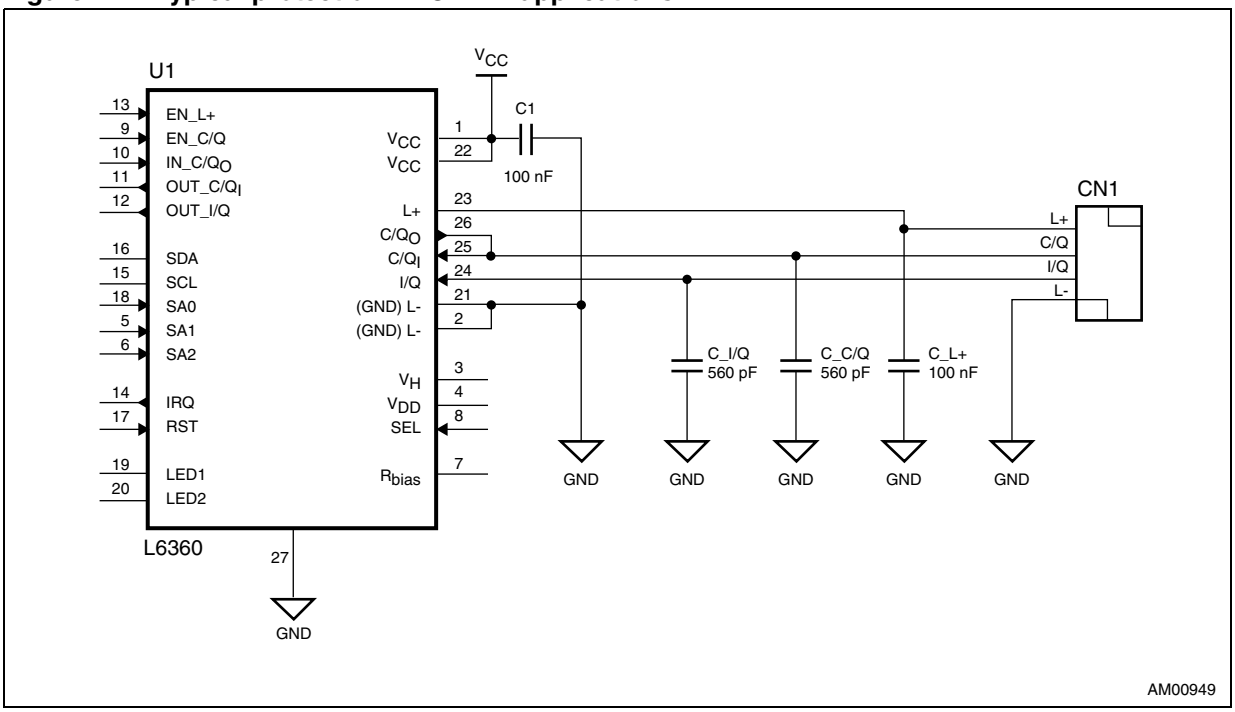


Table 35. Typical protection in IO-Link application component description

Part	Function	Description
C_1	Power supply blocking	Energy buffer for the L6360 supply, makes chip supply voltage stable, limits EMI noise.
C_I/Q, C_C/Q, C_L+	Filtration capacitors	Work as a basic protection against fast transient signals like burst or radio-frequency domain applied to the lines. Limit voltage spikes frequency spectrum and amplitude.

If an extended protection level is required, the solution seen in *Figure 48* is recommended. It provides robust protection according to IEC61131-2. It is suitable for IO-Link communication and is backward compatible with SIO (standard I/O). It protects the L6360 application against high energy surge pulses according to the IEC61000-4-5 standard. All the lines are protected against ±2.5 kV surge pulse amplitude in common mode and ±1 kV in differential mode considering 42 Ω/0.5 µF generator coupling.

Figure 48. IO-Link and SIO application extended protection

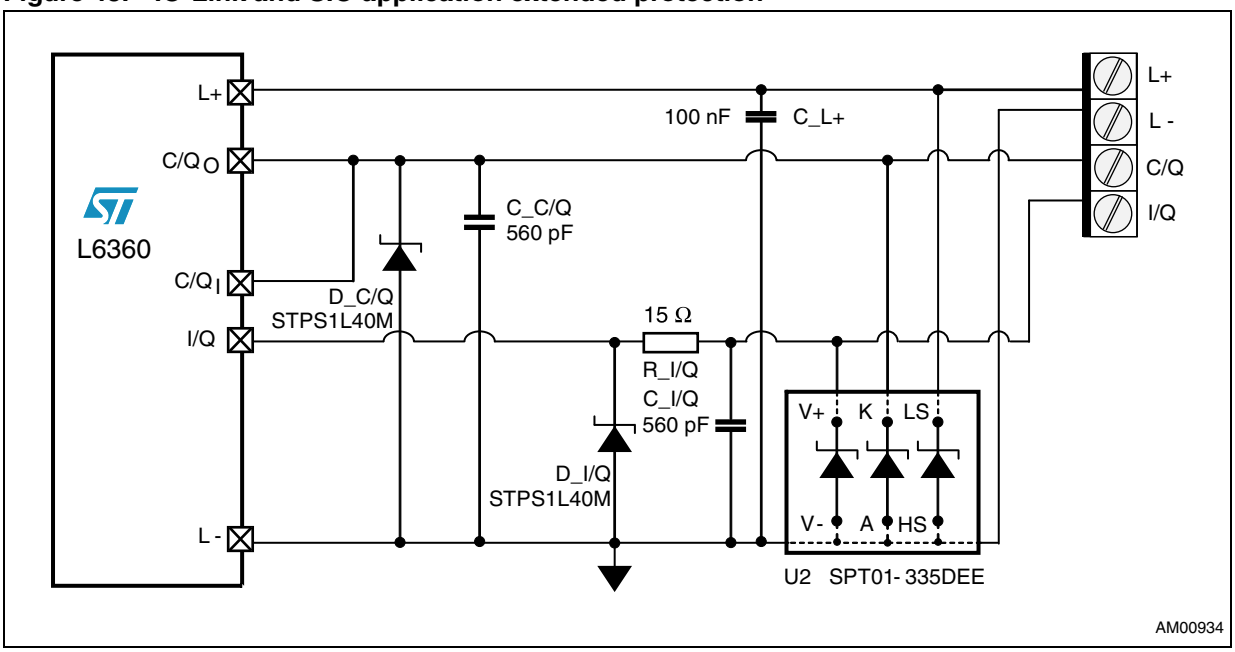


Table 36. IO-Link and SIO applications extended protection component description

Part	Function	Description
C_I/Q, C_C/Q, C_L+	Filtration capacitors	Work as a basic protection against fast transient signals like burst or radio-frequency domain applied to the lines. Limit voltage spike frequency spectrum and amplitude.
D_I/Q, D_C/Q	Negative voltage spike suppression	Schottky diodes with low VF clamp the disturbance applied to the lines in a reverse polarity direction. Capable of conducting high surge current pulses to avoid high peak current flow through L6360 pins.
R_I/Q	Surge current limitation	Reduces the current flow in the L6360 - the I/Q pin in both polarities when e.g. surge noise is applied to the line. If this resistor is omitted, the I/Q line surge immunity is lower.
U2 (SPT01-335DEE)	Overvoltage protection	Primary surge protection to avoid overvoltage on the L6360 interface. Protects L+ switch against negative voltage pulses. Shares current flow of negative surge pulses with the additional Schottky diodes on C/Q and I/Q lines. Clamps positive surge pulse amplitude applied to I/Q line.

12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK®2 packages, depending on their level of environmental compliance. ECOPACK2 specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK2 is an ST trademark.

Figure 49. Package outline for VFQFPN - 26-lead 3.5 x 5 x 1 mm - 0.50 pitch

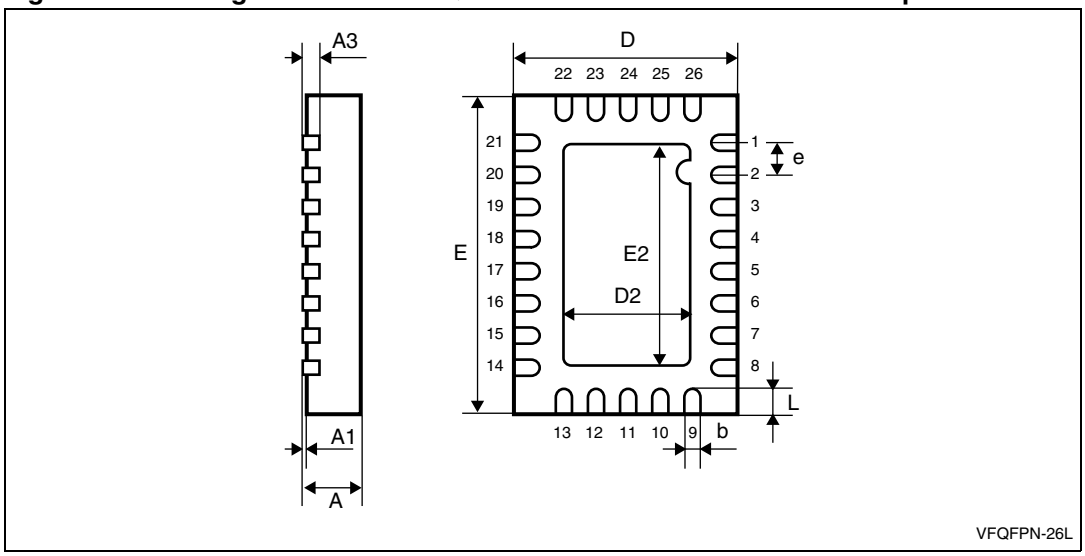


Table 37. Mechanical data for VFQFPN - 26-lead 3.5 x 5 x 1 mm - 0.50 pitch(1) (2) (3)

Symbol	Dimensions		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2		0.20	
b	0.18	0.25	0.30
D		3.50	
D2	1.90	2.00	2.10
E		5.00	
E2	3.40	3.50	3.60
e		0.50	
L	0.30	0.40	0.50

1. VFQFPN stands for thermally enhanced “very thin fine pitch quad flat package no lead”.
2. Very thin profile: 0.80 < A ≤ 1.00 mm.
3. All dimensions are in millimeters.

13 Revision history

Table 38. Document revision history

Date	Revision	Changes
12-Mar-2012	1	Initial release.
15-Mar-2012	2	Updated E_{load} definition in *Table 3: Absolute maximum ratings*. Updated *Figure 36: Block diagram communication mode*.
25-Jan-2013	3	Updated *Table 4: Recommended operating conditions*.

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