STE2002S

81 X 128 SINGLE CHIP LCD CONTROLLER / DRIVER

1 FEATURES

- 88 x 128 bits Display Data RAM
- Programmable MUX rate
- Programmable Frame Rate
- X,Y Programmable Carriage Return
- Dual Partial Display Mode
- Row by Row Scrolling
- Automatic data RAM Blanking procedure
- Selectable Input Interface:
  - I^2C Bus Fast and Hs-mode (read and write)
  - Parallel Interface (read and write)
  - Serial Interface (read and write)
- Fully Integrated Oscillator requires no external components
- CMOS Compatible Inputs
- Fully Integrated Configurable LCD bias voltage generator with:
  - Selectable multiplication factor (up to 6X)
  - Effective sensing for High Precision Output
  - Eight selectable temperature compensation coefficients
- Designed for chip-on-glass (COG) applications
- Low Power Consumption, suitable for battery operated systems
- Logic Supply Voltage range from 1.7 to 3.6V
- High Voltage Generator Supply Voltage range from 2.4 to 4.2V
- Display Supply Voltage range from 4.5 to 13V
- Backward Compatibility with STE2001

2 DESCRIPTION

The STE2002S is a low power CMOS LCD controller driver. Designed to drive a 81 rows by 128 columns graphic display, provides all necessary functions in a single chip, including on-chip LCD supply and bias voltages generators, resulting in a minimum of externals components and in a very low power consumption. The STE2002S features three standard interfaces (Serial, Parallel & I^2C) for ease of interfacing with the host mcontroller

Table 1. Order codes.

Part Numbers	Type
STE2002SDIE1	Bumped Wafers
STE2002SDIE2	Bumped Dice on Waffle Pack

Figure 1. Block Diagram

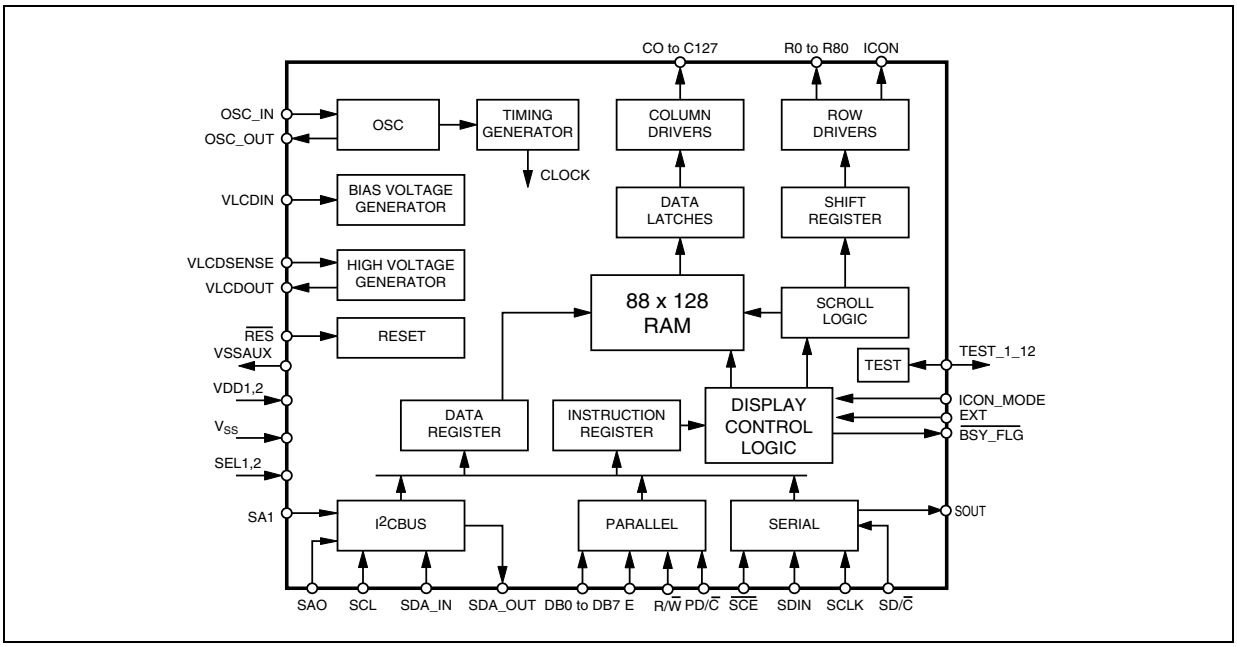


Table of Contents

3 PIN DESCRIPTION

Table 2. Pin Description

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td>R0 to R80</td><td>130-169
288-248</td><td>O</td><td>LCD Row Driver Output</td></tr>
<tr><td>ICON</td><td>129</td><td>O</td><td>ICON Row Driver</td></tr>
<tr><td>C0 to C127</td><td>128-1</td><td>O</td><td>LCD Column Driver Output</td></tr>
<tr><td>VSS</td><td>186-195</td><td>GND</td><td>Ground pads.</td></tr>
<tr><td>VDD1</td><td>226-231</td><td>Supply</td><td>IC Positive Power Supply</td></tr>
<tr><td>VDD2</td><td>220-225</td><td>Supply</td><td>Internal Generator Supply Voltages.</td></tr>
<tr><td>VLCDIN</td><td>176-180</td><td>Supply</td><td>LCD Supply Voltages for the Column and Row Output Drivers.</td></tr>
<tr><td>VLCDOUT</td><td>170-174</td><td>Supply</td><td>Voltage Multiplier Output</td></tr>
<tr><td>VLCDSENSE</td><td>175</td><td>Supply</td><td>Voltage Multiplier Regulation Input. V_{LCDOUT} Sensing for Output Voltage Fine Tuning</td></tr>
<tr><td>V_{SSAUX}</td><td>200, 213, 239</td><td>O</td><td>Ground Reference for Selection Pins Configuration</td></tr>
<tr><td>SEL1,2</td><td>234,235</td><td>I</td><td>Interface Mode Selection</td></tr>
<tr><td>EXT_SET</td><td>236</td><td>I</td><td>Extended Instruction Set Selection
<table>
<tr><th>EXT PAD CONFIG</th><th>INSTRUCTION SET SELECTED</th></tr>
<tr><td>VSS or VSSAUX</td><td>BASIC</td></tr>
<tr><td>VDD1</td><td>EXTENDED</td></tr>
</table></td></tr>
<tr><td>ICON_MODE</td><td>233</td><td>I</td><td>ICON ROW Management
<table>
<tr><th>ICON MODE PAD CONFIG</th><th>ICON MODE STATUS</th></tr>
<tr><td>VSS or VSSAUX</td><td>DISABLED</td></tr>
<tr><td>VDD1</td><td>ENABLED</td></tr>
</table></td></tr>
<tr><td>SDA_IN</td><td>197</td><td>I</td><td>I^2C Bus Data In</td></tr>
<tr><td>SDA_OUT1,2</td><td>198,199</td><td>O</td><td>I^2C Bus Data Out</td></tr>
<tr><td>SCL</td><td>196</td><td>I</td><td>I^2C bus Clock</td></tr>
<tr><td>SA0</td><td>237</td><td>I</td><td>I^2C Slave Address BIT 0</td></tr>
<tr><td>SA1</td><td>238</td><td>I</td><td>I^2C Slave Address BIT 1</td></tr>
<tr><td>OSCIN</td><td>232</td><td>I</td><td>External Oscillator Input</td></tr>
<tr><td>OSCOUT</td><td>181</td><td>O</td><td>Internal/External Oscillator Out</td></tr>
<tr><td>$\overline{RES}$</td><td>201</td><td>I</td><td>Reset Input. Active Low.</td></tr>
<tr><td>DB0 to DB7</td><td>204-211</td><td>I/O</td><td>Parallel Interface 8 Bit Data Bus</td></tr>
<tr><td>R/$\overline{W}$</td><td>212</td><td>I</td><td>Parallel Interface Read & Write Control Line</td></tr>
<tr><td>PCLK</td><td>202</td><td>I</td><td>Parallel Interface Data Latch Signal.</td></tr>
<tr><td>PD/$\overline{C}$</td><td>203</td><td>I</td><td>Parallel Interface Data/Command Selector</td></tr>
</table>

Table 2. Pin Description (continued)

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td>SDIN</td><td>217</td><td>I</td><td>Serial Interface Data Input</td></tr>
<tr><td>SCLK</td><td>214</td><td>I</td><td>Serial Interface Clock</td></tr>
<tr><td>$\overline{SCE}$</td><td>215</td><td>I</td><td>Serial Interface ENABLE. When Low the Incoming Data are Clocked In.</td></tr>
<tr><td>SD/$\overline{C}$</td><td>216</td><td>I</td><td>Serial Interface Data/Command Selector</td></tr>
<tr><td>SOUT</td><td>218</td><td>O</td><td>Serial Out</td></tr>
<tr><td>$\overline{BSYFLG}$</td><td>219</td><td>O</td><td>Active Procedure Flag. Notice if There is an ongoing Internal Operation or an active reset. Active Low.</td></tr>
<tr><td>T1 to T12</td><td>240-247, 182-185</td><td>I/O</td><td>Test Pads - A 50kohm pull-down resistor is added on input pis..
<table>
<tr><th>Pad_name</th><th>Pin_configuration</th></tr>
<tr><td>TEST_1</td><td>OPEN</td></tr>
<tr><td>TEST_2</td><td>OPEN</td></tr>
<tr><td>TEST_3</td><td>OPEN</td></tr>
<tr><td>TEST_4</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_5</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_6</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_7</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_8</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_9</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_10</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_11</td><td>VSS/VSSAUX</td></tr>
<tr><td>TEST_12</td><td>VSS/VSSAUX</td></tr>
</table></td></tr>
</table>

Figure 2. Chip Mechanical Drawing

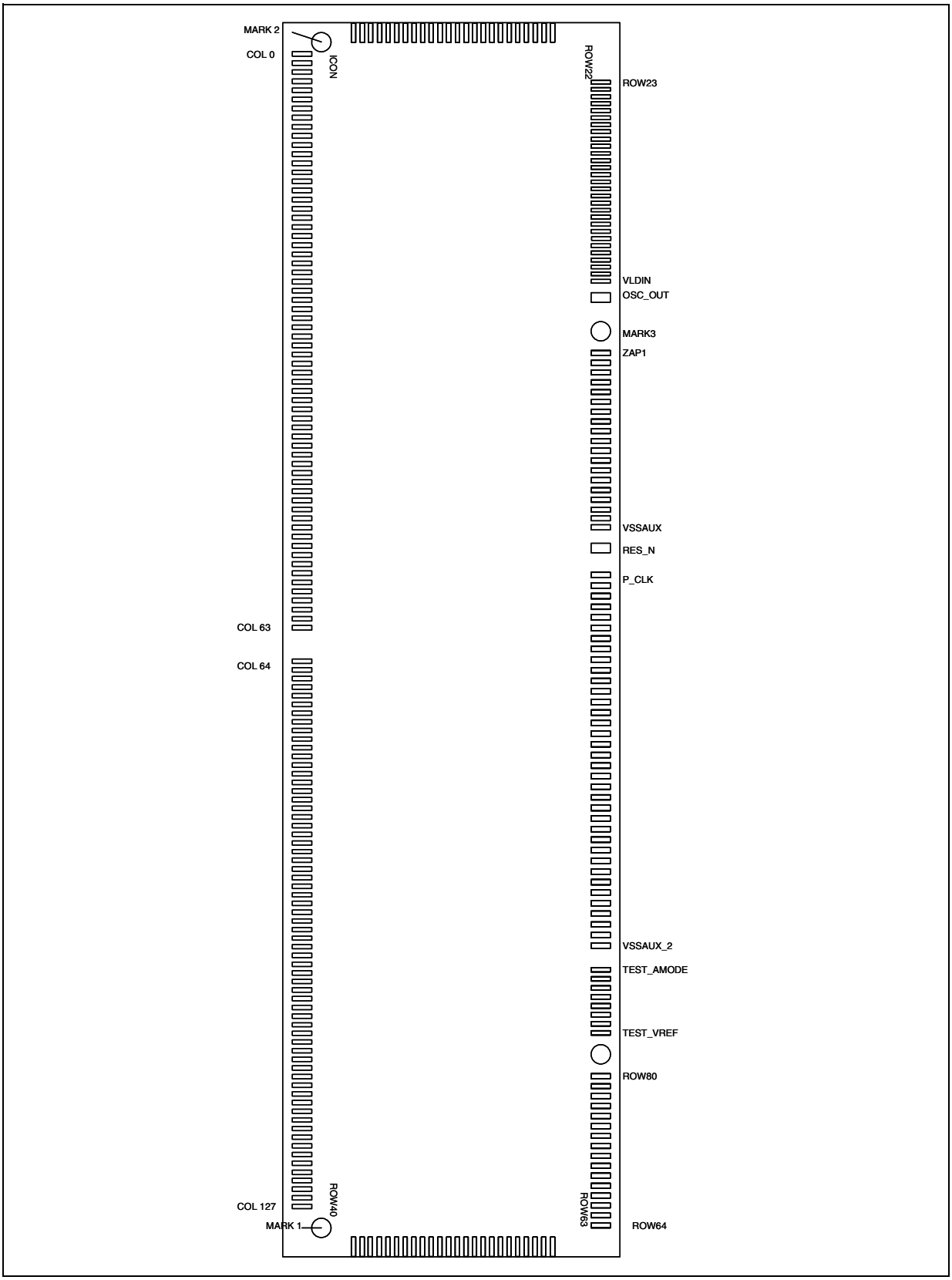
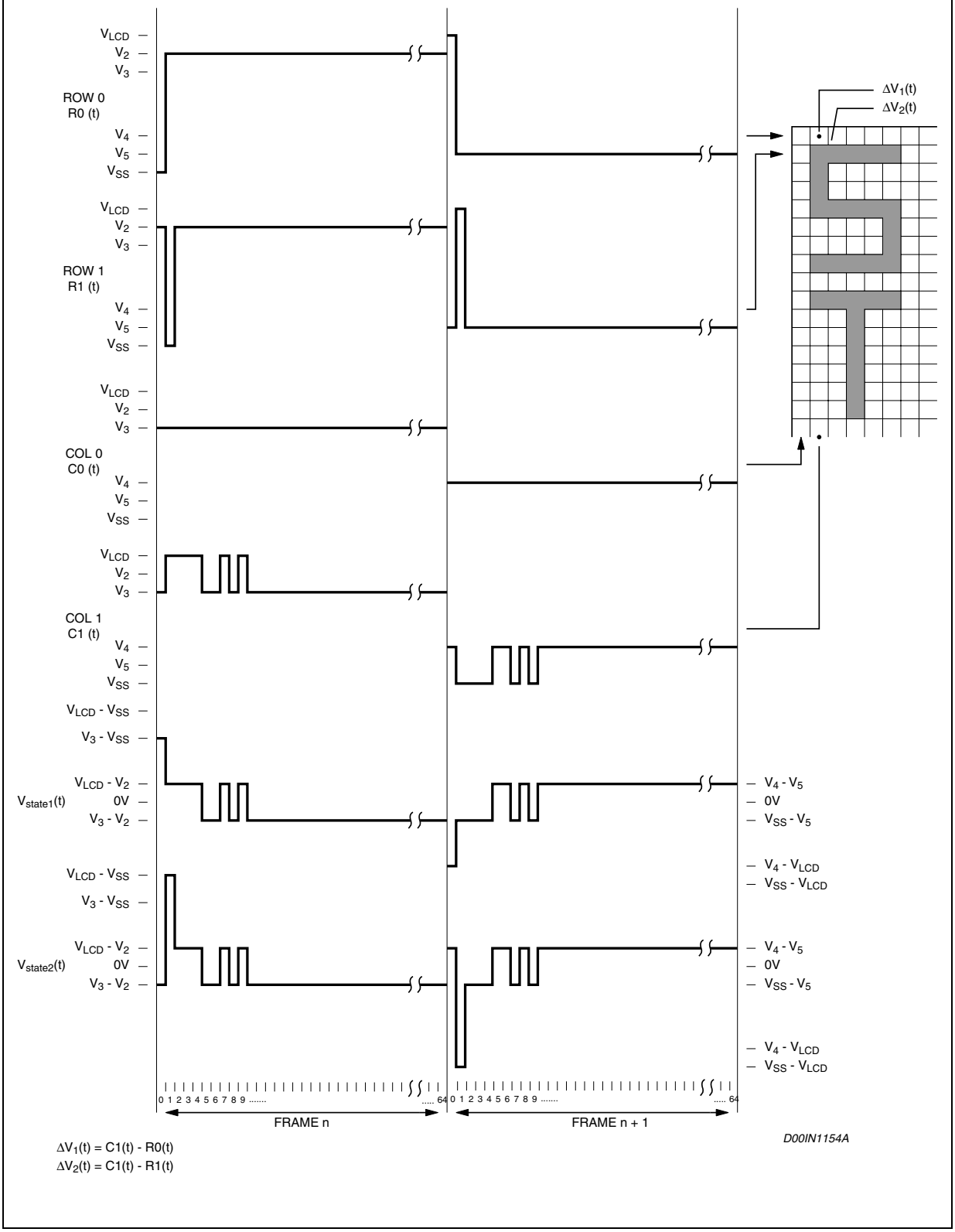


Figure 3. Improved ALTH & PLESKO Driving Method



4 CIRCUIT DESCRIPTION

4.1 Supplies Voltages and Grounds

V_{DD2} is supply voltages to the internal voltage generator (see below). If the internal voltage generator is not used, this should be connected to V_{DD1} pad. V_{DD1} supplies the rest of the IC. V_{DD1} supply voltage could be different form V_{DD2}.

$$V_{DD2} \geq \frac{2V_{LCD}}{(n+4)} + 200mV$$

4.2 Internal Supply Voltage Generator

The IC has a fully integrated (no external capacitors required) charge pump for the Liquid Crystal Display supply voltage generation. The multiplying factor can be programmed to be: Auto, X6, X5, X4, X3, X2, using the 'set CP Multiplication' Command. If Auto is set, the multiplying factor is automatically selected to have the lowest current consumption in every condition. This make possible to have an input voltage that changes over time and a constant V_{LCD} voltage. The output voltage (V_{LCDOUT}) is tightly controlled through the $V_{LCDSENSE}$ pad. For this voltage, eight different temperature coefficients (TC, rate of change with temperature) can be programmed using the bits TC1 and TC0 and T2,T1 & T0. This will ensure no contrast degradation over the LCD operating range. Using the internal charge pump, the V_{LCDIN} and V_{LCDOUT} pads must be connected together. An external supply could be connected to V_{LCDIN} to supply the LCD without using the internal generator. In such event the V_{LDCOUT} and $V_{LCDSENSE}$ must be connected to GND and the internal voltage generator must be programmed to zero (PRS = [0;0], Vop = 0 - Reset condition).

4.3 Oscillator

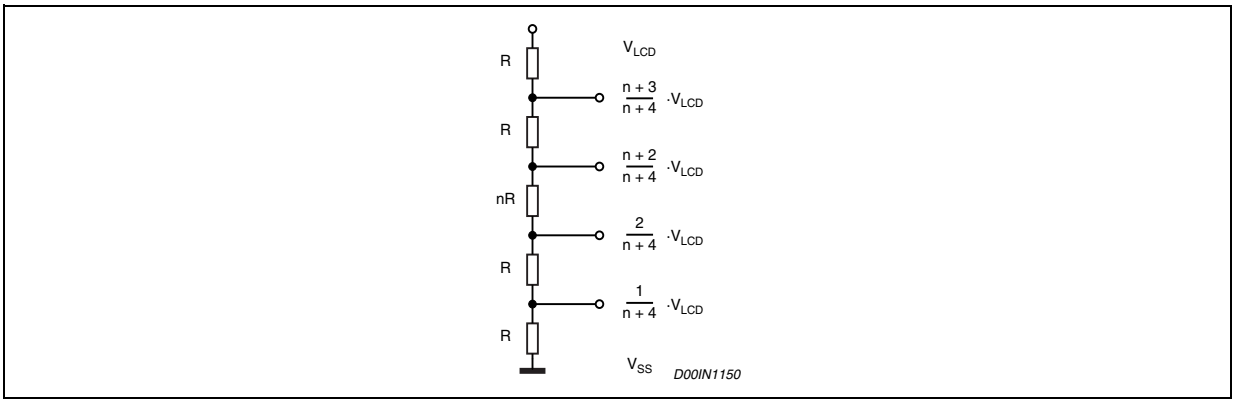
A fully integrated oscillator (requires no external components) is present to provide the clock for the Display System. When used the OSC pad must be connected to V_{DD1} pad. An external oscillator could be used and fed into the OSC pin. An oscillator out is provided on the OSCOUT Pad to cascade two or more drivers

4.4 Bias Levels

To properly drive the LCD, six (Including VLCD and VSS) different voltage (Bias) levels are generated. The ratios among these levels and VLCD, should be selected according to the MUX ratio (m). They are established to be (Fig. 4):

$$V_{LCD}, \frac{n+3}{n+4} V_{LCD}, \frac{n+2}{n+4} V_{LCD}, \frac{2}{n+4} V_{LCD}, \frac{1}{n+4} V_{LCD}, V_{SS}$$

Figure 4. Bias level Generator



thus providing an 1/(n+4) ratio, with n calculated from:

$$n = \sqrt{m} - 3$$

For m = 81, n = 6 and an 1/10 ratio is set.

For m = 65, n =5 and an 1/9 ratio is set.

The STE2002S provides three bits (BS0, BS1, BS2) for programming the desired Bias Ratio as shown below:

BS2	BS1	BS0	n
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

The following table Bias Level for m = 65 and m = 81 are provided:

Symbol	m = 65 (1/9)	m = 81 (1/10)
V1	V_{LCD}	V_{LCD}
V2	8/9*V_{LCD}	9/10*V_{LCD}
V3	7/9*V_{LCD}	8/10*V_{LCD}
V4	2/9*V V_{LCD}	2/10*V_{LCD}
V5	1/9 *V_{LCD}	1/10*V_{LCD}
V6	V_{SS}	V_{SS}

4.5 LCD Voltage Generation

The LCD Voltage at reference temperature (To = 27°C) can be set using the VOP register content according to the following formula:

$$V_{LCD}(T=To) = V_{LCD}o = (Ai+V_{OP} \cdot B) \qquad (i=0,1,2)$$

with the following values:

Symbol	Value	Unit	Note
Ao	2.95	V	PRS = [0;0]
A1	6.83	V	PRS = [0;1]
A2	10.71	V	PRS = [1;0]
B	0.0303	V	
To	27	°C	

Note that the three PRS values produce three adjacent ranges for VLCD. If the V_{OP} register and PRS bits are set to zero the internal voltage generator is switched off.

The proper value for the VLCD is a function of the Liquid Crystal Threshold Voltage (Vth) and of the Multiplexing Rate. A general expression for this is:

$$V_{LCD} = \frac{1+\sqrt{m}}{\sqrt{2 \cdot \left(1-\frac{1}{\sqrt{m}}\right)}} \cdot V_{th}$$

For MUX Rate m = 65 the ideal V_{LCD} is:

$$V_{LCD(to)} = 6.85 \cdot V_{th}$$

than:

$$V_{op} = \frac{(6.85 \cdot V_{th} - A_i)}{0.03}$$

4.6 Temperature Coefficient

As the viscosity, and therefore the contrast, of the LCD are subject to change with temperature, there's the need to vary the LCD Voltage with temperature. The STE2002S provides the possibility to change the VLCD in a linear fashion against temperature with eight different Temperature Coefficient selectable through the T2, T1 and T0 bits. Only four of them are available with basic instruction set (TC1 & TC0 Bits).

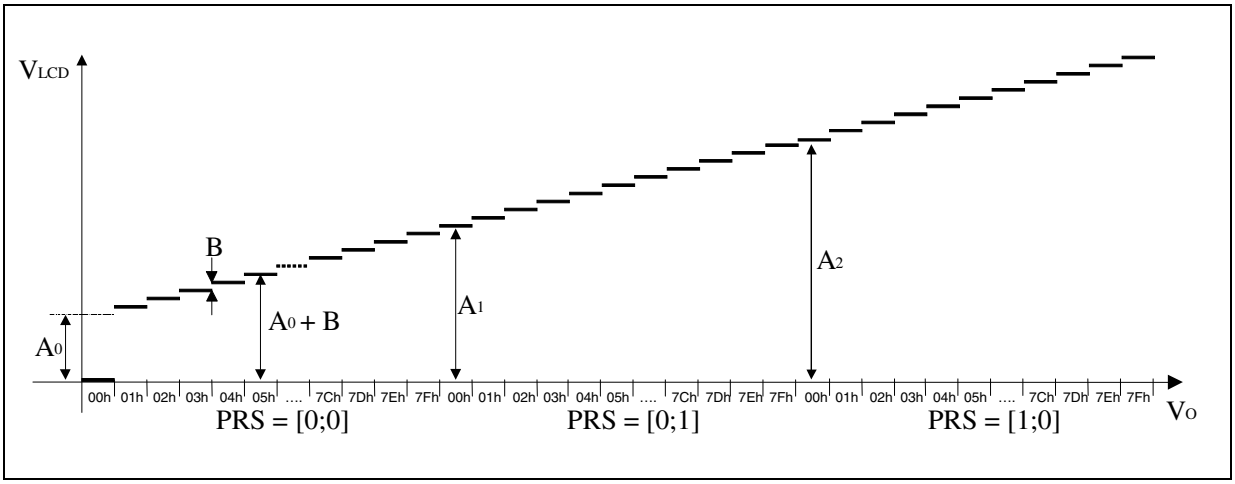
Table 3.

NAME	TC1	TC0	Value	Unit
TC0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC2	0	1	$-0.7 \cdot 10^{-3}$	1/°C
TC3	1	0	$-1.05 \cdot 10^{-3}$	1/°C
TC6	1	1	$-2.1 \cdot 10^{-3}$	1/°C

Table 4.

NAME	T2	T1	T0	Value	Unit
TC0	0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC1	0	0	1	$-0.35 \cdot 10^{-3}$	1/°C
TC2	0	1	0	$-0.7 \cdot 10^{-3}$	1/°C
TC3	0	1	1	$-1.05 \cdot 10^{-3}$	1/°C
TC4	1	0	0	$-1.4 \cdot 10^{-3}$	1/°C
TC5	1	0	1	$-1.75 \cdot 10^{-3}$	1/°C
TC6	1	1	0	$-2.1 \cdot 10^{-3}$	1/°C
TC7	1	1	1	$-2.3 \cdot 10^{-3}$	1/°C

Figure 5.



Finally, the V_{LCD} voltage at a given (T) temperature can be calculated as:

$$V_{LCD}(T) = V_{LCD}o \cdot [1 + (T\text{-}To) \cdot TC]$$

5 DISPLAY DATA RAM

The STE2002S, provides an 88X128 bits Static RAM to store Display data. This is organized into 11 (Bank0 to Bank10) banks with 128 Bytes. One of these banks (128 bits wide) can be used for Icons. RAM access is accomplished in either one of the Bus Interfaces provided (see below). Allowed addresses are X0 to X127 (Horizontal) and Y0 to Y10 (Vertical).

When writing to RAM, four addressing mode are provided:

- Normal Horizontal (MX=0 and V=0), having the column with address X= 0 located on the left of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the following bank and X restarts from X=0. (Fig. 6)
- Normal Vertical (MX=0 and V=1), having the column with address X= 0 located on the left of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), X address pointer is set to jump to next column and Y restarts from Y=0 (Fig. 7).
- Mirrored Horizontal (MX=1 and V=0), having the column with address X= 0 located on the right of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the next bank and X restarts from X=0 (fig. 8).
- Mirrored Vertical (MX=1 and V=1), having the column with address X= 0 located on the right of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), the X pointer is set to jump to next column and Y restarts from Y=0 (fig. 9).

After the last allowed address (X;Y)=(X-Carriage; Y-Carriage), the address pointers always jump to the cell with address (X;Y) = (0;0) (Figg. 10, 11, 12 & 13).
Data bytes in the memory could have the MSB either on top (D0 = 0, Fig.14) or on the bottom (D0=1, Fig. 15).
The STE2002S provides also means to alter the normal output addressing. A mirroring of the Display along the X axis is enabled setting to a logic one MY bit.This function doesn't affect the content of the memory RAM. It is only related to the visualization process.
When ICON MODE=1 the Icon Row is not mirrored with MY and is not scrolled. When ICON Mode=0 the Icon Row is like the other graphic lines and is mirrored and scrolled.

Four are the multiplex ratio available when the partial display mode is disabled (MUX 33, MUX 49, MUX 65 and MUX 81).

Only a subset of writable rows are output on Row drivers.

When **Y-Carriage<MUX/8,** if Mux 65 is selected only the first 65 memory rows are visualized, if Mux 49 is selected only the first 49 memory rows are visualized, if Mux 33 is selected only the first 33 memory rows are visualized. All unused Row and Column drivers must be left floating.

When **Y-Carriage<MUX/8,** the icon Bank is located to BANK 10 in MUX 81 Mode, to BANK8 in MUX 65 Mode, to BANK 6 in MUX 49 Mode and to BANK 4 in MUX 33 Mode.

When **Y-Carriage>MUX/8** lines only 33, 49, 65 or 81 lines are visualized but it is possible to select which lines of DDRAM are connected on the output drivers. The DDRAM rows to visualized can be selected in the 0-Y-Carriage*8 range using the scrolling function.

When **Y-Carriage>MUX lines**, the icon row is moved in DDRAM to the first row of the Y-CARRIAGE Return BANK even if it is always connected on the same output Driver.

When **MY=0**, the icon Row is output on R80 in mux 81 mode, on R72 in MUX 65, on R64 in MUX49 and on R56 in MUX 33.

When **MY=1**, and **ICON MODE=1**, the icon Row is output on R80 in mux 81 mode, on R72 in MUX 65, on R64 in MUX49 and on R56 in MUX 33.
When **MY=1**, and **ICON MODE=0**, the icon Row is output on R0 whatever is the MUX Rate.

When **ICON MODE =1**, the Memory ICON Row content is output on ICON Pad.

If Not Used ICON Pad must be left floating.

Figure 6. Automatic data RAM writing sequence with V=0 and Data RAM Normal Format (MX=0)[1]

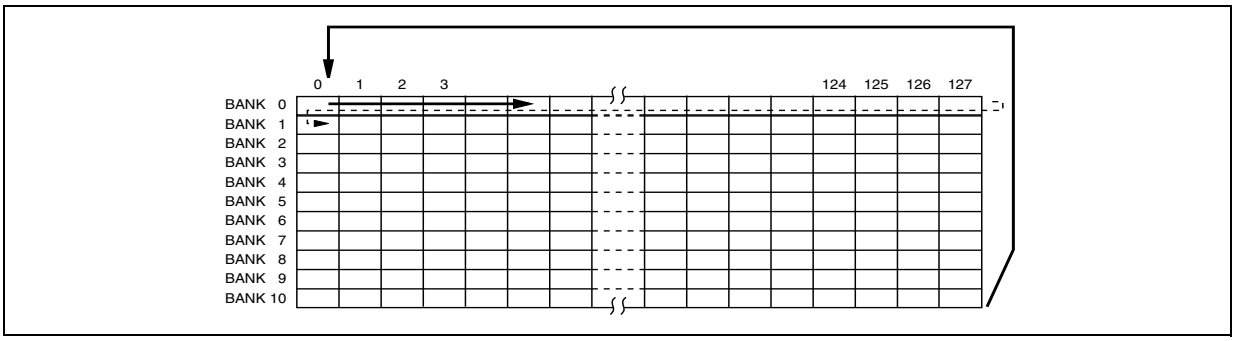


Figure 7. Automatic data RAM writing sequence with V=1 and Data RAM Normal Format (MX=0)[1]

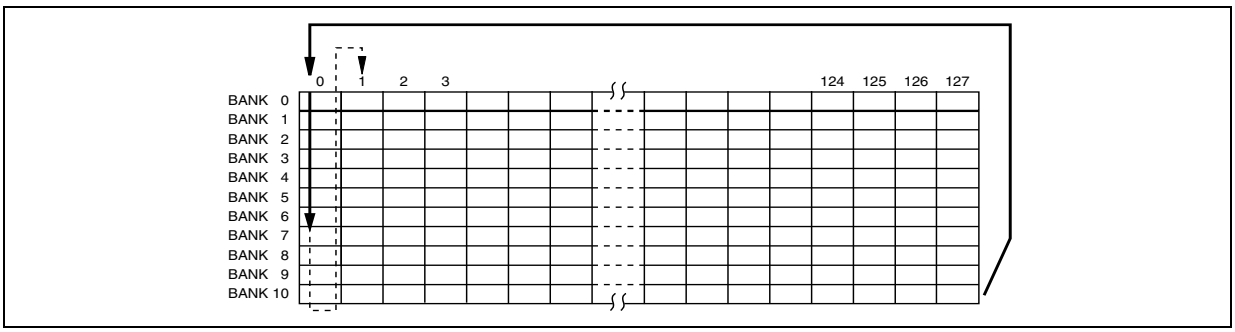


Figure 8. Automatic data RAM writing sequence with V=0 and Data RAM Mirrored Format (MX=1)[1]

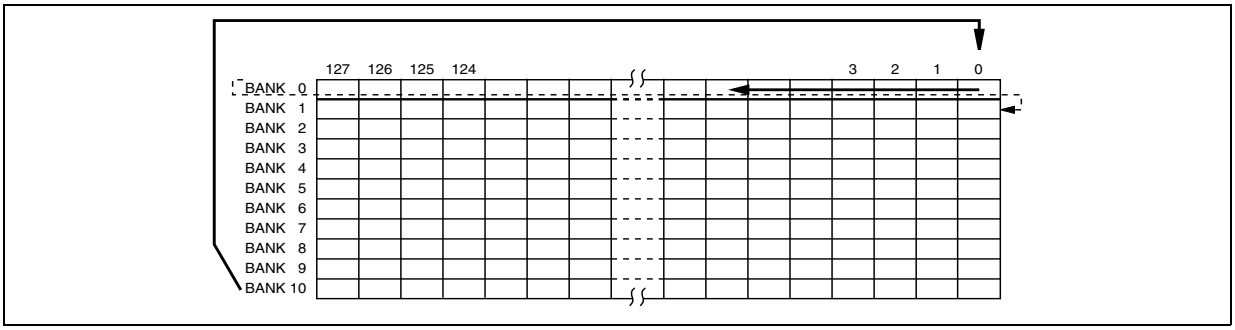
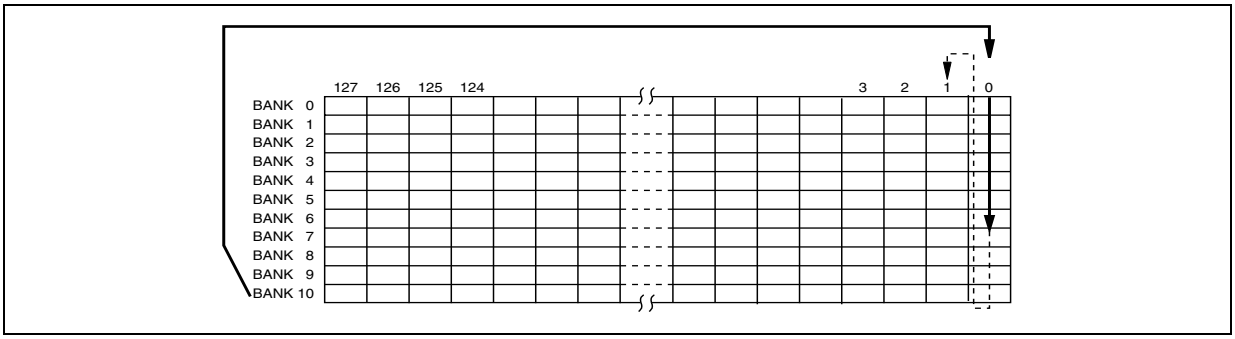


Figure 9. Automatic data RAM writing sequence with V=1 and Data RAM Mirrored Format (MX=1)[1]



1. X Carriage=127; Y-Carriage = 12

Figure 10. Automatic data RAM writing sequence with X-Y Carriage Return (V=0; MX=0)

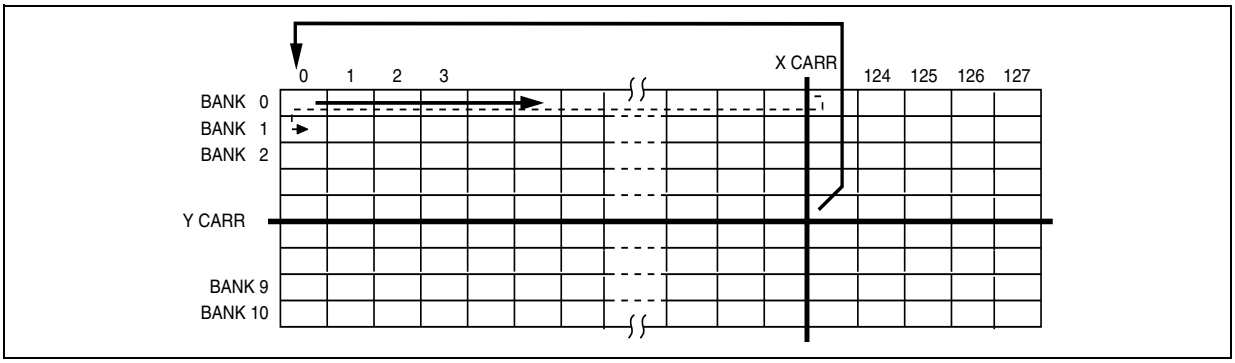


Figure 11. Automatic data RAM writing sequence with X-Y Carriage Return (V=1; MX=0)

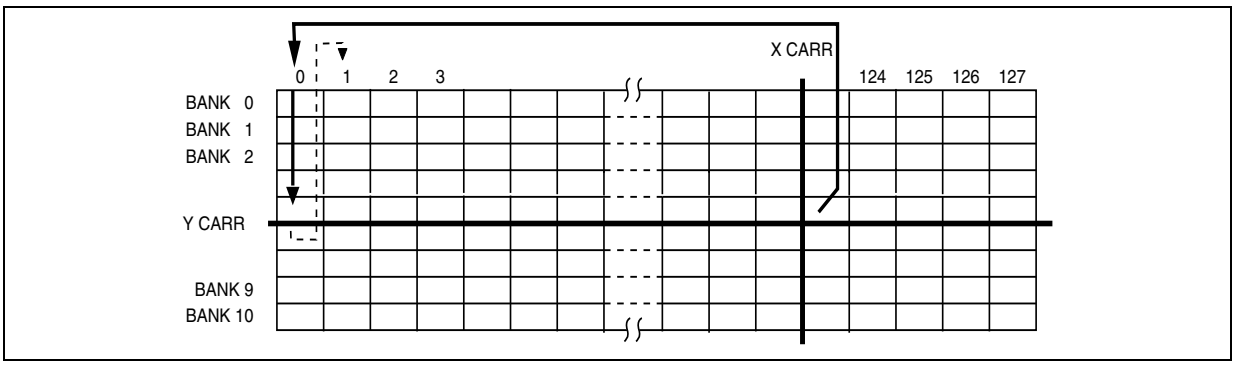


Figure 12. Automatic data RAM writing sequence with X-Y Carriage Return (V=0; MX=1)

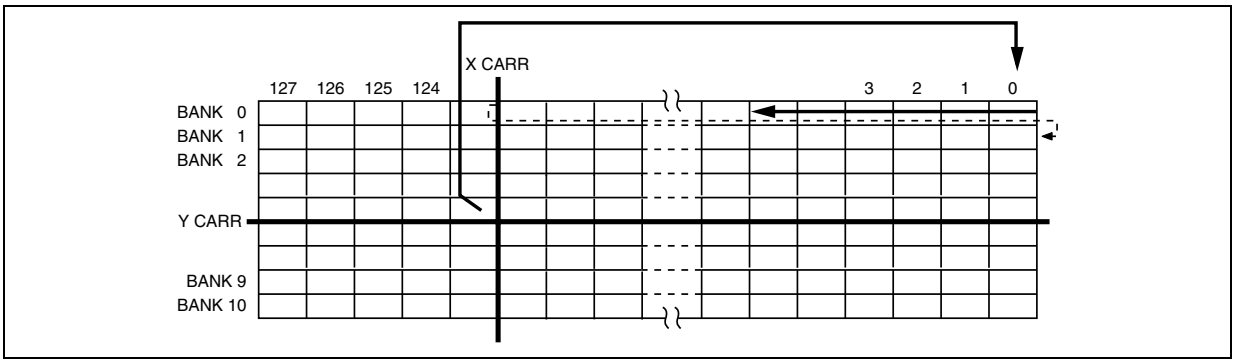


Figure 13. Automatic data RAM writing sequence with X-Y Carriage Return (V=1; MX=1)

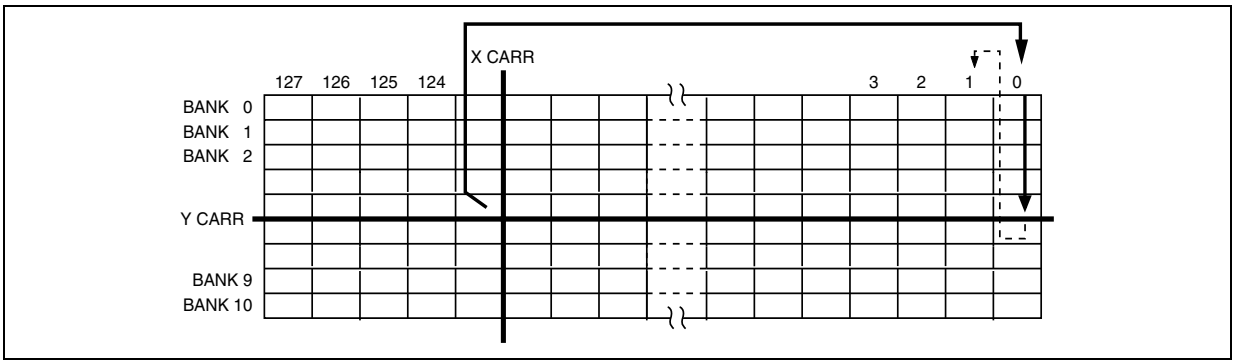


Figure 14. Data RAM Byte organization with D0 = 0

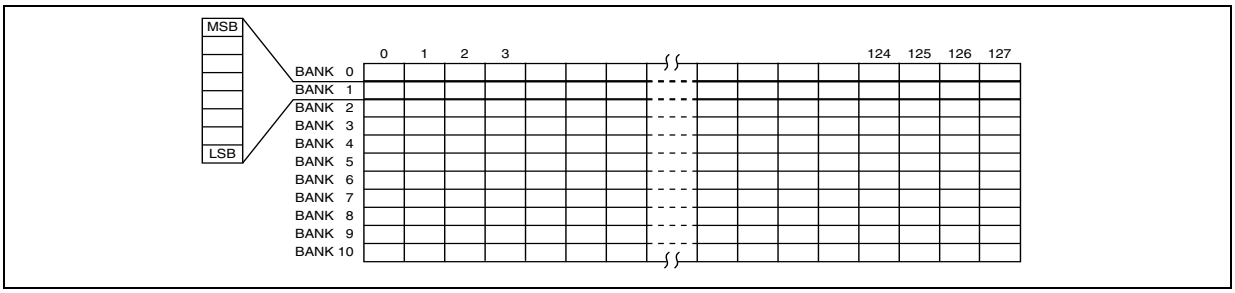


Figure 15. Data RAM Byte organization with D0 = 1

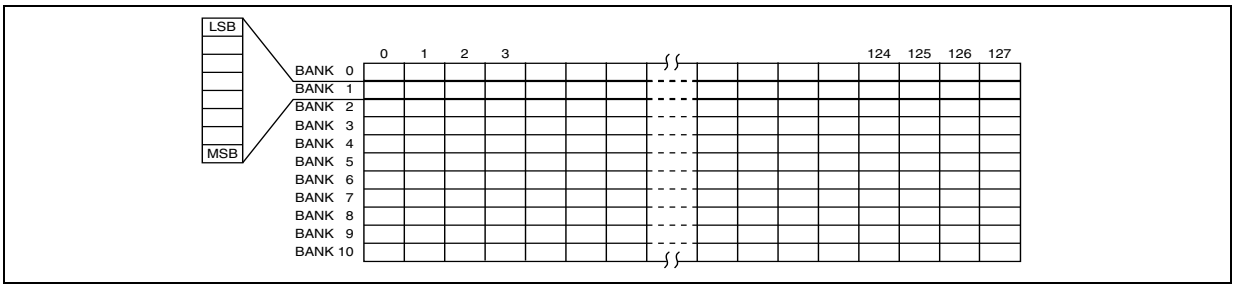


Figure 16. Memory Rows vs. Row drivers mapping with MY=0, MUX81, ICON MODE=0,1

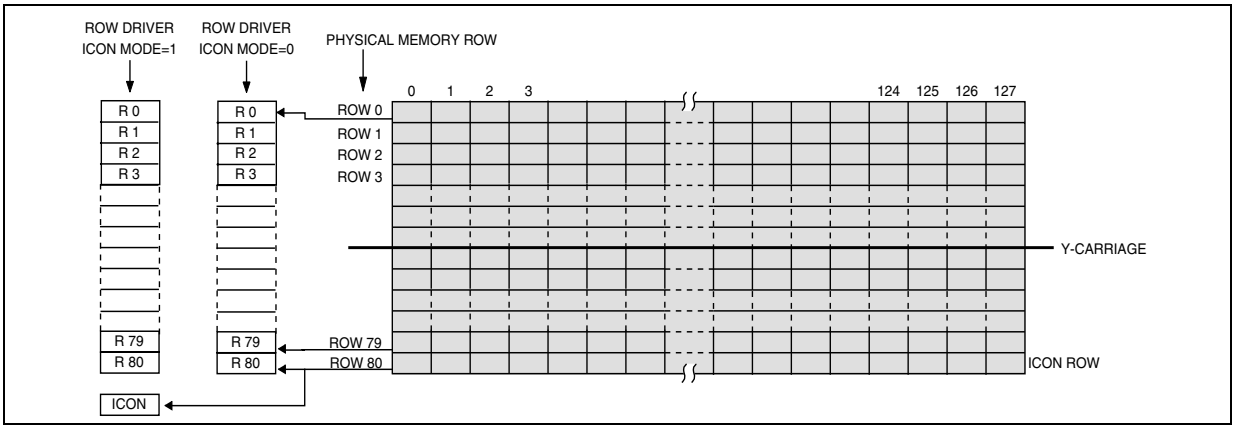


Figure 17. Memory Rows vs. Row drivers mapping with MY=0, MUX 81, SCROLL POINTER = +3, ICON MODE=1

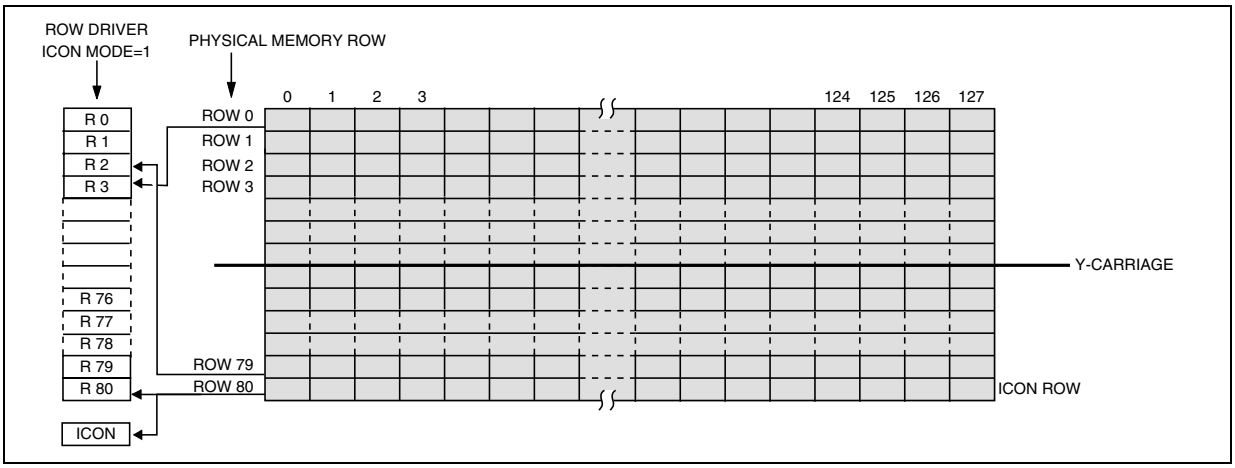


Figure 18. Memory Rows vs. Row drivers mapping with MY=0, MUX 81, SCROLL POINTER=+3, ICON MODE=0

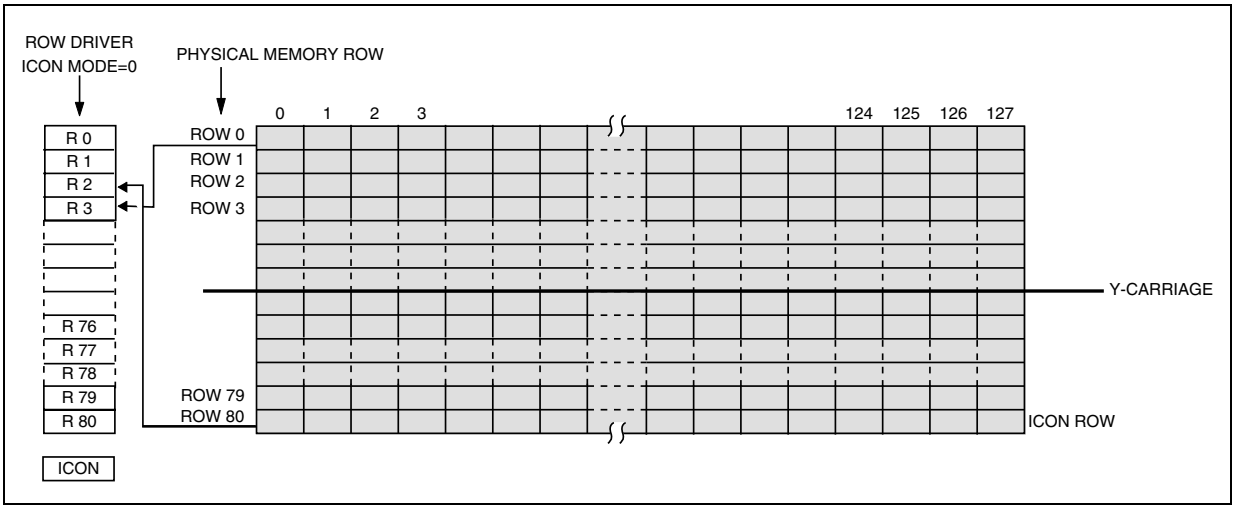


Figure 19. Memory Rows vs. Row drivers mapping with MUX 65 Y-CARRIAGE<=8 SCROLL POINTER=0, ICON MODE=1

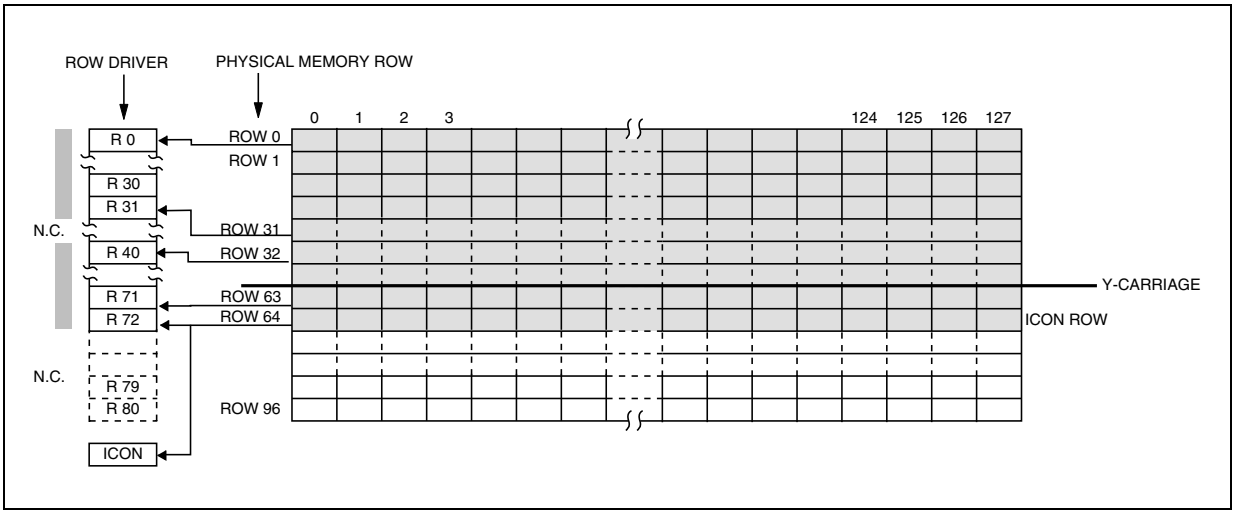


Figure 20. Memory Rows vs. Row drivers mapping with MUX65, Y-CARRIAGE>8, SCROLL POINTER=0, ICON MODE=1

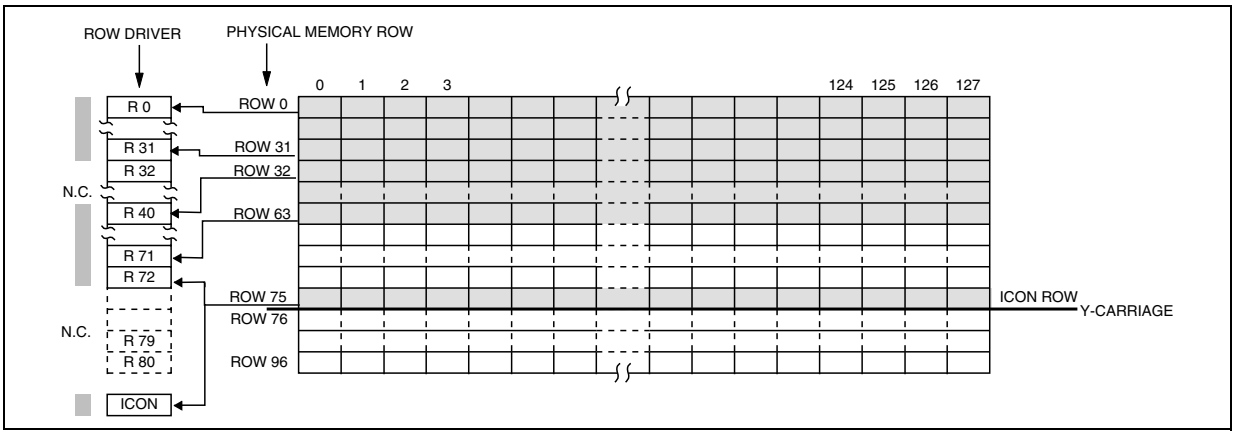


Figure 21. Memory Rows vs. Row drivers mapping with MUX65, Y-CARRIAGE>8, SCROLL POINTER=3, ICON MODE=1,

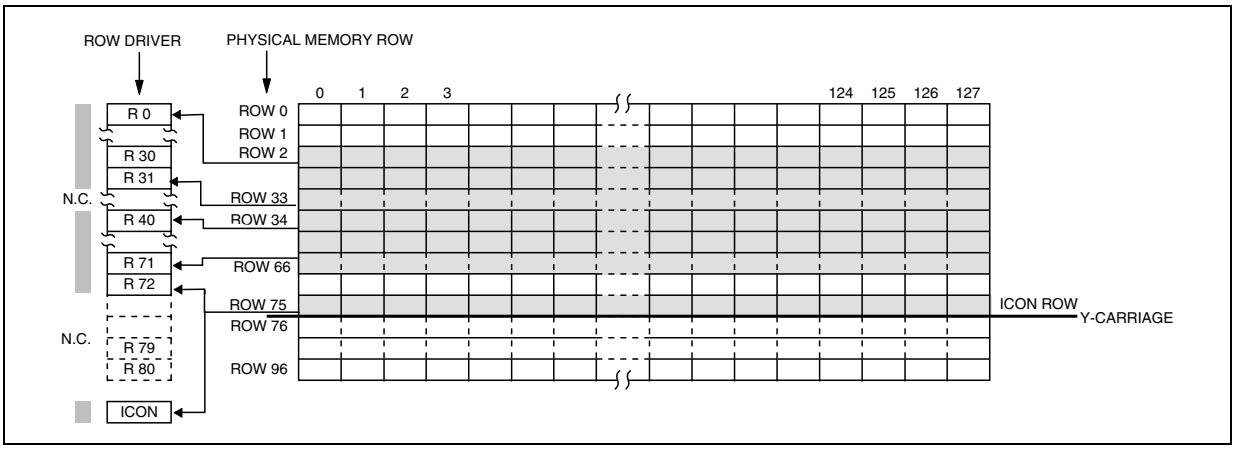


Figure 22. Memory Rows vs. Row drivers mapping with MY=1, MUX81, ICON MODE 0,1 SCROLL POINTER=0

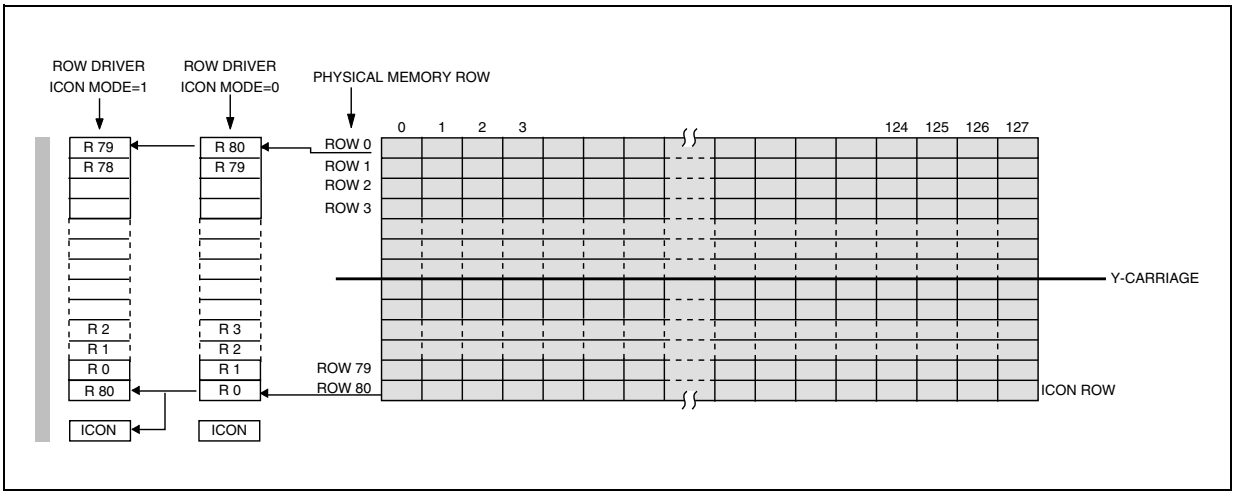


Figure 23. Memory Rows vs. Row drivers mapping with MY=1, MUX81, SCROLL OFFSET= +3, ICON MODE =0

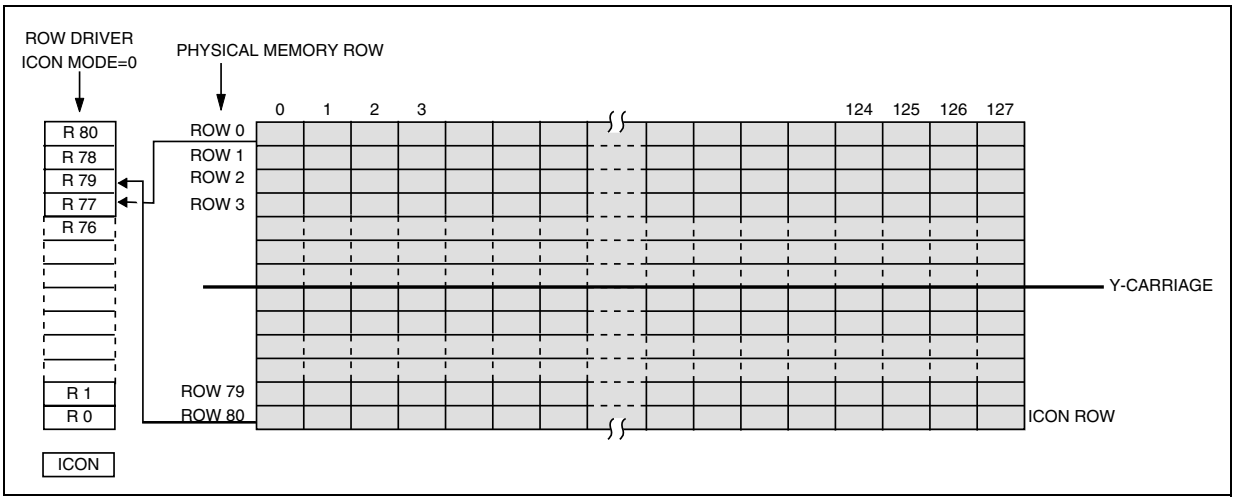


Figure 24. Memory Rows vs. Row drivers mapping with MY=1, MUX81, SCROLL OFFSET= +3, ICON MODE =1

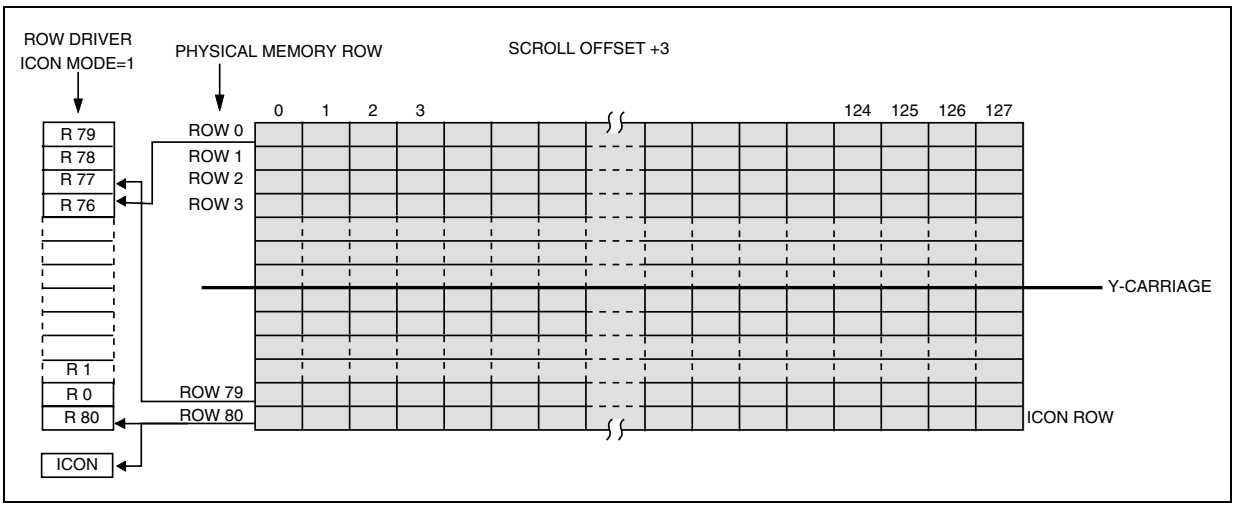


Figure 25. Row Drivers vs. LCD Panel Interconnection in MUX81 Mode

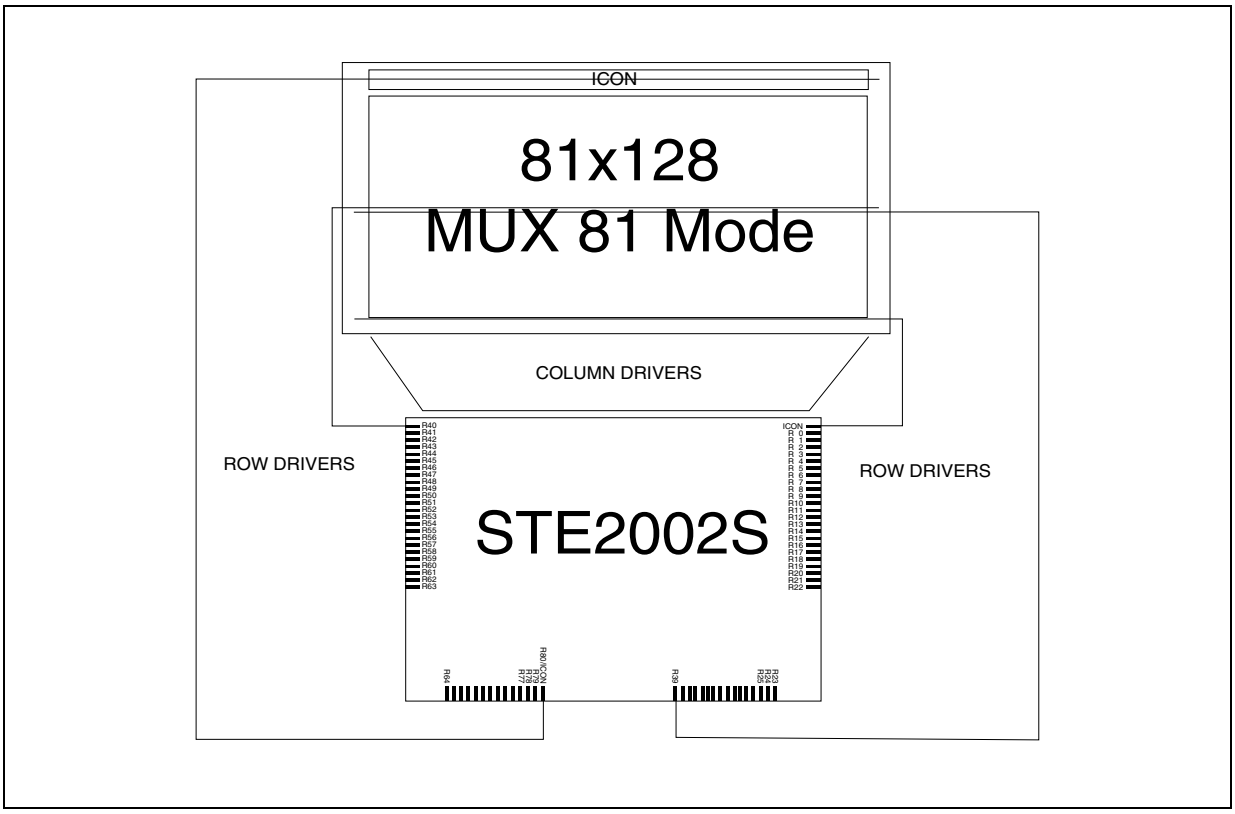


Figure 26. Row Drivers vs. LCD Panel Interconnection in MUX65 Mode

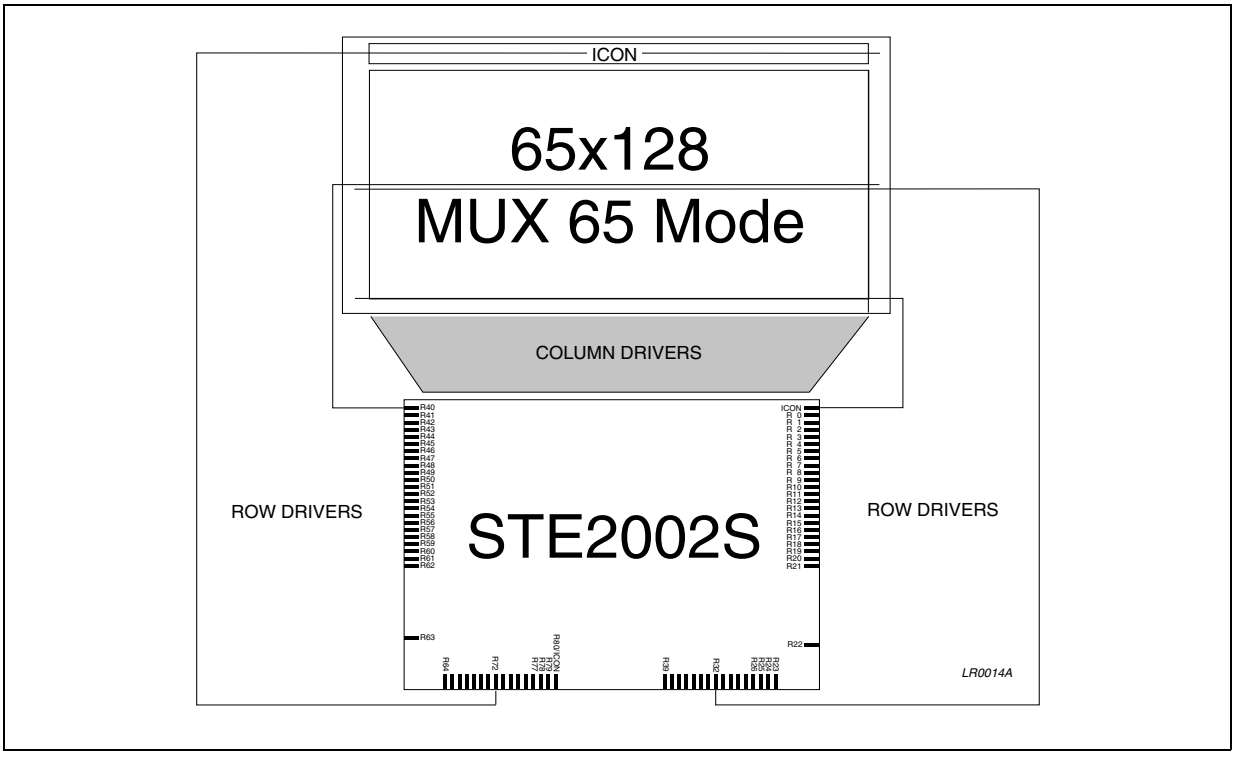


Figure 27. Row Drivers vs. LCD Panel Interconnection in MUX49 Mode

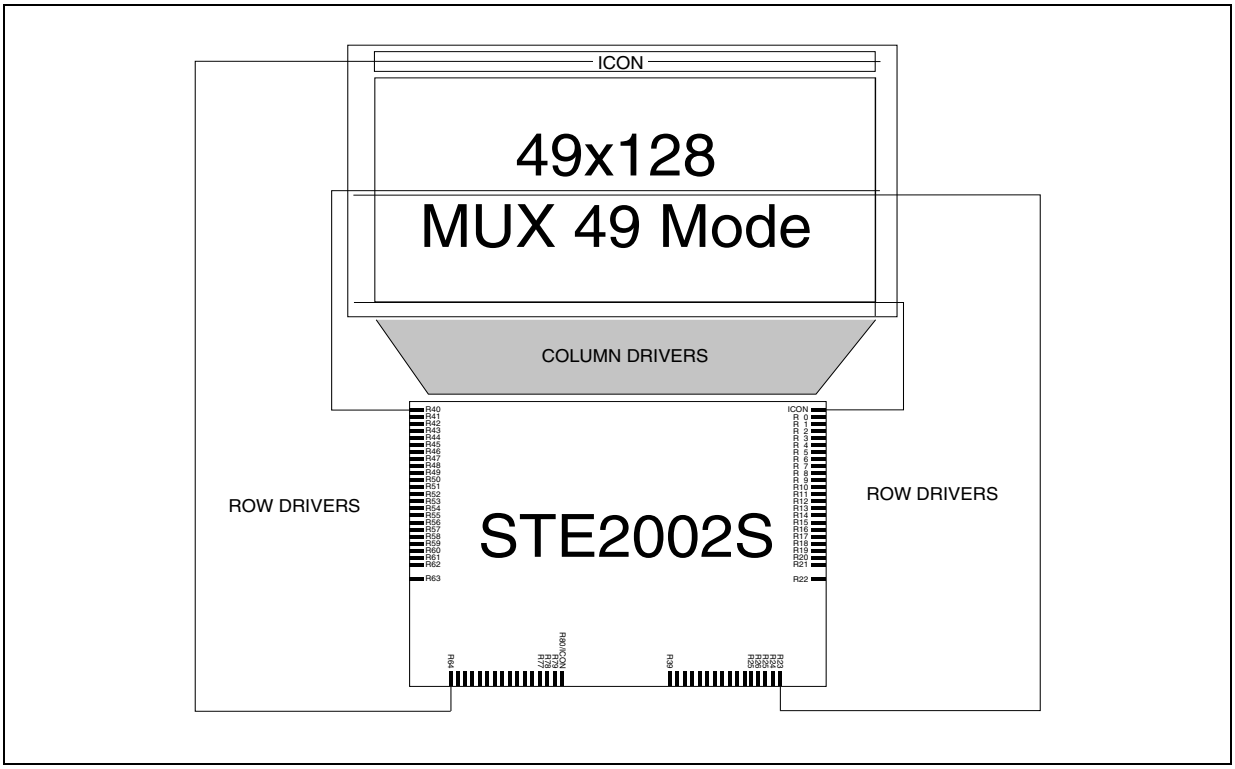
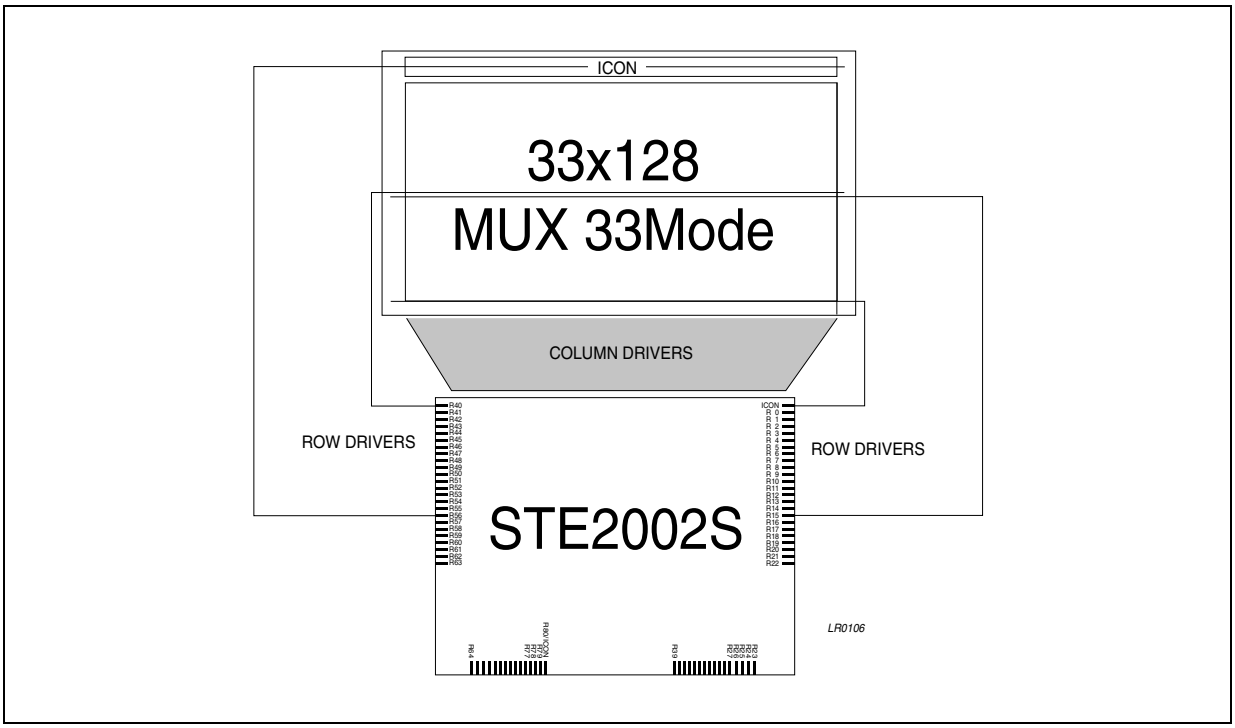


Figure 28. Row Drivers vs. LCD Panel Interconnection in MUX33 Mode



6 INSTRUCTION SET

Two different instructions formats are provided:
- With D/$\overline{C}$ set to LOW
commands are sent to the Control circuitry.
- With D/$\overline{C}$ set to HIGH
the Data RAM is addressed.

Two different instruction set are embedded: the STE2001-like instruction set and the extended instruction set. To select the STE2001-like instruction set the EXT pad has to be connected to a logic LOW (connect to VSS). To select the extended instruction the EXT pad has to be connected to a logic HIGH (connect to VDD1).

The instructions have the syntax summarized in Table 1 (basic-set) and Table 2 (extended set)

6.1 Reset ($\overline{RES}$)

At power-on, all internal registers are configured with the default value. The RAM content is not defined. A Reset pulse on RES pad (active low) re-initialize the internal registers content (see Tables 3,4,5,&6). Applying a reset pulse, every on-going communication with the host controller is interrupted. After the power-on, the Software Reset instruction can be used to re-load the reset configuration into the internal registers

The Default configurations is: .

- Horizontal addressing (V = 0)
- Normal instruction set (H[1:0] = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6: 0] = 0 and Y[4: 0] = 0
- Temperature coefficient (TC[1: 0] = 0)
- Bias system (BS[2: 0] = 0)
- Multiplexing Ratio (M[1:0]=0)
- Frame Rate (FR[1:0]="75Hz")
- Power Down (PD = 1)
- Dual Partial Display Disabled (PE=0)
- V_{OP}=0

A MEMORY BLANK instruction can be executed to clear the RAM content.

6.2 Power Down (PD = 1)

When at Power Down, all LCD outputs are kept at V_{SS} (display off). Bias generator and V_{LCD} generator are OFF (V_{LCDOUT} output is discharged to V_{SS}, and then is possible to disconnect V_{LCDOUT}). The internal Oscillator is in off state. An external clock can be provided. The RAM contents is not cleared.

6.3 Memory Blanking Procedure

This instruction allows to fill the memory with "blank" patterns, in order to delete patterns randomly generated in memory when starting up the device. This instruction substitutes (128X11) single "write" instructions. It is possible to program "Memory Blanking Procedure" only under the following conditions:

- PD bit = 0

The end of the procedure will be notified on the $\overline{BSY\_FLG}$ pad going HIGH (while LOW the procedure is running). Any instruction programmed with $\overline{BSY\_FLG}$ LOW will be ignored that is, no instruction can be programmed for a period equivalent to 128X11 internal write cycles (128X11X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I^2C interface).

6.4 Checker Board Procedure

This instruction allows to fill the memory with "checker-board" pattern. It is mainly intended to developers, who can now simply obtain complex module test configuration by means of a single instruction. It is possible to program "Checker Board Procedure" only under the following conditions:

- PD bit = 0

The end of the procedure will be notified on the $\overline{\text{BSY\_FLG}}$ pad going HIGH, while LOW the procedure is running. Any instruction programmed with $\overline{\text{BSY\_FLG}}$ LOW will be ignored, that is, no instruction can be programmed for a period equivalent to 128X11 internal write cycles (128X11X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I^2C interface).

6.5 Scrolling function

The STE2002S can scroll the graphics display in units of raster-rows. The scrolling function is achieved changing the correspondence between the rows of the logical memory map and the output row drivers. The scroll function doesn't affect the data ram content. It is only related to the visualization process. The information output on the drivers is related to the row reading sequence (the 1st row read is output on R0, the 2nd on R1 and so on). Scrolling means reading the matrix starting from a row that is sequentially increased or decreased. After every scrolling command the offset between the memory address and the memory scanning pointer is increased or decreased by one. The offset range changes in accordance with MUX Rate. After 80th/81th scrolling commands in MUX 81 mode, or after the 64th/65th scrolling commands in mux 65 mode, or after 48nd/49rd scrolling command in MUX 49 mode, or after 32nd/33rd scrolling command in MUX 33 mode, the offset between the memory address and the memory scanning pointer is again zero (Cyclic Scrolling).
A Reset Scrolling Pointer instruction can be executed to force to zero the offset between the memory address and the memory scanning pointer
The Icon Row is not scrolled if ICON MODE =1. If ICON MODE=0 the last row is like a general purpose row and it is scrolled as other rows.
If the DIR Bit is set to a logic zero the offset register is increased by one and the raster is scrolled from top down. If the DIR Bit is set to a logic one the offset register is decreased by one and the raster is scrolled from bottom-up.

Table 5.

MUX RATE	ICON MODE	OFFSET RANGE	DESCRIPTION	ICON Row Driver with MY=0
MUX 33	1	0-31	ICON ROW NOT SCROLLED	R56
MUX 33	0	0-32	33 LINE GRAPHIC MATRIX	R56
MUX 49	1	0-47	ICON ROW NOT SCROLLED	R64
MUX 49	0	0-48	49 LINE GRAPHIC MATRIX	R64
MUX 65	1	0-63	ICON ROW NOT SCROLLED	R72
MUX 65	0	0-64	65 LINE GRAPHIC MATRIX	R72
MUX 81	1	0-79	ICON ROW NOT SCROLLED	R80
MUX 81	0	0-80	81 LINE GRAPHIC MATRIX	R80

6.6 Dual Partial Display

If the PE Bit is set to a logic one the dual partial display mode is enabled.
Eight partial display modes are available. The offset of the two partial display zones is row by row programmable. The Icon row is accessed last in each partial display frame.
Two sets of register for the HV-generator parameters are provided (PRS[1:0], Vop[6:0], BS[2:0], CP[2:0].). This allows switching from normal mode to partial display mode applying one instruction. The HV generator is automatically re configured using the parameters related to the enabled mode. The parameters of the two sets of registers with the same function are located in the same position of the instruction set. The registers related to the normal mode are accessible when normal mode (PE=0) is selected, the others are accessible when the partial display mode is enabled (PE=1). To Setup PRS[1:0], Vop[6:0], BS[2:0], CP[2:0] values the instruction flow proposed in Fig.46 must be followed. To setup Partial Display Sectors Start Address and Partial Display Mode no particular instruction flow has to be followed.

.

PD2	PD1	PD0	SECTION 1	SECTION2 (*)	RESET STATE
0	0	0	0	8 + Icon Row	000
0	0	1	8	0 + Icon Row	
0	1	0	8	8 + Icon Row	
0	1	1	0	16 + Icon Row	
1	0	0	16	0 + Icon Row	
1	0	1	8	16 + Icon Row	
1	1	0	16	8 + Icon Row	
1	1	1	16	16 + Icon Row	

(*) section2=y if Icon=0; section2=y+Icon if Icon=1

7 BUS INTERFACES

To provide the widest flexibility and ease of use the STE2002S features three different methods for interfacing the host Controller. To select the desired interface the SEL1 and SEL2 pads need to be connected to a logic LOW (connect to GND) or a logic HIGH (connect to VDD). All the I/O pins of the unused interfaces must be connected to GND.

All interfaces are working while the STE2002S is in Power Down

Table 6. .

SEL2	SEL1	Interface	Note
0	0	I^2C	Read and Write; Fast and High Speed Mode
0	1	Serial	Read and Write
1	0	Parallel	Read and Write
1	1		Not Used

7.1 I^2C Interface

The I^2C interface is a fully complying I^2C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different Ics. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of

the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2002S will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

To be compliant with the I^2C-bus Hs-mode specification the STE2002S is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 29. Bit transfer and START,STOP conditions definition

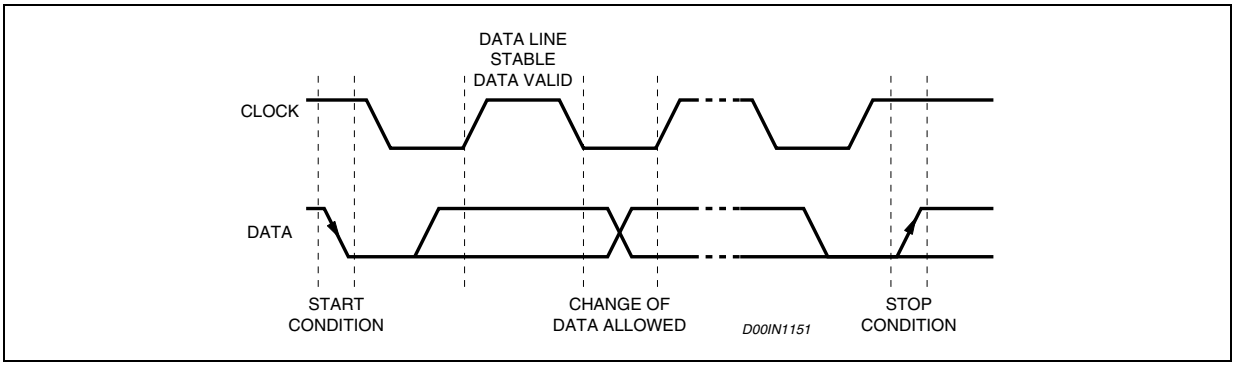
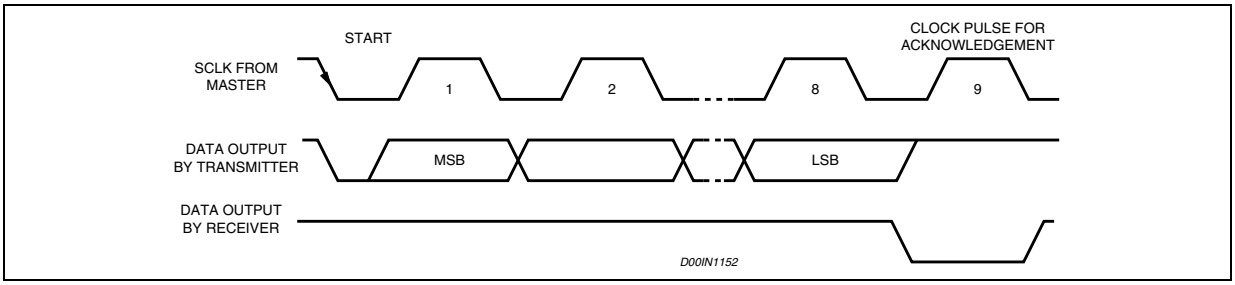


Figure 30. Acknowledgment on the I^2C-bus



7.1.1 Communication Protocol

The STE2002S is an I^2C slave. The access to the device is bi-directional since data write and status read are allowed. Four are the device addresses available for the device. All have in common the first 5 bits (01111). The two least significant bit of the slave address are set by connecting the SA0 and SA1 inputs to a logic 0 or to a logic 1.
To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, shown in Fig. 30, on the SDA bus line (Most significant bit first). This consists of the 7-bit Device select Code, and the 1-bit Read/Write Designator (R/$\overline{W}$).
All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer.

7.1.1.1 Writing Mode.

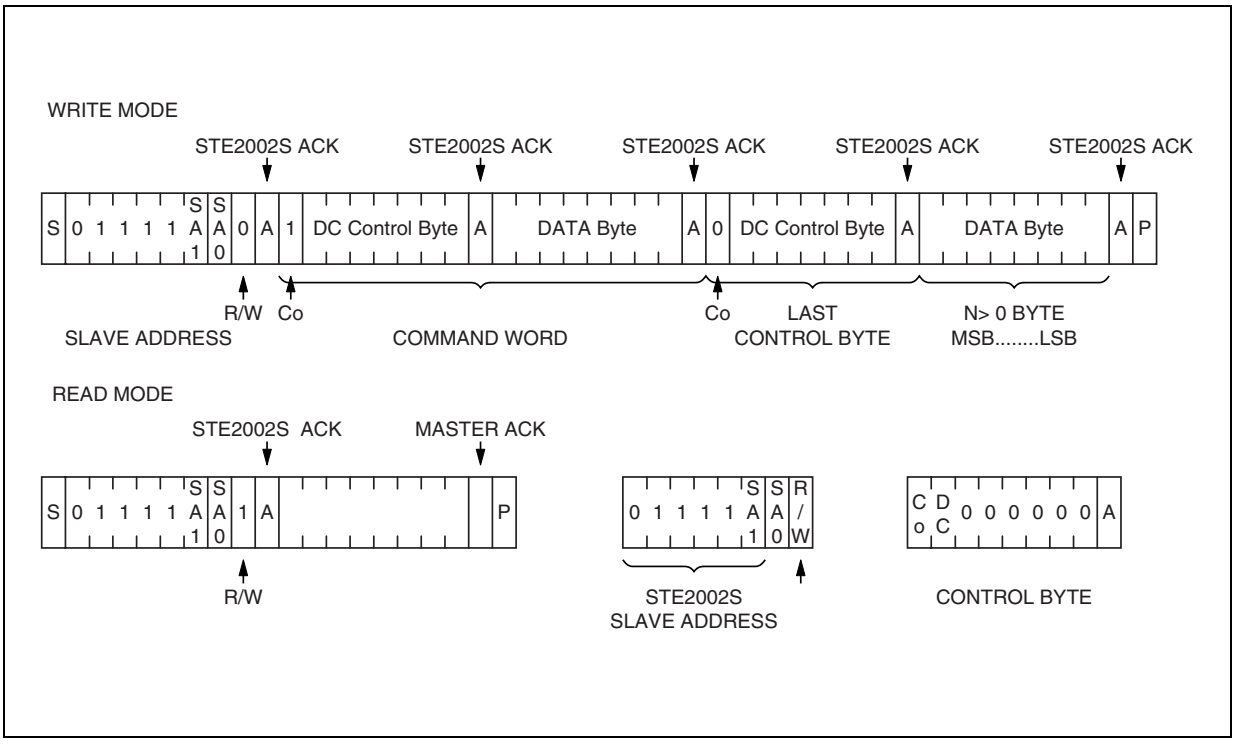
If the R/W bit is set to logic 0 the STE2002S is set to be a receiver. After the slaves acknowledge one or more command word follows to define the status of the device.

A command word is composed by two bytes. The first is a control byte which defines the Co and D/$\overline{C}$ values, the second is a data byte (fig 31). The Co bit is the command MSB and defines if after this command will follow one data byte and an other command word or if will follow a stream of data (Co = 1 Command word, Co = 0 Stream of data). The D/$\overline{C}$ bit defines whether the data byte is a command or RAM data (D/$\overline{C}$ = 1 RAM Data, D/$\overline{C}$ = 0 Command).
If Co =1 and D/$\overline{C}$ = 0 the incoming data byte is decoded as a command, and if Co =1 and D/$\overline{C}$ =1, the following data byte will be stored in the data RAM at the location specified by the data pointer.
Every byte of a command word must be acknowledged by all addressed units.
After the last control byte, if D/$\overline{C}$ is set to a logic 1 the incoming data bytes are stored inside the STE2002S Display RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.
Every byte must be acknowledged by all addressed units.

7.1.1.2 Reading Mode.

If the R/W bit is set to logic 1 the chip will output data immediately after the slave address. If the D/C bit sent during the last write access, is set to a logic 0, the byte read is the status byte.

Figure 31. Communication Protocol



7.2 SERIAL INTERFACE

The STE2002S serial Interface is a bidirectional link between the display driver and the application supervisor.

It consists of five lines: two for data signals (SDIN, SOUT), one for clock signals (SCLK), one for the peripheral enable ($\overline{SCE}$) and one for mode selection (SD/$\overline{C}$).

The serial interface is active only if the SCE line is set to a logic 0. When $\overline{SCE}$ line is high the serial peripheral power consumption is zero. While $\overline{SCE}$ pin is high the serial interface is kept in reset.

The STE2002S is always a slave on the bus and receive the communication clock on the SCLK pin from the master.

Information are exchanged byte-wide. During data transfer, the data line is sampled on the positive SCLK edge.

SD/$\overline{C}$ line status indicates whether the byte is a command (SD/$\overline{C}$ =0) or RAM data (SD/$\overline{C}$ =1);it is read on the eighth SCLK clock pulse during every byte transfer.

If $\overline{SCE}$ stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next byte at the next SCLK positive edge.

A reset pulse on $\overline{RES}$ pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.

If $\overline{SCE}$ is low after the positive edge of $\overline{RES}$, the serial interface is ready to receive data.

Throughout SOUT can be read only the driver I^2C slave address. The Command sequence that allows to read I^2C slave address is reported in Fig. 34 & 35. SOUT is in High impedance in steady state and during data write. It is possible to short circuit DOUT and SDIN and read I2C address without any additional lines.

Figure 32. Serial bus protocol - one byte transmission

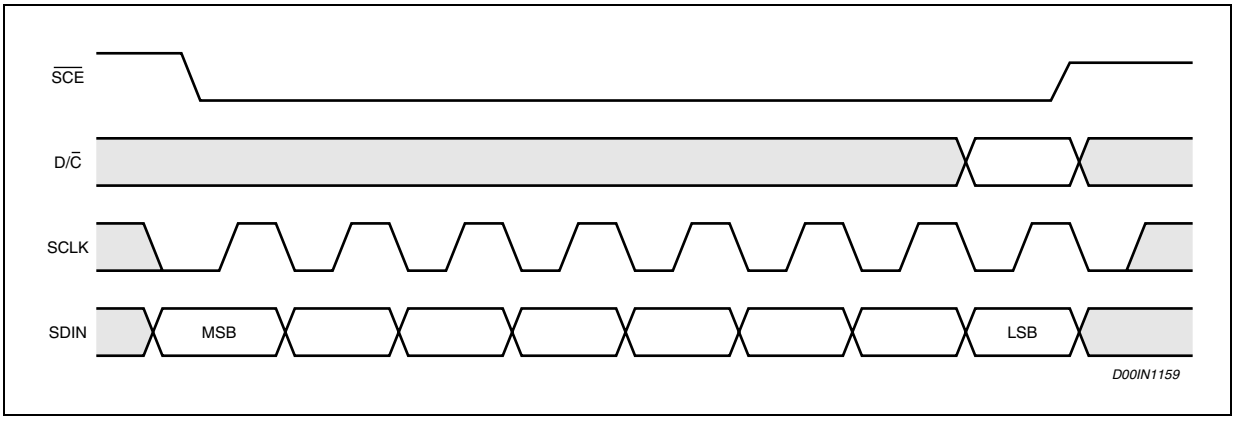


Figure 33. Serial bus protocol - several byte transmission

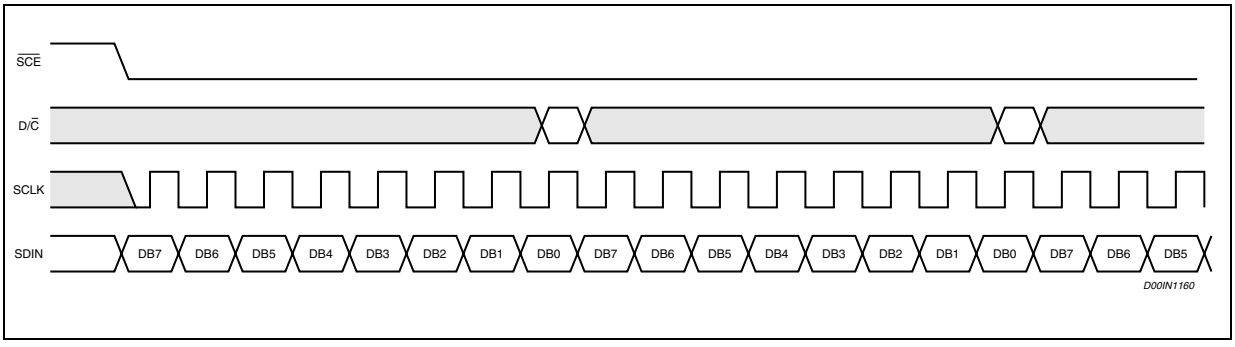


Figure 34. Serial bus protocol - several byte transmission

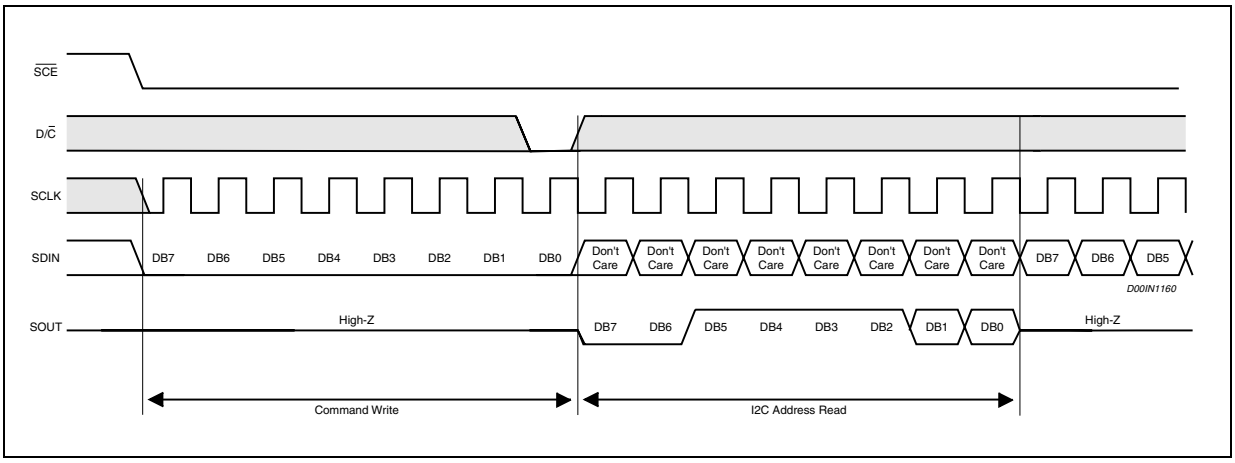
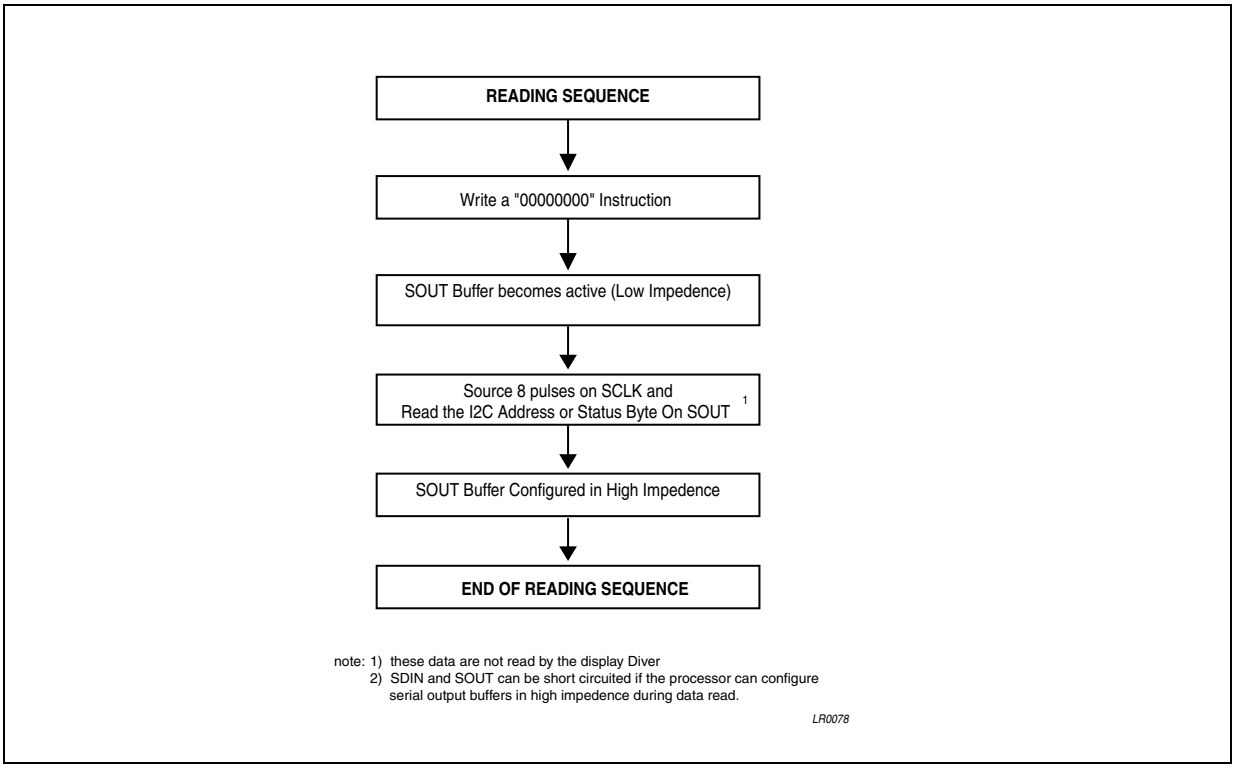


Figure 35. Reading Sequence



7.3 Parallel Interface

The STE2002S parallel Interface is a bidirectional link between the display driver and the application supervisor. It consists of eleven lines: eight data lines (from DB7 to DB0) and three control lines. The control lines are: enable (E) for data latch, PD/$\overline{C}$ for mode selection and R/$\overline{W}$ for reading or writing.

The data lines and the control line values are internally latched on E rising edge (fig. 50).

When the parallel interface is selected, if R/W line is set to “one”, D0-D7 lines are configured as output drivers (low impedence) and it is possible to read the driver I^2C address (Fig. 51)

Table 7. STE2001-like instruction Set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H=0 or H=1											
	0	0	0	0	0	0	0	0	0	0	Read I^2C Address (with Serial Interface only)
Function Set	0	0	0	0	1	MX	MY	PD	V	H[0]	Power Down Management; Entry Mode;
Read Status Byte	0	1	PD	A1	A2	D	E	MX	MY	DO	(I^2C interface only)
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=0											
Memory Blank	0	0	0	0	0	0	0	0	0	1	Starts Memory Blank Procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one Row UP or DOWN
V_{LCD} Range Setting	0	0	0	0	0	0	0	1	0	PRS [0]	V_{LDC} programming range selection
Display Control	0	0	0	0	0	0	1	D	0	E	Select Display Configuration
Set CP Factor	0	0	0	0	0	1	0	S2	S1	S0	Charge Pump Multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set Horizontal (Y) RAM Address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set Vertical (X) RAM Address
H=1											
Checker Board	0	0	0	0	0	0	0	0	0	1	Starts Checker Board Procedure
Multiplex Select	0	0	0	0	0	0	0	0	1	MUX	Selects MUX factor
TC Select	0	0	0	0	0	0	0	1	TC1	TC0	Set Temperature Coefficient for V_{LDC}
Output Address	0	0	0	0	0	0	1	DO	A1	A2	No function
Bias Ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired Bias Ratios
Reserved	0	0	0	1	X	X	X	X	X	X	Not to be used
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register Write instruction

Table 8. Extended Instruction Set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H Independent Instructions											
NOP	0	0	0	0	0	0	0	0	0	0	Read I^2C Address (with Serial Interface only)
Function Set	0	0	0	0	1	MX	MY	PD	H[1]	H[0]	Power Down Management; Entry Mode; Extended Instruction Set
Read Status Byte	0	1	PD	0	0	D	E	MX	MY	DO	(I^2C interface only)
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=[0;0] RAM Commands											
Memory Blank	0	0	0	0	0	0	0	0	0	1	Starts Memory Blank Procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one Row UP or DOWN
V_{LCD} Range Setting	0	0	0	0	0	0	0	1	PRS [1]	PRS [0]	V_{LDC} programming range selection
Display Control	0	0	0	0	0	0	1	D	0	E	Select Display Configuration
Set CP Factor	0	0	0	0	0	1	0	S2	S1	S0	Charge Pump Multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set Horizontal (Y) RAM Address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set Vertical (X) RAM Address
H=[0;1]											
Checker Board	0	0	0	0	0	0	0	0	0	1	Starts Checker Board Procedure
	0	0	0	0	0	0	0	0	1	V	Vertical Addressing Mode
TC Select	0	0	0	0	0	0	0	1	TC1	TC0	Set Temperature Coefficient for V_{LDC}
Data Format	0	0	0	0	0	0	1	DO	0	0	MSB Position
Bias Ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired Bias Ratios
	0	0	0	1	X	X	X	X	X	X	Reserved
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register Write instruction
H=[1;0]											
Soft Reset	0	0	0	0	0	0	0	0	0	1	Software RESET
Partial Enable	0	0	0	0	0	0	0	0	1	PE	Partial Enable
Frame Rate	0	0	0	0	0	0	0	1	FR1	FR0	Frame rate Control
Multiple Select	0	0	0	0	0	0	1	0	M[1]	M[0]	Mux Ratio
Partial Mode	0	0	0	0	0	1	0	PD2	PD1	PD0	Partial Display Config
1st Sector Start	0	0	0	1	PDY 5	PDY 4	PDY 3	PDY 2	PDY 1	PDY 0	1^{st} Sector Start Address
2nd Sector Start	0	0	1	PDY 6	PDY 5	PDY 4	PDY 3	PDY 2	PDY 1	PD Y0	2^{nd} Sector Start Address
H=[1;1]											
Pointer Reset	0	0	0	0	0	0	0	0	0	1	Scrolling Pointer Reset
	0	0	0	0	0	0	0	0	1	X	Not Used
	0	0	0	0	0	0	0	1	X	X	Not Used
TC Select	0	0	0	0	0	0	1	T2	T1	T0	Set Temperature Coefficient for V_{LDC}
	0	0	0	0	0	1	X	X	X	X	Not Used
Y - Carriage	0	0	0	1	0	0	YC-3	YC-2	YC-1	YC-0	Y-CARRIAGE RETURN
X - Carriage	0	0	1	XC-6	XC-5	XC-4	XC-3	XC-2	XC-1	XC-0	X CARRIAGE RETURN

Table 9. Explanations of Table 2 symbols

BIT	0	1	RESET STATE
DIR	Scroll by one down	Scroll by one up	
PD	Device fully working	Device in power down	1
V	Horizontal addressing	Vertical addressing	0
MX	Normal X axis addressing	X axis address is mirrored.	0
MY	Image is displayed not vertically mirrored	Image is displayed vertically mirrored	0
DO	MSB on TOP	MSB on BOTTOM	0
PE	Partial Display disabled	Partial Display enabled	0
H[0]	Select page 0	Select page 1	0
MUX	MUX 65	MUX 33	0

Table 10. PAGE NUMBER

H[1]	H[0]	DESCRIPTION	RESET STATE
0	0	Page 0	Page 0
0	1	Page 1	
1	0	Page 2	
1	1	Page 3	

Table 11. DISPLAY MODE

D	E	DESCRIPTION	RESET STATE
0	0	display blank	D=0 E=0
0	1	all display segments on	
1	0	normal mode	
1	1	inverse video mode	

Table 12. FRAME RATE CONTROL

FR[1]	FR[0]	DESCRIPTION	RESET STATE
0	0	65Hz	75Hz
0	1	70Hz	
1	0	75Hz	
1	1	80Hz	

Table 13. VLCD RANGE SELECTION

PRS[1]	PRS[0]	DESCRIPTION	RESET STATE
0	0	2.94	
0	1	6.78	
1	0	10.62	
1	1	Not Used	

Table 14. MULTIPLEXING RATIO

M[1]	M[0]	DESCRIPTION	RESET STATE
0	0	49	01
0	1	65	
1	0	81	
1	1	Not Used	

Table 15. TEMPERATURE COEFFICIENT

T2	T1	T0	DESCRIPTION	RESET STATE
0	0	0	VLCD temperature Coefficient 0	000
0	0	1	VLCD temperature Coefficient 1	
0	1	0	VLCD temperature Coefficient 2	
0	1	1	VLCD temperature Coefficient 3	
1	0	0	VLCD temperature Coefficient 4	
1	0	1	VLCD temperature Coefficient 5	
1	1	0	VLCD temperature Coefficient 6	
1	1	1	VLCD temperature Coefficient 7	

Table 16.

TC1	TC0	DESCRIPTION	RESET STATE
0	0	VLCD temperature Coefficient 0	00
0	1	VLCD temperature Coefficient 2	
1	0	VLCD temperature Coefficient 3	
1	1	VLCD temperature Coefficient 6	

Table 17. CHARGE PUMP MULTIPLICATION FACTOR

CP2	CP1	CP0	DESCRIPTION	RESET STATE
0	0	0	Multiplication Factor X2	000
0	0	1	Multiplication Factor X3	
0	1	0	Multiplication Factor X4	
0	1	1	Multiplication Factor X5	
1	0	0	Multiplication Factor X6	
1	0	1	NOT USED	
1	1	0	NOT USED	
1	1	1	AUTOMATIC	

Table 18. BIAS RATIO

BS2	BS1	BS0	DESCRIPTION	RESET STATE
0	0	0	Bias Ratio equal to 7	000
0	0	1	Bias Ratio equal to 6	
0	1	0	Bias Ratio equal to 5	
0	1	1	Bias Ratio equal to 4	
1	0	0	Bias Ratio equal to 3	
1	0	1	Bias Ratio equal to 2	
1	1	0	Bias Ratio equal to 1	
1	1	1	Bias Ratio equal to 0	

Table 19. Y CARRIAGE RETURN REGISTER

Y-C[3]	Y-C[2]	Y-C[1]	Y-C[0]	DESCRIPTION	RESET STATE
0	0	0	0		1000
0	0	0	1	Y-CARRIAGE =1	
0	0	1	0	Y-CARRIAGE =2	
0	0	1	1	Y-CARRIAGE =3	
0	1	0	0	Y-CARRIAGE =4	
0	1	0	1	Y-CARRIAGE =5	
.	.	.	.		
1	0	1	0	Y-CARRIAGE =10	

Table 20. PARTIAL DISPLAY CONFIGURATION

PD2	PD1	PD0	SECTION 1	SECTION2 (*)	RESET STATE
0	0	0	0	8 + Icon Row	000
0	0	1	8	0 + Icon Row	
0	1	0	8	8 + Icon Row	
0	1	1	0	16 + Icon Row	
1	0	0	16	0 + Icon Row	
1	0	1	8	16 + Icon Row	
1	1	0	16	8 + Icon Row	
1	1	1	16	16 + Icon Row	

(*) section2=y if Icon=0; section2=y+Icon if Icon=1

Figure 36. Host Processor Interconnection with I²C Interface

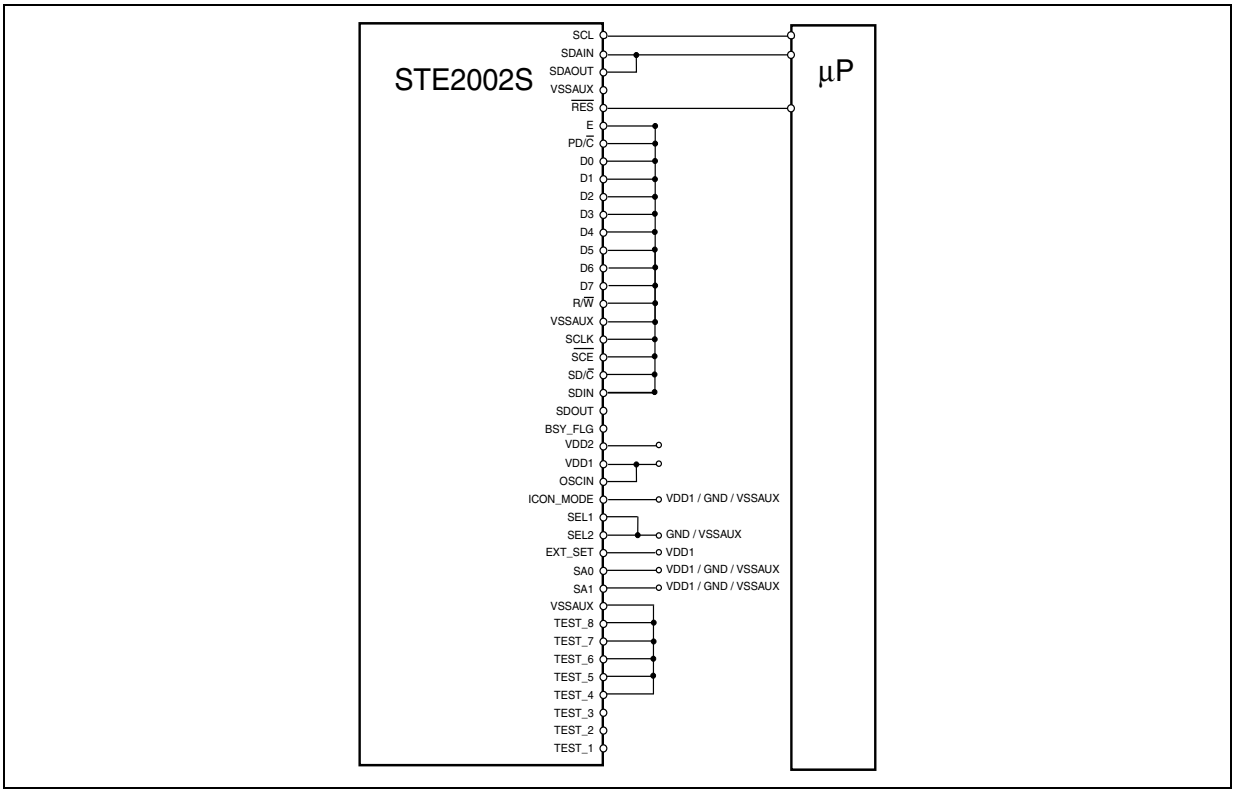


Figure 37. Host Processor Interconnection with Serial Interface

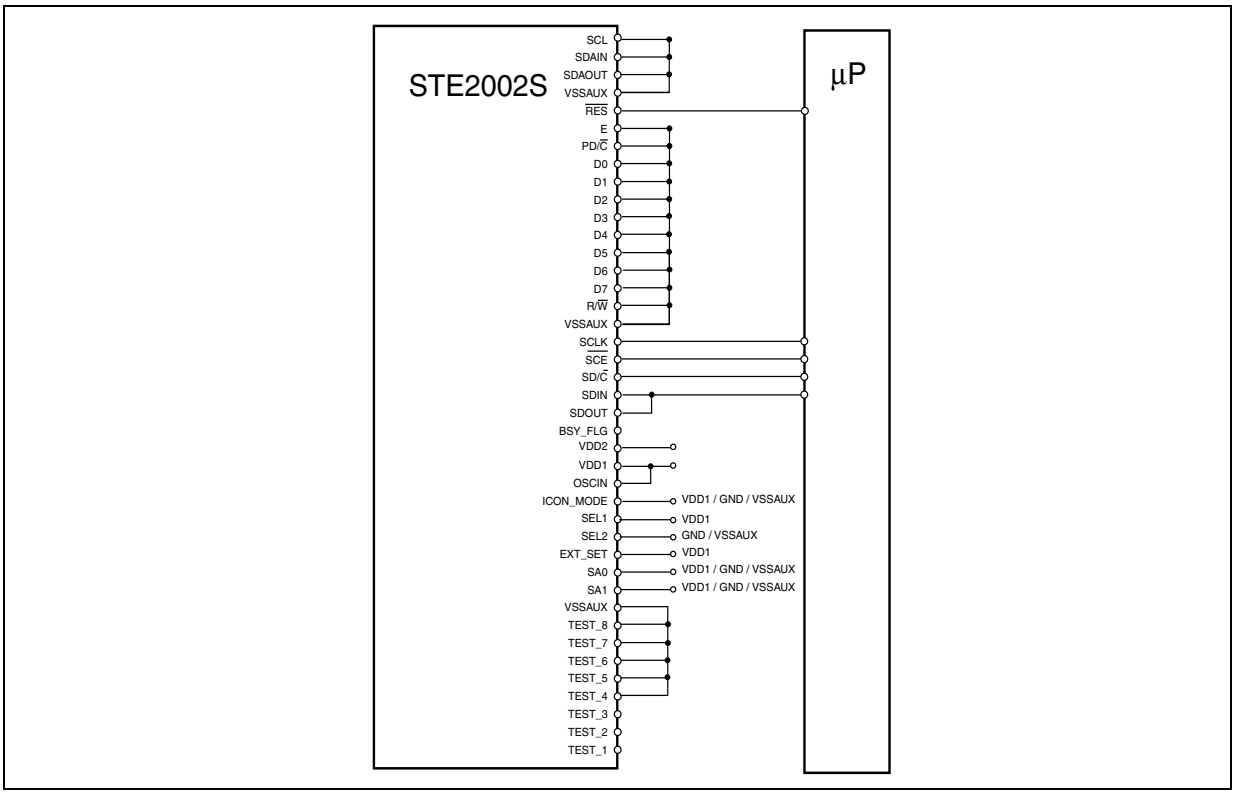


Figure 38. Host Processor Interconnection with Parallel Interface

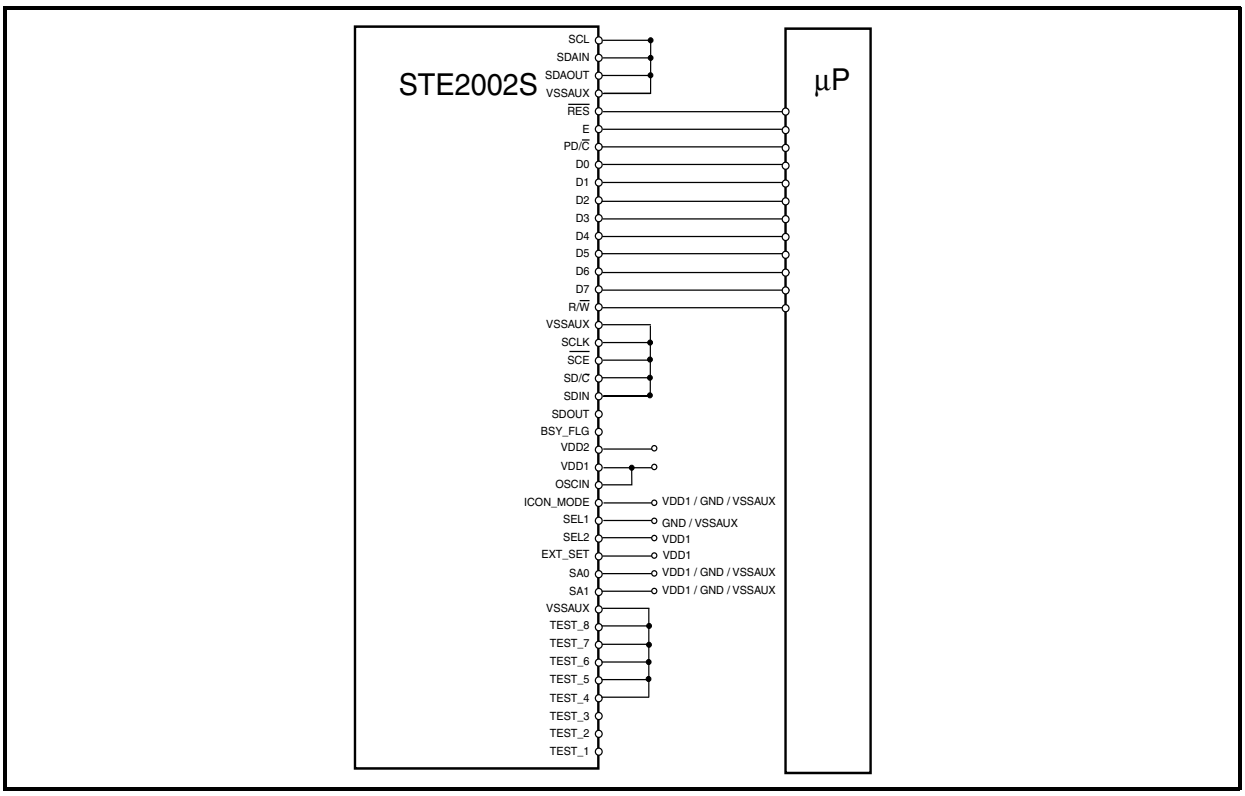


Figure 39. Application Schematic Using an External LCD Voltage Generator

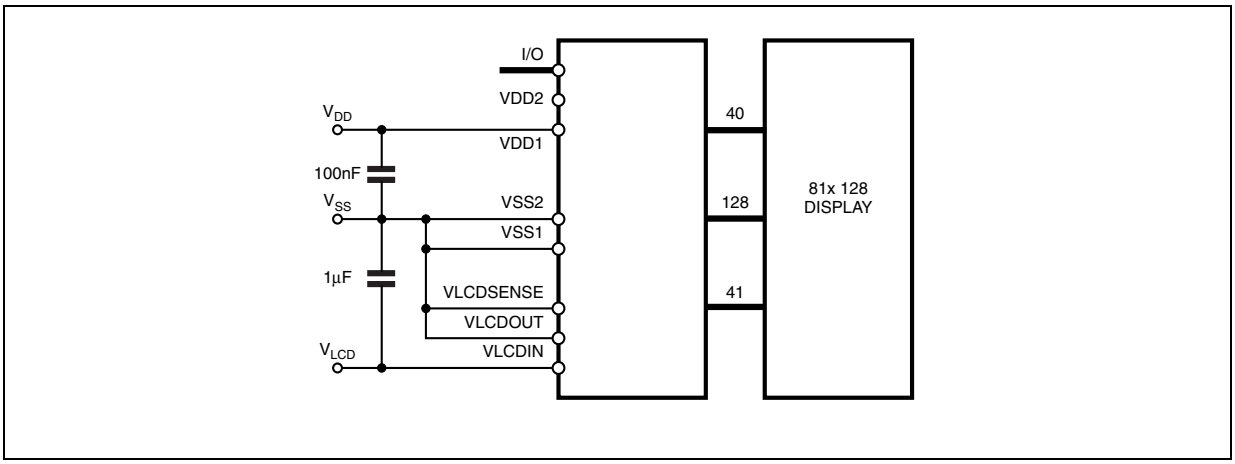


Figure 40. Application Schematic using the Internal LCD Voltage Generator and two separate supplies

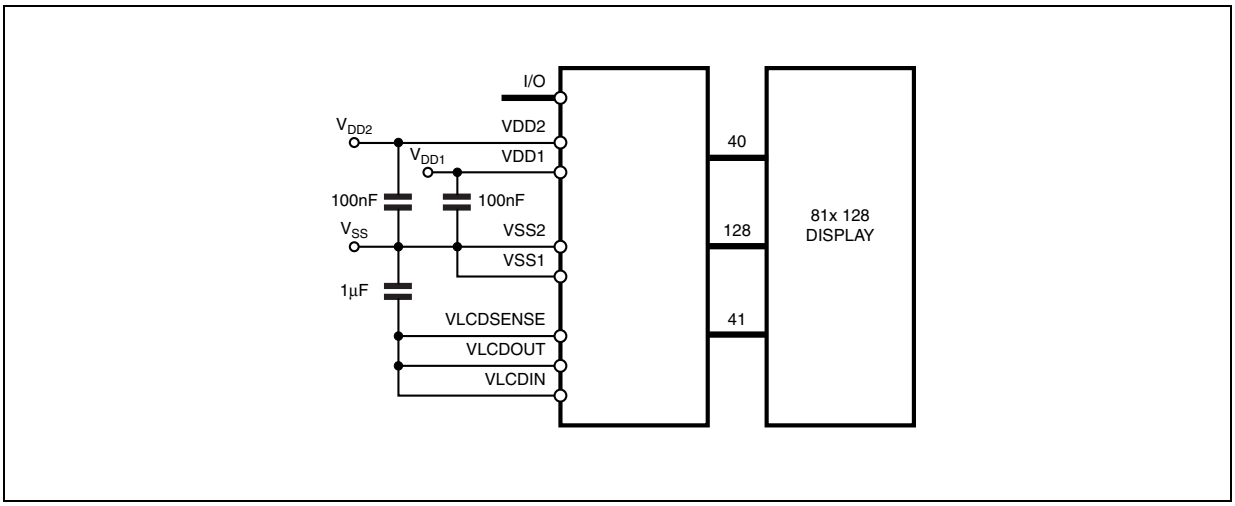


Figure 41. Application Schematic using the Internal LCD Voltage Generator and a single supply

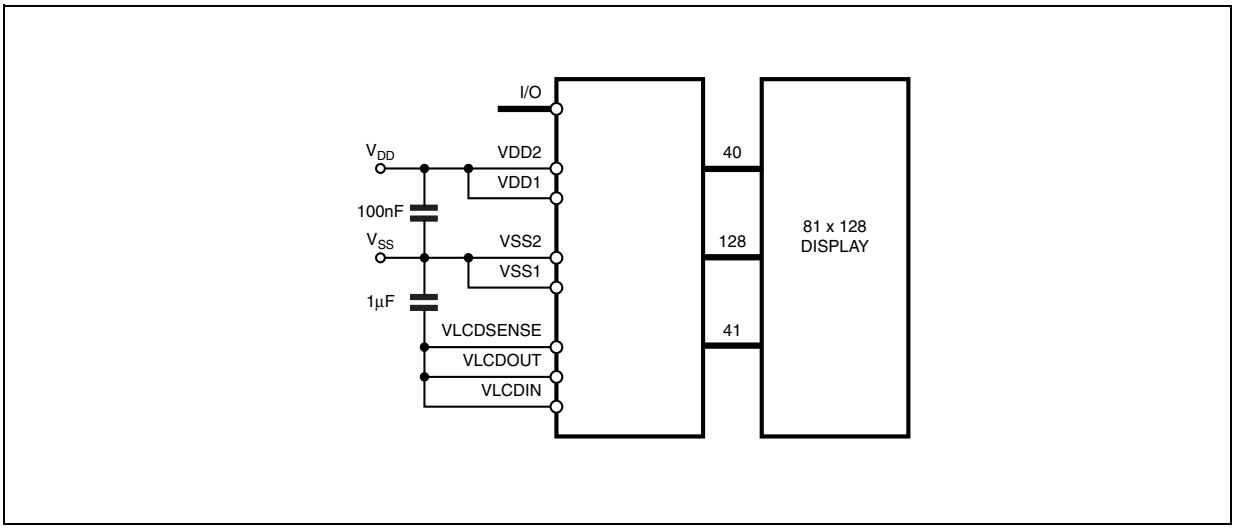


Figure 42. Power-Up sequence

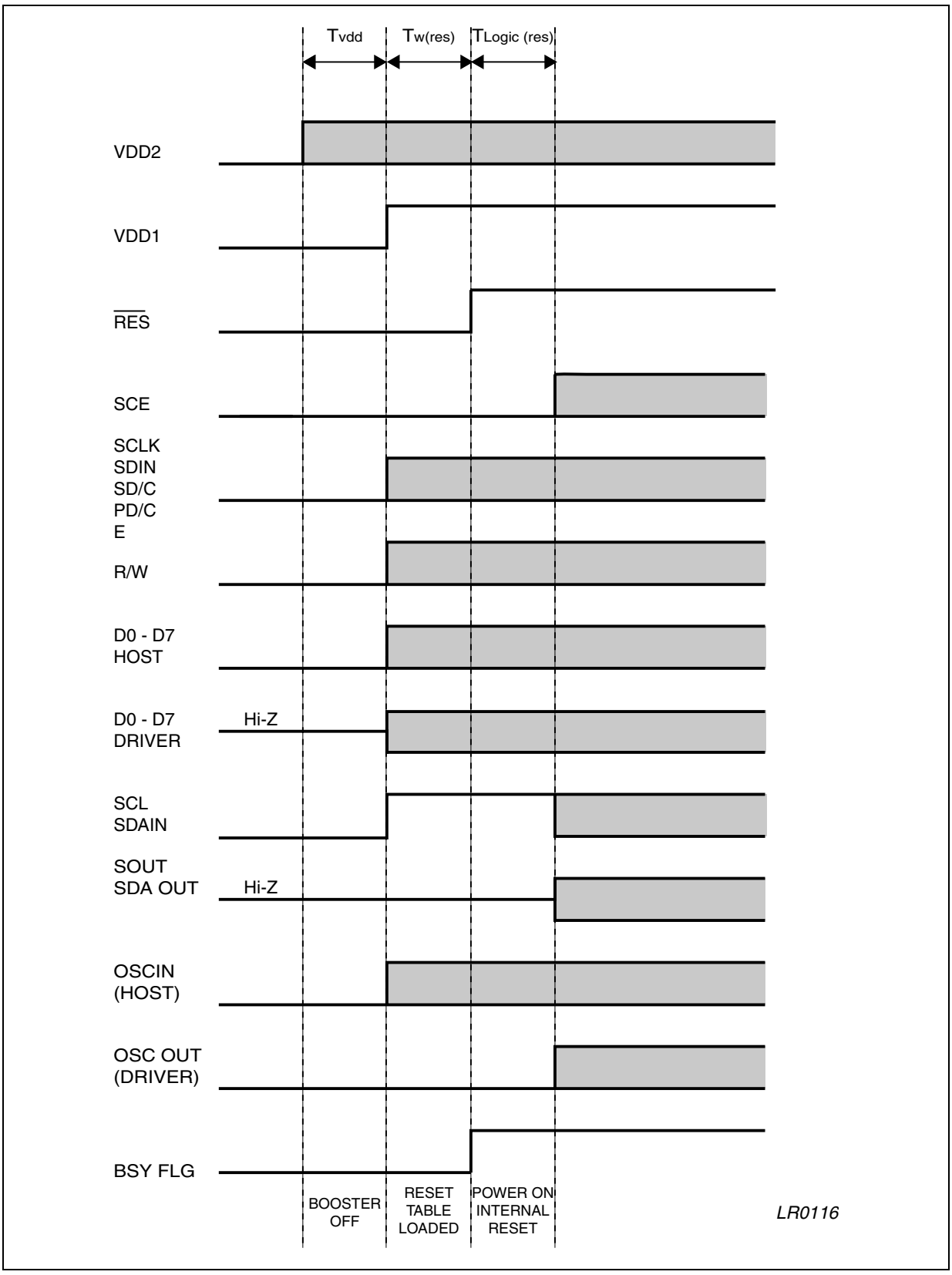


Figure 43. Power-OFF Sequence

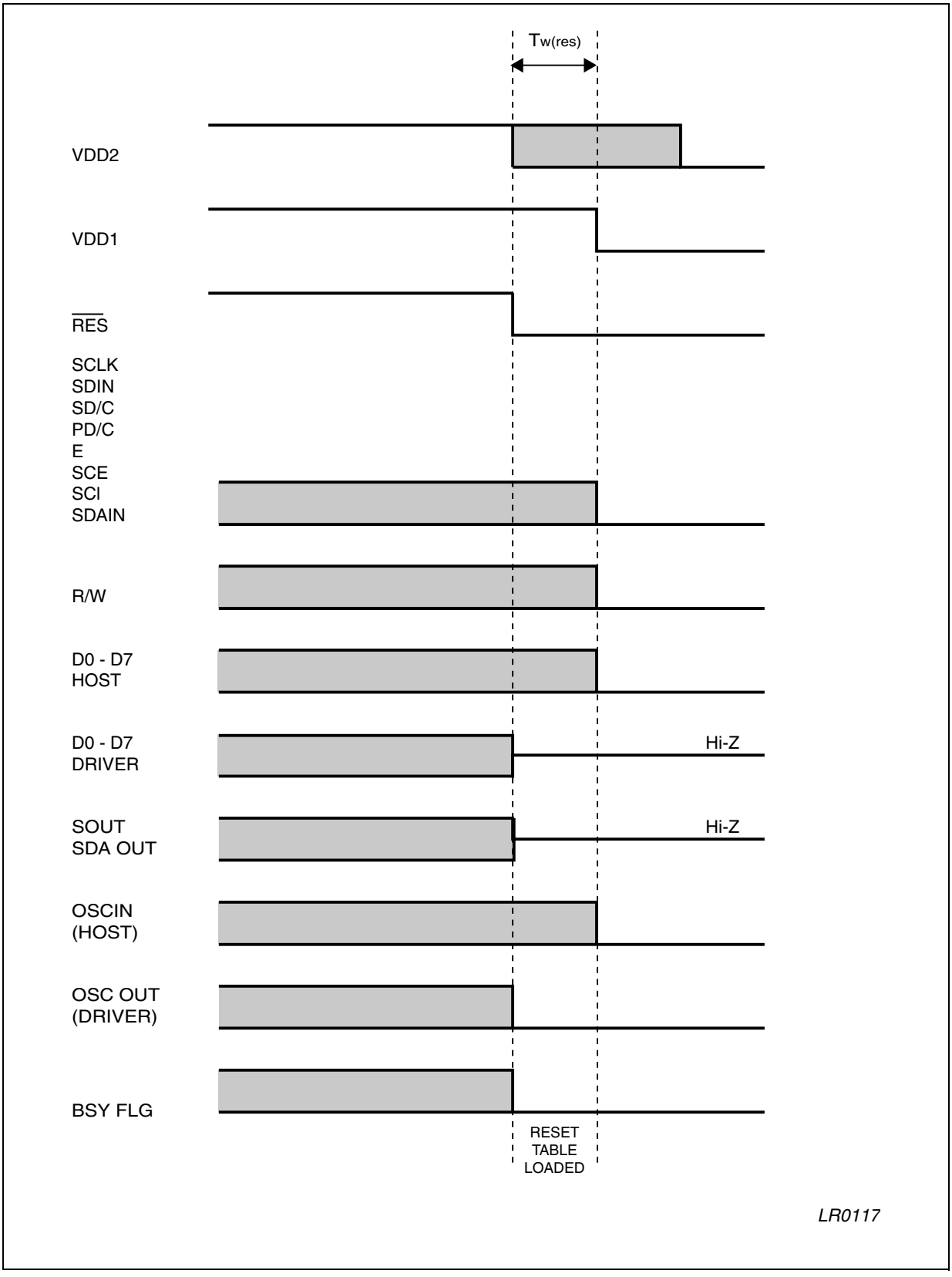


Figure 44. Initialization with built-in Booster

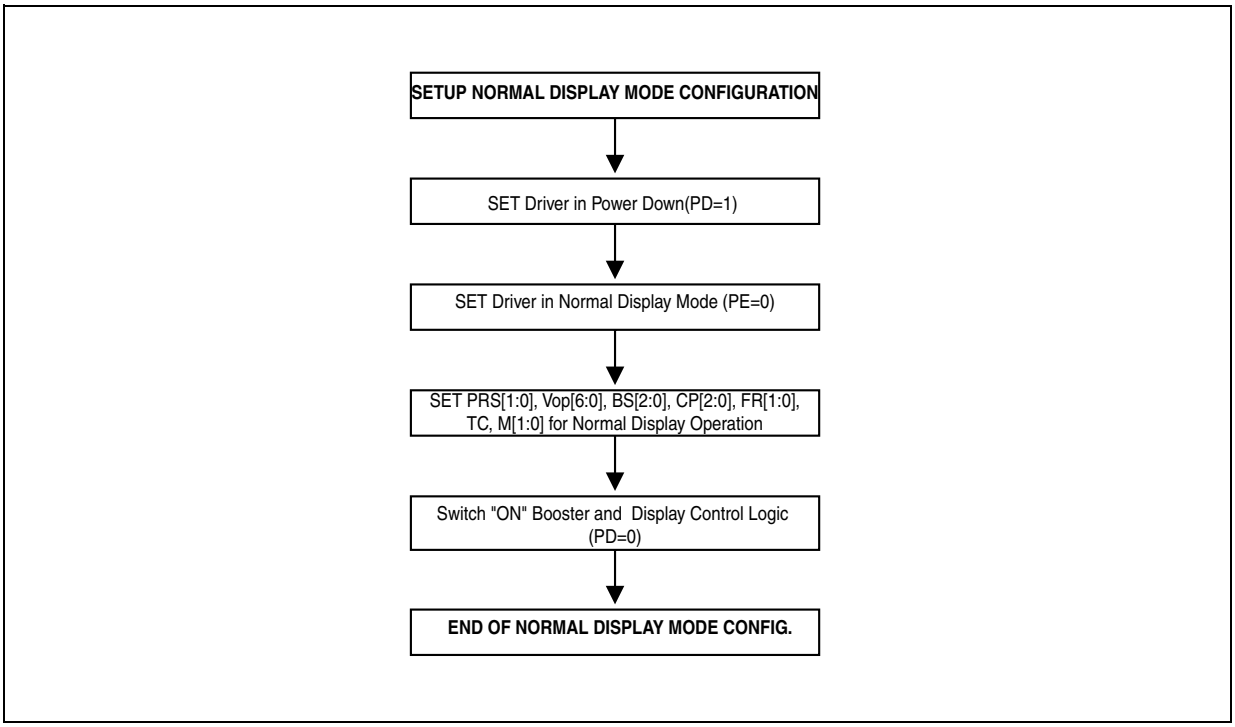


Figure 45. Dual Partial Display Enabling Instruction Flow

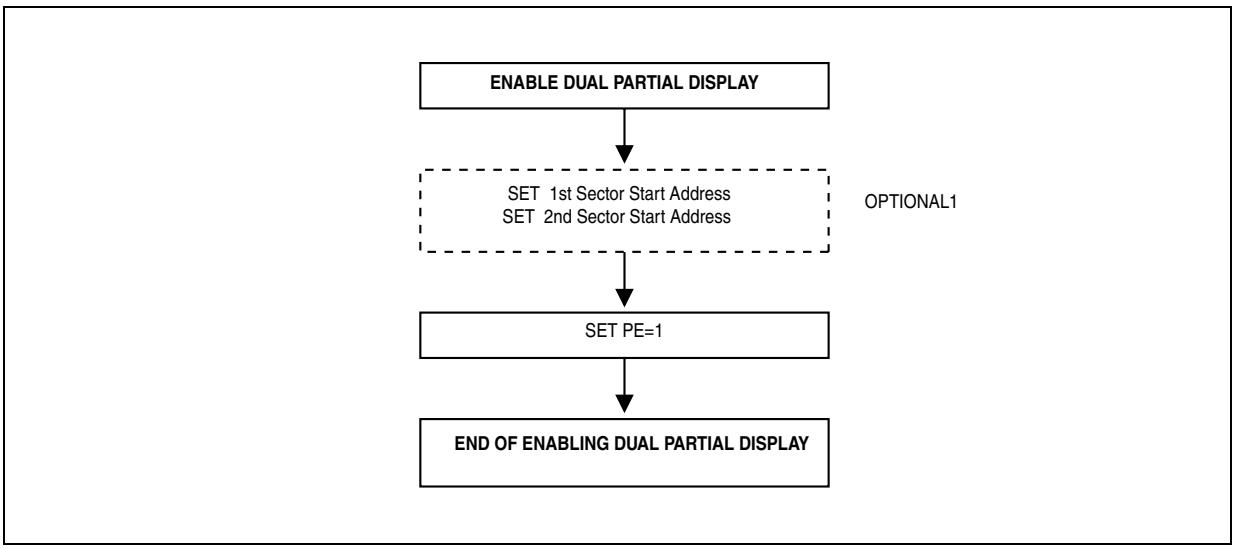


Figure 46. Dual Partial Display Mode configuration or Duty Change

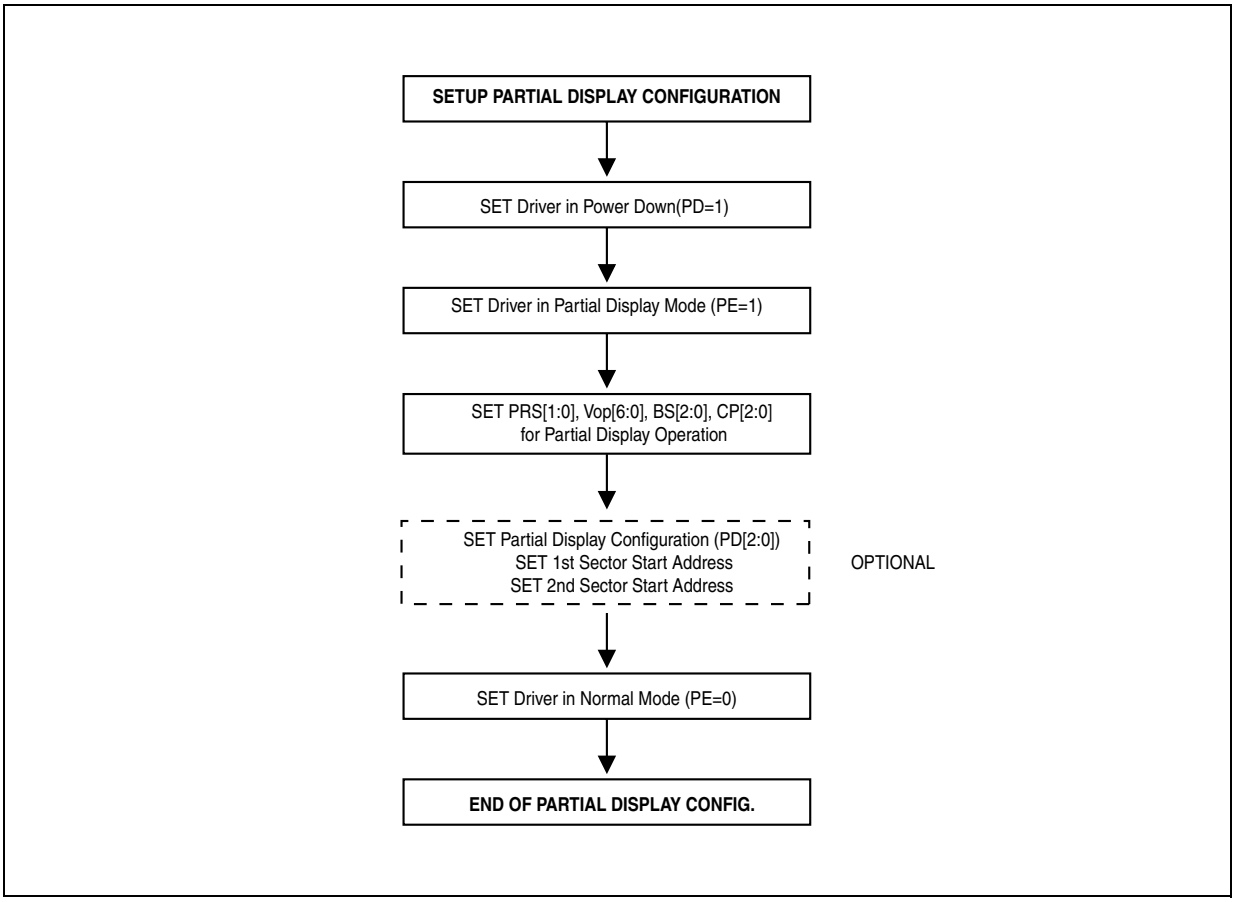


Figure 47. DATA RAM to display Mapping

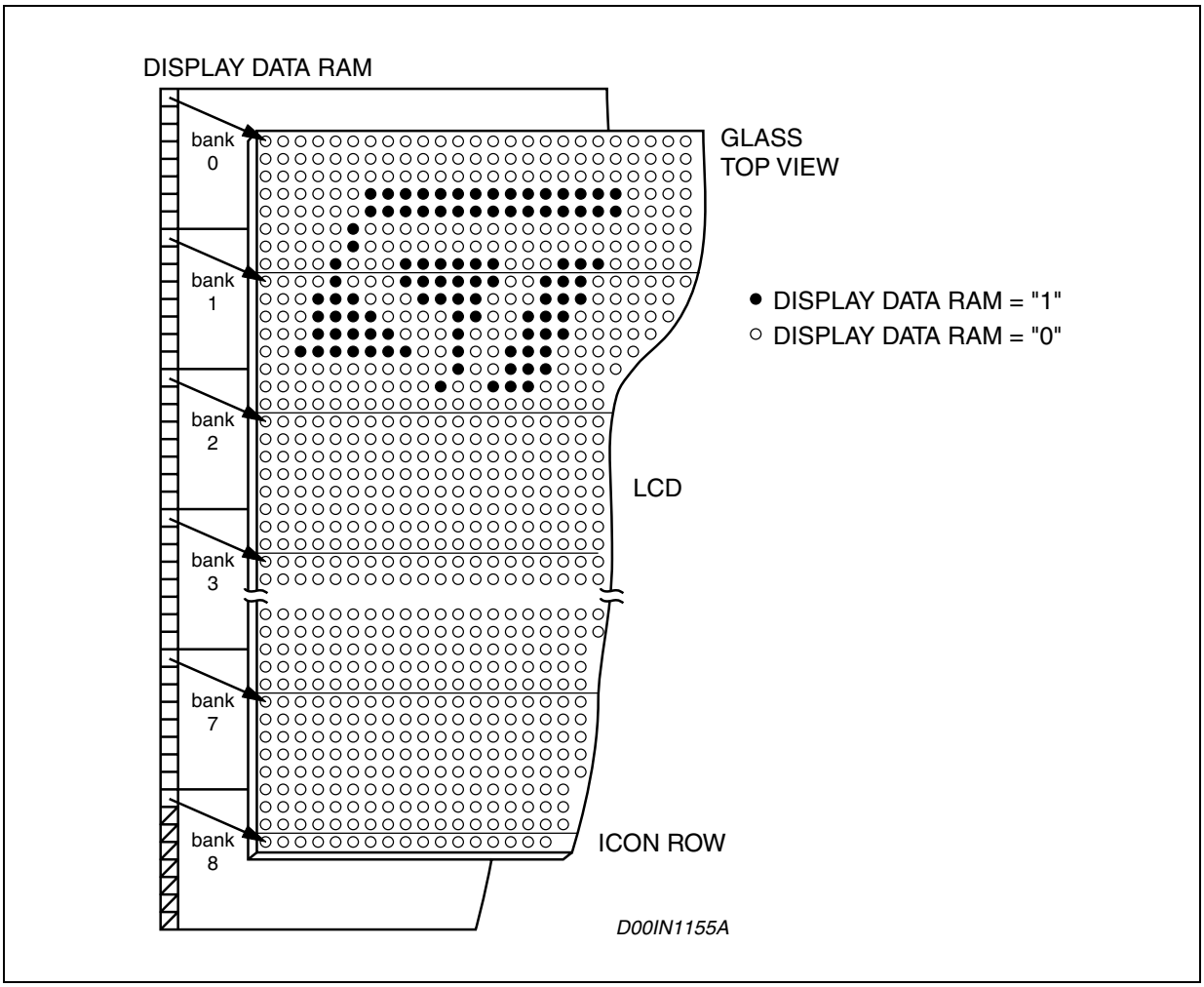


Table 21. Test Pin Configuration

Pad_name	Pin_configuration
TEST_1	OPEN
TEST_2	OPEN
TEST_3	OPEN
TEST_4	VSS/VSSAUX
TEST_5	VSS/VSSAUX
TEST_6	VSS/VSSAUX
TEST_7	VSS/VSSAUX
TEST_8	VSS/VSSAUX
TEST_9	VSS/VSSAUX
TEST_10	VSS/VSSAUX
TEST_11	VSS/VSSAUX
TEST_12	VSS/VSSAUX

8 ELECTRICAL SPECIFICATIONS

Table 22. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD1}	Supply Voltage Range	- 0.5 to + 5	V
V_{DD2}	Supply Voltage Range	- 0.5 to + 7	V
V_{LCD}	LCD Supply Voltage Range	- 0.5 to + 15	V
I_{SS}	Supply Current	- 50 to +50	mA
V_i	Input Voltage (all input pads)	-0.5 to V_{DD2} + 0.5	V
I_{in}	DC Input Current	- 10 to + 10	mA
I_{out}	DC Output Current	- 10 to + 10	mA
P_{tot}	Total Power Dissipation (T_j = 85°C)	300	mW
P_o	Power Dissipation per Output	30	mW
T_j	Operating Junction Temperature	-40 to + 85	°C
T_{stg}	Storage Temperature	- 65 to 150	°C

Table 23. Electrical Characteristics - DC OPERATION

(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13 V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltages						
V_{DD1}	Supply Voltage	note 9	1.7		3.6	V
V_{DD2}	Supply Voltage	LCD Voltage Internally generated	2.4		4.2	V
V_{LCDIN}	LCD Supply Voltage	LCD Voltage Supplied externally	4.5		13	V
V_{LCDOUT}	LCD Supply Voltage	Internally generated; note 1	4.5		13	V
$I(V_{DD1})$	Supply Current	V_{DD1} = 2.8V; V_{LCD} = 10V; f_{sclk} = 0;T_{amb} = 25°C; note 3.	15	20	40	µA
		V_{DD1} = 2.8V; V_{LCD} = 10V; f_{sclk} = 1Mhz;T_{amb} = 25°C; note 3, 8. OSC_IN=GND; parallel port		120	200	µA
$I(V_{DD2})$	Voltage Generator Supply Current	with V_{OP} = 0 and PRS = [0:0] with external V_{LCD}			1	µA
		V_{DD2}= 2.8V;V_{LCD}=10V; f_{sclk}= 0; T_{amb} = 25°C; no display load; 5x charge pump; note 2,3,6,	10		40	µA
$I(V_{DD1,2})$	Total Supply Current	V_{DD1},V_{DD2}= 2.8V; V_{LCD} = 10V; 5x charge pump; f_{sclk} = 0;T_{amb} = 25°C; no display load; note 2,3,6	25		80	µA
		Power down Mode with internal or External VLCD. Note 4		3	10	µA
$I(V_{LDCIN})$	External LCD Supply Voltage Current	V_{DD} =2.8V; V_{LCD} =10V;no display load; f_{sclk} = 0; T_{amb} = 25°C; note 3.	5	10	15	µA
Logic Outputs						
V_{0H}	High logic Level Output Voltage	IOH=-500µA	0.8V_{DD1}		V_{DD1}	V
V_{OL}	Low logic Level Output Voltage	IOL=500µA	V_{SS}		0.2V_{DD1}	V

Table 23. Electrical Characteristics - DC OPERATION (continued)
(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13 V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Logic Inputs						
V_{IL}	Logic LOW voltage level		V_{SS}		$0.3V_{DD1}$	V
V_{IH}	Logic HIGH Voltage Level		$0.7V_{DD1}$		V_{DD2}	V
I_{in}	Input Current	V_{in} = V_{SS1} or V_{DD1}	-1		1	µA
Logic Inputs/Outputs						
V_{IL}	Logic LOW voltage level		V_{SS}		$0.3V_{DD1}$	V
V_{IH}	Logic HIGH Voltage Level		$0.7V_{DD1}$		V_{DD1} +0.5V	V
Column and Row Driver						
R_{row}	ROW Output Resistance	V_{LCD} = 10V;		3K	5K	kohm
R_{col}	Column Output resistance	V_{LCD} = 10V;		5K	10K	kohm
V_{col}	Column Bias voltage accuracy	No load	-50		+50	mV
V_{row}	Row Bias voltage accuracy		-50		+50	mV
LCD Supply Voltage						
V_{LCD}	LCD Supply Voltage accuracy; Internally generated	V_{DD} = 2.8V; V_{LCD} = 10V; fsclk=0; T_{amb}=25°C; no display load; note 2, 3, 6 & 7; VOP = 61h, PRS = 2hex	-2.2		2.2	%
TC0	Temperature coefficient			$-0.0 \cdot 10^{-3}$		1/°C
TC1				$-0.35 \cdot 10^{-3}$		1/°C
TC2				$-0.7 \cdot 10^{-3}$		1/°C
TC3				$-1.05 \cdot 10^{-3}$		1/°C
TC4				$-1.4 \cdot 10^{-3}$		1/°C
TC5				$-1.75 \cdot 10^{-3}$		1/°C
TC6				$-2.1 \cdot 10^{-3}$		1/°C
TC7				$-2.3 \cdot 10^{-3}$		1/°C

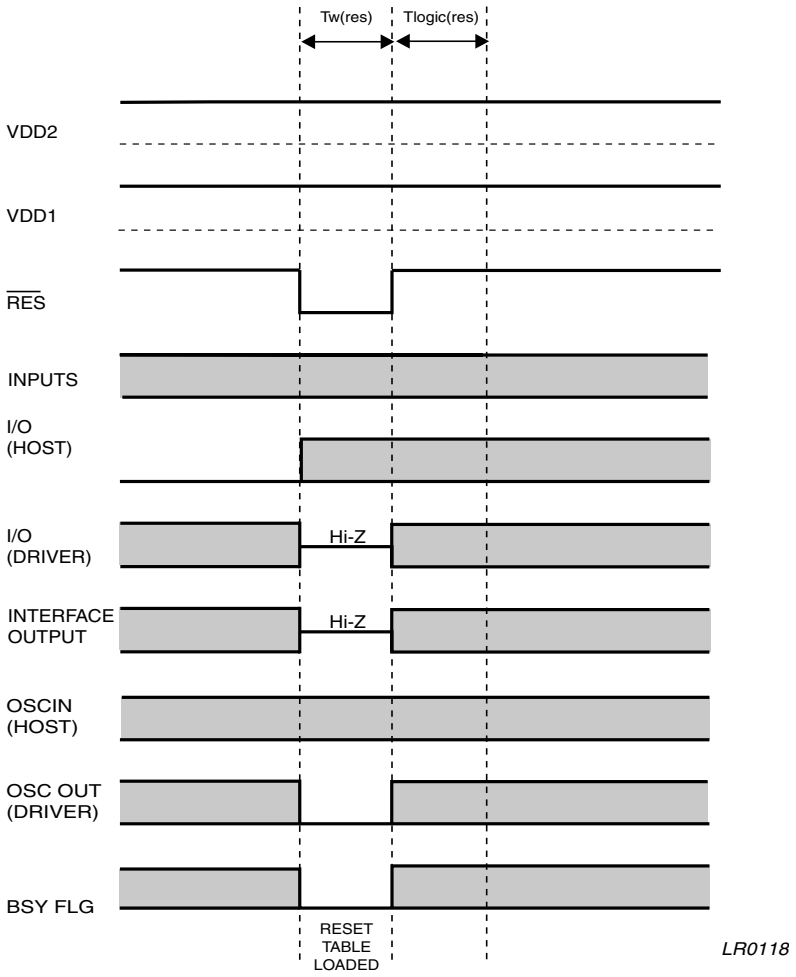
Notes: 1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. When f_{sclk} = 0 there is no interface clock.
4. Power-down mode. During power-down all static currents are switched-off.
5. f external V_{LCD}, the display load current is not transmitted to I_{DD}
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27°C), maximum tolerance values are measured at the temperature range limit.
7. For TC0 to TC7
8. Data Byte Writing Mode
9. $V_{DD1} \leq V_{DD2}$

Table 24. Electrical Characteristics - AC OPERATION

(V_{DD1} = 1.7 to 3.6V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INTERNAL OSCILLATOR						
F_{OSC}	Internal Oscillator frequency	V_{DD} = 2.8V; Tamb = -20 to +70 °C	61	72	83	kHz
F_{EXT}	External Oscillator frequency		20		100	kHz
F_{FRAME}	Frame frequency	fosc or fext = 72 kHz; note 1		75		Hz
$T_{w(RES)}$	$\overline{RES}$ LOW pulse width		5			µs
	Reset Pulse Rejection				1	µs
T_{LOGIC} (RES)	Internal Logic Reset Time				5	µs
T_{VDD}	V_{DD1} vs. V_{DD2} Delay		0			µs

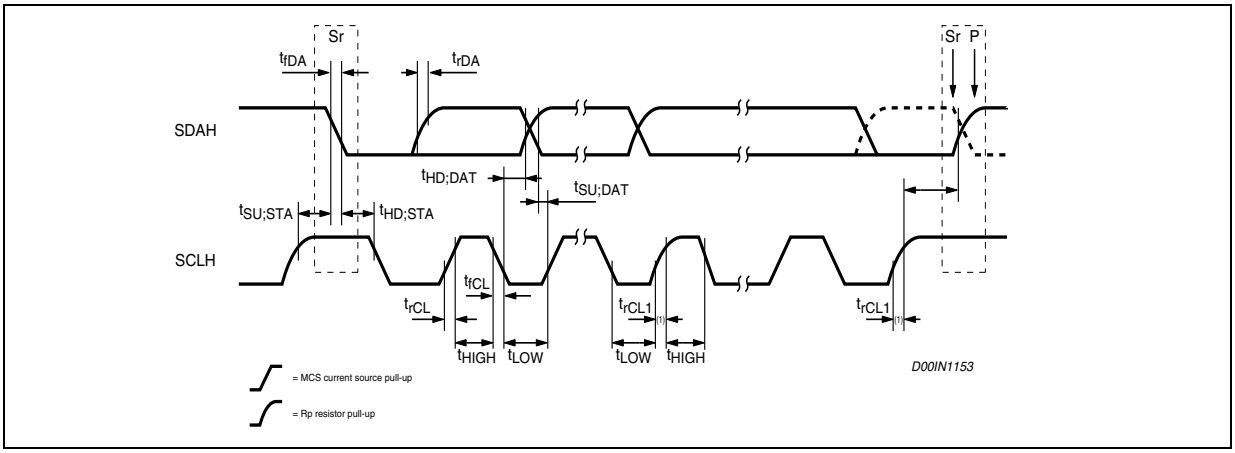
Table 25. RESET timing diagram



Electrical Characteristics - AC OPERATION (continued)
(V_{DD1} = 1.7 to 3.6V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I^2C BUS INTERFACE (See note 4)						
F_{SCL}	SCL Clock Frequency	Fast Mode	DC		400	kHz
		High Speed Mode; Cb=100pF (max);VDD1=2	DC		3.4	MHz
		High Speed Mode; Cb=400pF (max); VDD1=2	DC		1.7	MHz
		Fast Mode; VDD1=1.7V			400	KHz
$T_{SU;STA}$	Set-up time (repeated) START condition	Note 2, 3, Cb=100pF	160			ns
$T_{HD;STA}$	Hold time (repeated) START condition	Note 2, 3, Cb=100pF	160			ns
T_{LOW}	LOW period of the SCLH clock	Note 2, 3, Cb=100pF	160			ns
T_{HIGH}	HIGH period of the SCLH clock	Note 2, 3, Cb=100pF	60			ns
$T_{SU;DAT}$	Data set-up time	Note 2, 3, Cb=100pF	10			ns
$T_{HD;DAT}$	Data hold time	Note 2, 3; Cb=100pF	40			ns
$T_{r;CL}$	Rise time of SCLH signal	Note 2, 3; Cb=100pF	10			ns
T_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	Note 2, 3, Cb=100pF	10			ns
T_{fCL}	Fall time of SCLH signal	Note 2, 3, Cb=100pF	10			ns
T_{rDA}	Rise time of SDAH signal	Note 2, 3, 4, Cb=100pF	10			ns
T_{fDA}	Fall time of SDAH signal	Note 2, 3, 4, Cb=100pF	10		80	ns
T_{rDA}	Rise time of SDAH signal	Note 2, 3, 4, Cb=400pF	20			ns
T_{fDA}	Fall time of SDAH signal	Note 2, 3, 4, Cb=400pF	20		160	ns
$T_{SU;STO}$	Set-up time for STOP condition	Note 2, 3, Cb=100pF	160			ns
C_b	Capacitive load for SDAH and SCLH		100		400	pF
C_b	Capacitive load for SDAH + SDA line and SCLH + SCL line				400	pF

Figure 48. I^2C-bus timings



Electrical Characteristics - AC OPERATION (continued)
(V_{DD1} = 1.7 to 3.6V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PARALLEL INTERFACE						
$T_{CY(EN)}$	Enable Cycle Time	V_{DD1} = 1.7V; Write; note 2, 6	150			ns
$T_{W(EN)}$	Enable Pulse width		60			ns
$T_{SU(A)}$	Address Set-up Time		30			ns
$T_{H(A)}$	Address Hold Time		40			ns
$T_{SU(D)}$	Data Set-Up Time		30			ns
$T_{H(D)}$	Data Hold Time		30			ns
$T_{SU(D)}$	Data Set-Up Time in read Mode				100	ns
$T_{HU(D)}$	Data Hold Time In Read mode		100			ns

Figure 49. Parallel interface Write timing

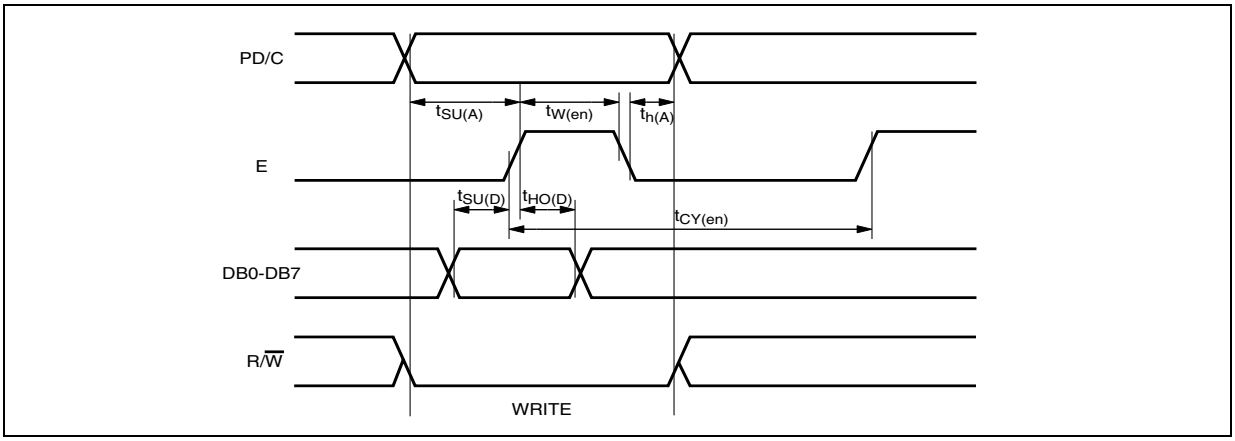
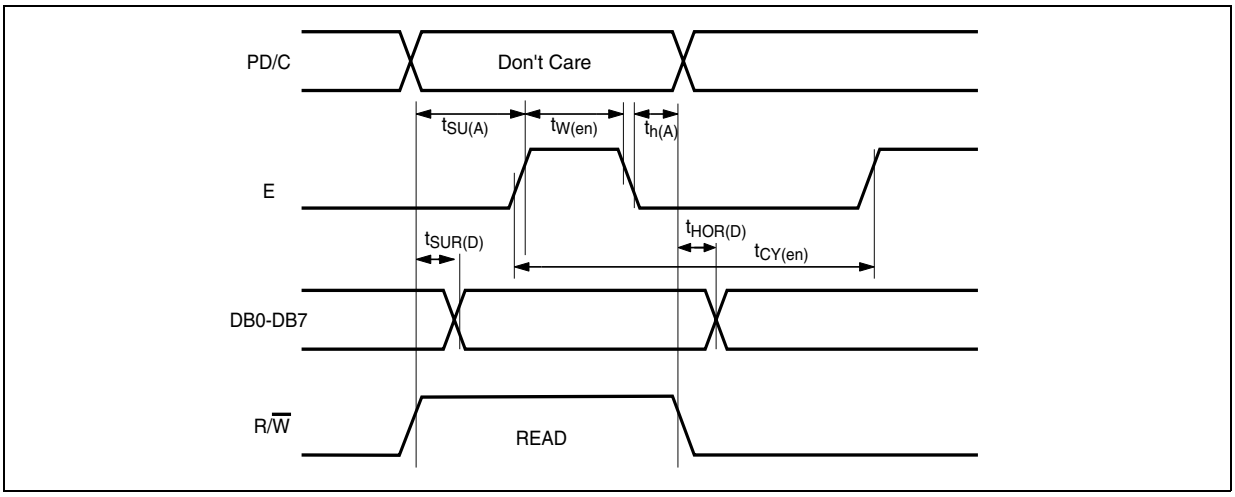


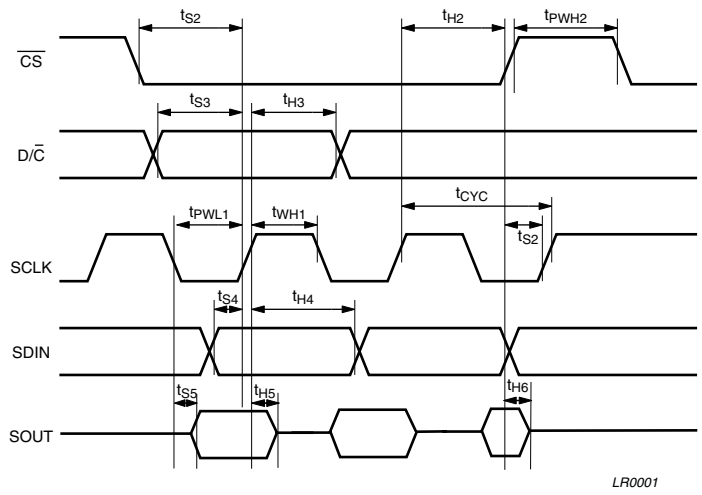
Figure 50. Parallel interface Read timing



Electrical Characteristics AC OPERATION (continued)
(V_{DD1} = 1.7 to 3.6V; V_{DD2} = 2.4 to 4.2V; $V_{ss1,2}$ = 0V; V_{LCD} = 4.5 to 13V; T_{amb} =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SERIAL INTERFACE						
T_{CYC}	Clock Cycle SCLK	V_{DD1} = 1.7V; Write; note 2, 6	150			ns
T_{PWH1}	SCLK pulse width HIGH		60			ns
T_{PWL1}	SCLK Pulse width LOW		60			ns
T_{S2}	$\overline{SCE}$ setup time		30			ns
T_{H2}	$\overline{SCE}$ hold time		50			ns
T_{PWH2}	$\overline{SCE}$ minimum high time		50			ns
T_{S3}	SD/$\overline{C}$ setup time		30			ns
T_{H3}	SD/$\overline{C}$ hold time		40			ns
T_{S4}	SDIN setup time		30			ns
T_{H4}	SDIN hold time		40			ns
T_{S5}	SOUT Access Time				100	ns
T_{H5}	SOUT Disable Time vs. SCLK				100	ns
T_{H6}	SOUT Disable Time vs. SCE				100	ns

Figure 51. Serial interface Timing



Notes: 1. $F_{frame} = \frac{f_{osc}}{960}$

2. All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}
3. Cb is the capacitive load for each bus line.
4. For bus line loads Cb between 100 and 400pF the timing parameters must be linearly interpolated
5. C_{VLCD} is the filtering Capacitor on VLCDOUT
6. T_{rise} and T_{fall} (30%-70%) = 10 ns

All numbers given inside the table below are after Shrink. Shrink factor= 0.9.

Table 26. Pad Coordinates

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
		X (hor)	Y (ver)
1	C127	2965.95	-590.85
2	C126	2920.95	-590.85
3	C125	2875.95	-590.85
4	C124	2830.95	-590.85
5	C123	2785.95	-590.85
6	C122	2740.95	-590.85
7	C121	2695.95	-590.85
8	C120	2650.95	-590.85
9	C119	2605.95	-590.85
10	C118	2560.95	-590.85
11	C117	2515.95	-590.85
12	C116	2470.95	-590.85
13	C115	2425.95	-590.85
14	C114	2380.95	-590.85
15	C113	2335.95	-590.85
16	C112	2290.95	-590.85
17	C111	2245.95	-590.85
18	C110	2200.95	-590.85
19	C109	2155.95	-590.85
20	C108	2110.95	-590.85
21	C107	2065.95	-590.85
22	C106	2020.95	-590.85
23	C105	1975.95	-590.85
24	C104	1930.95	-590.85
25	C103	1885.95	-590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
26	C102	1840.95	-590.85
27	C101	1795.95	-590.85
28	C100	1750.95	-590.85
29	C99	1705.95	-590.85
30	C98	1660.95	-590.85
31	C97	1615.95	-590.85
32	C96	1570.95	-590.85
33	C95	1525.95	-590.85
34	C94	1480.95	-590.85
35	C93	1435.95	-590.85
36	C92	1390.95	-590.85
37	C91	1345.95	-590.85
38	C90	1300.95	-590.85
39	C89	1255.95	-590.85
40	C88	1210.95	-590.85
41	C87	1165.95	-590.85
42	C86	1120.95	-590.85
43	C85	1075.95	-590.85
44	C84	1030.95	-590.85
45	C83	985.95	-590.85
46	C82	940.95	-590.85
47	C81	895.95	-590.85
48	C80	850.95	-590.85
49	C79	805.95	-590.85
50	C78	760.95	-590.85
51	C77	715.95	-590.85
52	C76	670.95	-590.85
53	C75	625.95	-590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
54	C74	580.95	-590.85
55	C73	535.95	-590.85
56	C72	490.95	-590.85
57	C71	445.95	-590.85
58	C70	400.95	-590.85
59	C69	355.95	-590.85
60	C68	310.95	-590.85
61	C67	265.95	-590.85
62	C66	220.95	-590.85
63	C65	175.95	-590.85
64	C64	130.95	-590.85
65	C63	-130.95	-590.85
66	C62	-175.95	-590.85
67	C61	-220.95	-590.85
68	C60	-265.95	-590.85
69	C59	-310.95	-590.85
70	C58	-355.95	-590.85
71	C57	-400.95	-590.85
72	C56	-445.95	-590.85
73	C55	-490.95	-590.85
74	C54	-535.95	-590.85
75	C53	-580.95	-590.85
76	C52	-625.95	-590.85
77	C51	-670.95	-590.85
78	C50	-715.95	-590.85
79	C49	-760.95	-590.85
80	C48	-805.95	-590.85
81	C47	-850.95	-590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
82	C46	-895.95	-590.85
83	C45	-940.95	-590.85
84	C44	-985.95	-590.85
85	C43	-1030.95	-590.85
86	C42	-1075.95	-590.85
87	C41	-1120.95	-590.85
88	C40	-1165.95	-590.85
89	C39	-1210.95	-590.85
90	C38	-1255.95	-590.85
91	C37	-1300.95	-590.85
92	C36	-1345.95	-590.85
93	C35	-1390.95	-590.85
94	C34	-1435.95	-590.85
95	C33	-1480.95	-590.85
96	C32	-1525.95	-590.85
97	C31	-1570.95	-590.85
98	C30	-1615.95	-590.85
99	C29	-1660.95	-590.85
100	C28	-1705.95	-590.85
101	C27	-1750.95	-590.85
102	C26	-1795.95	-590.85
103	C25	-1840.95	-590.85
104	C24	-1885.95	-590.85
105	C23	-1930.95	-590.85
106	C22	-1975.95	-590.85
107	C21	-2020.95	-590.85
108	C20	-2065.95	-590.85
109	C19	-2110.95	-590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
110	C18	-2155.95	-590.85
111	C17	-2200.95	-590.85
112	C16	-2245.95	-590.85
113	C15	-2290.95	-590.85
114	C14	-2335.95	-590.85
115	C13	-2380.95	-590.85
116	C12	-2425.95	-590.85
117	C11	-2470.95	-590.85
118	C10	-2515.95	-590.85
119	C9	-2560.95	-590.85
120	C8	-2605.95	-590.85
121	C7	-2650.95	-590.85
122	C6	-2695.95	-590.85
123	C5	-2740.95	-590.85
124	C4	-2785.95	-590.85
125	C3	-2830.95	-590.85
126	C2	-2875.95	-590.85
127	C1	-2920.95	-590.85
128	C0	-2965.95	-590.85
129	ICON	-3133.35	-517.5
130	R0	-3133.35	-472.5
131	R1	-3133.35	-427.5
132	R2	-3133.35	-382.5
133	R3	-3133.35	-337.5
134	R4	-3133.35	-292.5
135	R5	-3133.35	-247.5
136	R6	-3133.35	-202.5
137	R7	-3133.35	-157.5

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
138	R8	-3133.35	-112.5
139	R9	-3133.35	-67.5
140	R10	-3133.35	-22.5
141	R11	-3133.35	22.5
142	R12	-3133.35	67.5
143	R13	-3133.35	112.5
144	R14	-3133.35	157.5
145	R15	-3133.35	202.5
146	R16	-3133.35	247.5
147	R17	-3133.35	292.5
148	R18	-3133.35	337.5
149	R19	-3133.35	382.5
150	R20	-3133.35	427.5
151	R21	-3133.35	472.5
152	R22	-3133.35	517.5
153	R23	-2965.95	590.85
154	R24	-2920.95	590.85
155	R25	-2875.95	590.85
156	R26	-2830.95	590.85
157	R27	-2785.95	590.85
158	R28	-2740.95	590.85
159	R29	-2695.95	590.85
160	R30	-2650.95	590.85
161	R31	-2605.95	590.85
162	R32	-2560.95	590.85
163	R33	-2515.95	590.85
164	R34	-2470.95	590.85
165	R35	-2425.95	590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
166	R36	-2380.95	590.85
167	R37	-2335.95	590.85
168	R38	-2290.95	590.85
169	R39	-2245.95	590.85
170	VLCDOUT	-2200.95	590.85
171	VLCDOUT_1	-2155.95	590.85
172	VLCDOUT_2	-2110.95	590.85
173	VLCDOUT_3	-2065.95	590.85
174	VLCDOUT_4	-2020.95	590.85
175	VLCDSENSE	-1975.95	590.85
176	VLCDIN	-1930.95	590.85
177	VLCDIN_1	-1885.95	590.85
178	VLCDIN_2	-1840.95	590.85
179	VLCDIN_3	-1795.95	590.85
180	VLCDIN_4	-1750.95	590.85
181	OSC_OUT	-1630.22	590.85
182	TEST_12	-1415.57	590.85
183	TEST_11	-1370.57	590.85
184	TEST_10	-1325.57	590.85
185	TEST_9	-1280.57	590.85
186	Vss	-1235.57	590.85
187	Vss_1	-1190.57	590.85
188	Vss_2	-1145.57	590.85
189	Vss_3	-1100.57	590.85
190	Vss_4	-1055.57	590.85
191	Vss_5	-1010.57	590.85
192	Vss_6	-965.565	590.85
193	Vss_7	-920.565	590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
194	Vss_8	-875.565	590.85
195	Vss_9	-830.565	590.85
196	SCL	-785.565	590.85
197	SDA_IN	-740.565	590.85
198	SDA_OUT	-695.565	590.85
199	SDA_OUT_1	-650.565	590.85
200	VSSAUX	-605.565	590.85
201	N_RES	-444.645	590.85
202	PCLK	-290.565	590.85
203	PDC	-245.565	590.85
204	PD0	-200.565	590.85
205	PD1	-155.565	590.85
206	PD2	-110.565	590.85
207	PD3	-65.565	590.85
208	PD4	-20.565	590.85
209	PD5	24.435	590.85
210	PD6	69.435	590.85
211	PD7	114.435	590.85
212	R_W	159.435	590.85
213	VSSAUX_1	204.435	590.85
214	SCLK	249.435	590.85
215	N_SCE	294.435	590.85
216	SDC	339.435	590.85
217	SDIN	384.435	590.85
218	SDOUT	429.435	590.85
219	N_BSY_FLG	474.435	590.85
220	VDD2	519.435	590.85
221	VDD2_1	564.435	590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
222	VDD2_2	609.435	590.85
223	VDD2_3	654.435	590.85
224	VDD2_4	699.435	590.85
225	VDD2_5	744.435	590.85
226	VDD	789.435	590.85
227	VDD_1	834.435	590.85
228	VDD_2	879.435	590.85
229	VDD_3	924.435	590.85
230	VDD_4	969.435	590.85
231	VDD_5	1014.44	590.85
232	OSC_IN	1059.44	590.85
233	ICON_MODE	1104.44	590.85
234	SEL1	1149.44	590.85
235	SEL2	1194.44	590.85
236	EXT_SET	1239.44	590.85
237	SA0	1284.44	590.85
238	SA1	1329.44	590.85
239	VSSAUX_2	1374.44	590.85
240	TEST_8	1587.38	590.85
241	TEST_7	1632.38	590.85
242	TEST_6	1677.38	590.85
243	TEST_5	1722.38	590.85
244	TEST_4	1767.38	590.85
245	TEST_3	1812.38	590.85
246	TEST_2	1857.38	590.85
247	TEST_1I	1902.38	590.85
248	R80	2245.95	590.85
249	R79	2290.95	590.85

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
250	R78	2335.95	590.85
251	R77	2380.95	590.85
252	R76	2425.95	590.85
253	R75	2470.95	590.85
254	R74	2515.95	590.85
255	R73	2560.95	590.85
256	R72	2605.95	590.85
257	R71	2650.95	590.85
258	R70	2695.95	590.85
259	R69	2740.95	590.85
260	R68	2785.95	590.85
261	R67	2830.95	590.85
262	R66	2875.95	590.85
263	R65	2920.95	590.85
264	R64	2965.95	590.85
265	R63	3133.35	517.50
266	R62	3133.35	472.50
267	R61	3133.35	427.50
268	R60	3133.35	382.50
269	R59	3133.35	337.50
270	R58	3133.35	292.50
271	R57	3133.35	247.50
272	R56	3133.35	202.50
273	R55	3133.35	157.50
274	R54	3133.35	112.50
275	R53	3133.35	67.50
276	R52	3133.35	22.50
277	R51	3133.35	-22.50

Table 26. Pad Coordinates (continued)

N°	NAME	PAD PLACEMENT	
		X (hor)	Y (ver)
278	R50	3133.35	-67.50
279	R49	3133.35	-112.50
280	R48	3133.35	-157.50
281	R47	3133.35	-202.50
282	R46	3133.35	-247.50
283	R45	3133.35	-292.50
284	R44	3133.35	-337.50
285	R43	3133.35	-382.50
286	R42	3133.35	-427.50
287	R41	3133.35	-472.50
288	R40	3133.35	-517.50

Table 27. Alignment marks coordinates & size

item	X	Y	X_size	Y_size
Marker 1	3132.90	-594	84.6	84.6
Marker 2	-3132.9	-594	84.6	84.6
Marker 3	-1519.92	594.00	84.6	84.6
Marker 4	2078.685	594.00	84.6	84.6

Alignment marks dimensions

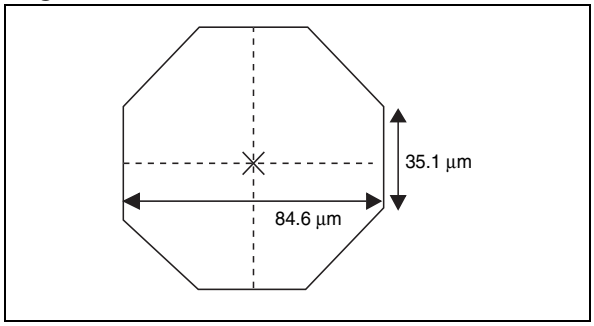


Table 28. Bumps

	dimensions
bumps	31µmx89µmx17.5µm
pad size	38µmx96µm
pad pitch	45µm
spacing between bumps	14µm

Table 29. Die Mechanical Dimensions

Die Size	6517µmx1432µm
Wafers Thickness	500µm

Figure 52. DIE orientation in tray

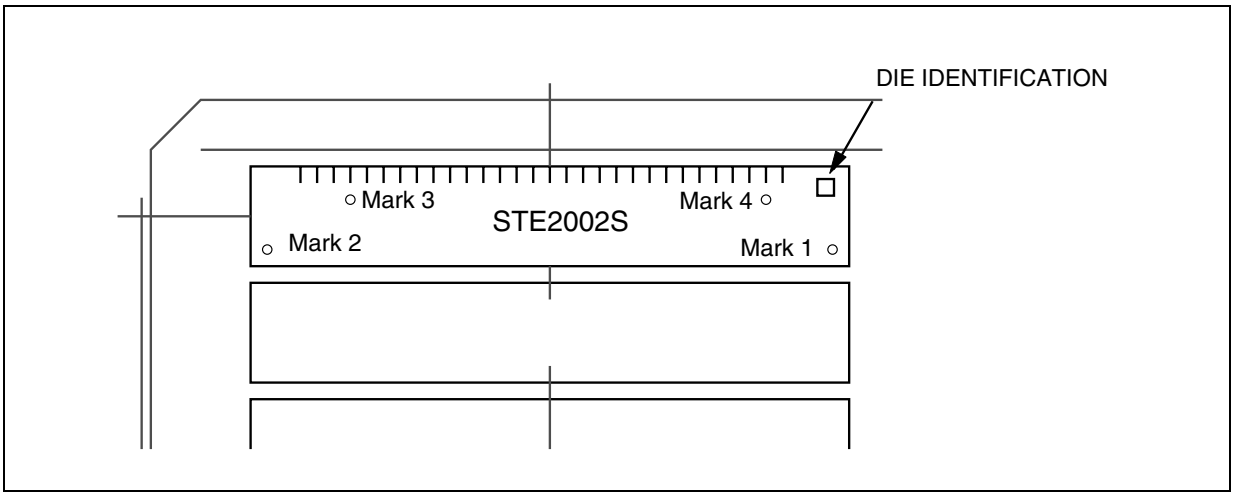


Figure 53. Tray Information

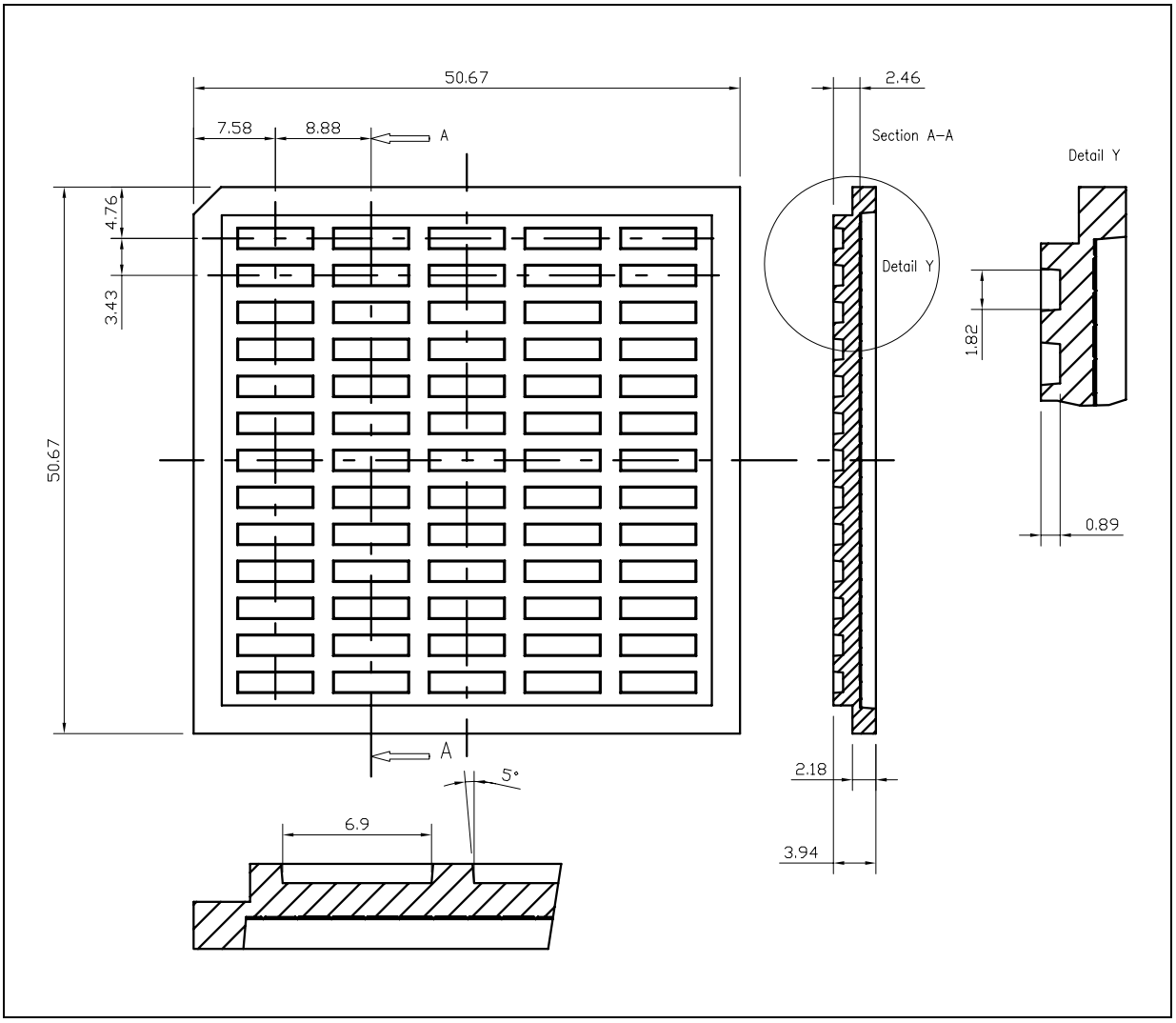


Table 30. Revision History

Date	Revision	Description of Changes
October 2005	1	First Issue