REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added test circuit to Figure 2. –lgt	00-07-21	Raymond Monnin
B	Add device type 02. Add package Y. Add radiation features. Editorial changes throughout. - drw	01-06-29	Raymond Monnin
C	Add device type 03. - drw	01-08-29	Raymond Monnin
D	Add device types 04 and 05. Add appendix A. Editorial changes throughout. – drw	04-08-25	Raymond Monnin
E	For paragraph 1.5, clarify radiation features for device types 02, 03, 04, and 05. - drw	09-04-10	Joseph D. Rodenbeck
F	Add device type 06. Add radiation features for device type 06, paragraph 1.5. - drw	10-04-21	Charles F. Saffle
G	Add device type 07. Add case outline Z. - drw	14-05-19	Charles F. Saffle
H	Make change to the Output voltage (R_{OUT}) limit for device type 07 only as specified under paragraph 1.3. Make change to the Input clamp voltage (V_{CL}) test for device type 07 only as specified under Table I. - ro	15-03-09	Charles F. Saffle
J	Add device type 08 and delta burn-in life test Table IIB. Add last two sentences to Note section under figure A-1. - ro	15-11-02	Charles F. Saffle

REV																			
SHEET																			
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Dan Wonnell

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
00-04-19

REVISION LEVEL
J

MICROCIRCUIT, LINEAR, LINE RECEIVER, DIFFERENTIAL, QUAD, LVDS, LOW VOLTAGE, MONOLITHIC SILICON

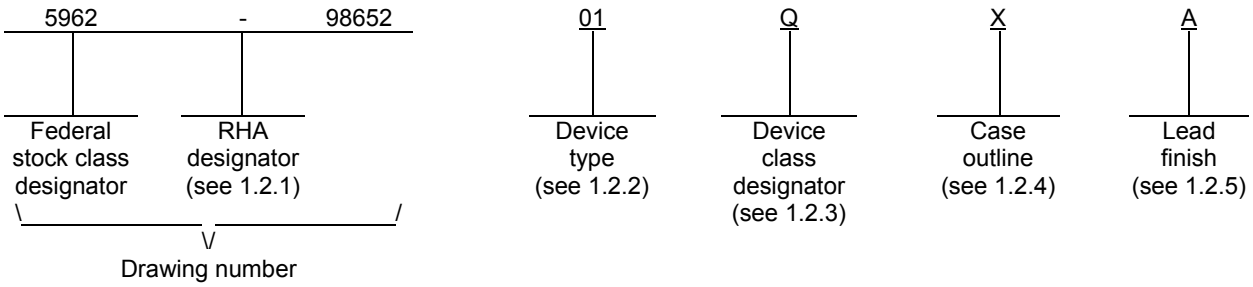
SIZE	CAGE CODE	
A	**67268**	**5962-98652**

SHEET 1 OF 28

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	DS90LV032A	Quad differential line receiver, LVDS
02	UT54LVDS032LV	Radiation hardened, LVDS quad differential line receiver.
03	UT54LVDS032LV	Radiation hardened, LVDS quad differential line receiver.
04	UT54LVDS032LVE	Radiation hardened, LVDS quad differential line receiver with enhanced AC parameters
05	UT54LVDS032LVE	Radiation hardened, LVDS quad differential line receiver with enhanced AC parameters
06	LVDS032	Radiation hardened, LVDS quad differential line receiver.
07	RHFLVDS32	Radiation hardened, LVDS quad differential line receiver.
08	RHFLVDS32	Radiation hardened, LVDS quad differential line receiver.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
F	GDFP2-F16 or CDFP3-T16	16	Flat pack
X	GDFP1-G16	16	Flat pack with gull-wing leads
Y	CDFP4-F16	16	Flat pack
Z	CDFP4-F16	16	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}):
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to +4 V
- Device types 07 and 08 ..... -0.3 V to +4.8 V

Input voltage (R_{IN}+, R_{IN}-) : 2/
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to +3.9 V
- Device type 07 ..... -5 V to +6 V
- Device type 08 ..... -2 V to +5 V

Enable input voltage (EN, $\overline{EN}$):
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to (V_{CC} + 0.3 V)
- Device types 07 and 08 ..... -0.3 V to +4.8 V

Output voltage (R_{OUT}):
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to (V_{CC} + 0.3 V)
- Device types 07 and 08 ..... -0.3 V to 4.8 V

Storage temperature range ..... -65°C to +150°C

Lead temperature (soldering, 4 seconds) ..... +260°C

Package power dissipation at T_A = +25°C (P_D): 3/
- Case outlines F and X ..... 845 mW
- Case outline Y ..... 1250 mW
- Case outline Z ..... 1.04 W

Thermal resistance, junction-to-ambient (θ_{JA}):
- Case outlines F and X ..... 148°C/W
- Case outlines Y and Z ..... 120°C/W

Thermal resistance, junction-to-case (θ_{JC}):
- Case outlines F and X ..... 21°C/W
- Case outline Y ..... 20°C/W
- Case outline Z ..... 22°C/W

Junction temperature (T_J) ..... +150°C 4/

1.4 Recommended operating conditions.

Operating temperature range (T_A):
- Device type 01 ..... -55°C to +85°C
- Device types 02, 03, 04, 05, 06, 07, and 08 ..... -55°C to +125°C

Operating voltage range (V_{CC}):
- Device type 01 ..... 3.15 V to 3.45 V
- Device types 02, 03, 04, 05, 06, 07, and 08 ..... 3.0 V to 3.6 V

Receiver input voltage
- Device types 01, 02, 03, 04, 05, 06 ..... GND to 3.0 V
- Device type 07 ..... -4 V to +5 V
- Device type 08 ..... -1 V to +4 V

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For device types 02, 03, 04, 05, and 06, maximum voltage on any pin during cold spare (V_{DD} = V_{SS}) – 0.3 V to 4.3 V.
For device type 07, maximum voltage on any pin during cold spare (V_{DD} = V_{SS}) – 5 V to 6 V.
For device type 08, maximum voltage on any pin during cold spare (V_{DD} = V_{SS}) – 2 V to 5 V.

3/ For case outlines F, X and Y, derate 6.8 mW/°C above T_A = +25°C. For case outline Z, derate 8.32 mW/°C above T_A = +25°C.

4/ For device types 02, 03, 04, 05, and 06, the maximum junction temperature may be increased to +175°C during burn-in and life test.

1.5 Radiation features.

Maximum total dose available:

Device types 02 and 04 (effective dose rate = 1 rad(Si)/s)	1 Mrads(Si) 5/
Device types 03 and 05 (effective dose rate = 5 rad(Si)/s)	100 krads(Si) 5/
Device type 06 (dose rate = 50 – 300 rads (Si)/s)	100 krads(Si) 6/
Device types 07 and 08 (effective dose rate = 0.25 rad(Si)/s)	300 krads(Si) 5/
Neutron irradiation for device types 02, 03, 04, and 05 only	1 X 10^{13} neutrons/cm^2 7/

Single event effects(SEE):

Device types 02, 03, 04 and 05 only	
No SEL occurs at effective LET (see 4.4.4.4)	≤ 100 MeV/mg/cm^2
Device types 07 and 08 only	
No SEL occurs at effective LET (see 4.4.4.4)	≤ 120 MeV/mg/cm^2

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

5/ Device types 02, 03, 04, 05, 07, and 08 are irradiated at dose rate = 50 – 300 rads(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and are guaranteed to the maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad(Si)/s for device types 02 and 04; and 5 rads(Si)/s for device types 03 and 05 ; and 0.25 rad(Si)/s for device types 07 and 08 per MIL-STD-883, method 1019, condition A and section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment.
6/ The device type 06 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.
7/ Guaranteed, but not tested.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Device type 01 conditions: $-55°C \le T_A \le +85°C$, V_{CC} = 3.15 V, 3.30 V, 3.45 V, C_L = 20 pF; Device types 02, 03, 04, 05, 06, 07 and 08 conditions: $-55°C \le T_A \le +125°C$ 1/, V_{CC} = 3.0 V to 3.6 V, C_L = 10 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential input low threshold	V_{TL}	V_{CM} = +1.2 V 2/	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08	-100		mV
		-4 V < V_{CM} < +5 V		07	-130		
Differential input high threshold	V_{TH}	V_{CM} = +1.2 V 2/	1, 2, 3	01, 02, 03, 04, 05, 06, 07, 08		100	mV
		-4 V < V_{CM} < +5 V		07		130	
Input clamp voltage	V_{CL}	I_{CL} = 18 mA	1, 2, 3	01		-1.5	V
				02, 03, 04, 05, 06	-1.5		
		I_{CL} = 18 mA, EN and $\overline{EN}$ pins		07, 08	-1.5		
Common mode voltage range	VCMR	V_{ID} = 200 mV peak to peak 2/, 3/, 4/	1, 2, 3	01, 02, 03, 04, 05, 06	0.1	2.3	V
		V_{ID} = 200 mV peak to peak 2/, 4/, 5/		07	-4	+5	
				08	-1	+4	
Input current	I_{IN}	V_{CC} = 3.45 V or 0 V, V_{IN} = 2.8 V or 0 V	1, 2, 3	01		±10	µA
		V_{CC} = 0 V, V_{IN} = 3.45 V				±20	
		V_{CC} = 3.6 V, V_{IN} = 2.4 V receiver inputs		02, 03, 04, 05, 06		±15	
		V_{CC} = 0 V, V_{IN} = 3.6 V, all inputs				±20	
		Each input differential = -4 V to +5 V, V_{CC} = 0 V		07		±60	
		V_{IN} = -4 V to +5 V, V_{CC} = 3.6 V				±70	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Device type 01 conditions: $-55°C \le T_A \le +85°C$, V_{CC} = 3.15 V, 3.30 V, 3.45 V, C_L = 20 pF; Device types 02, 03, 04, 05, 06, 07 and 08 conditions: $-55°C \le T_A \le +125°C$ 1/, V_{CC} = 3.0 V to 3.6 V, C_L = 10 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input current	I_{IN}	Each input differential = -1 V to +4 V, V_{CC} = 0 V	1, 2, 3	08		±60	µA
		V_{IN} = -1 V to +4 V, V_{CC} = 3.6 V				±70	
Output high voltage	V_{OH}	I_{OH} = -0.4 mA, V_{ID} = 200 mV	1, 2, 3	01	2.7		V
		I_{OH} = -0.4 mA, inputs open			2.7		
		I_{OH} = -0.4 mA, V_{CC} = 3.0 V		02, 03, 04, 05, 06, 07, 08	2.7		
Output low voltage	V_{OL}	I_{OL} = 2 mA, V_{ID} = -200 mV	1, 2, 3	01		0.25	V
		I_{OL} = 2 mA, V_{CC} = 3.0 V		02, 03, 04, 05, 06, 07, 08		0.25	
Output short circuit current	I_{OS}	Enabled, V_{OUT} = 0 V 6/	1, 2, 3	01	-15	-120	mA
				02, 03, 04, 05, 06	-15	-130	
				07, 08	-30	-90	
Output TRI-STATE current	I_{OZ}	Disabled, V_{OUT} = 0 V or V_{CC}	1, 2, 3	All		±10	µA
Input high voltage	V_{IH}	7/	1, 2, 3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}	7/	1, 2, 3	All	GND	0.8	V
Functional test	FT	See 4.4.1c	7, 8	All			
Input current	I_I	V_{IN} = V_{CC} or 0 V, other input = V_{CC} or GND	1, 2, 3	01		±10	µA
		V_{IN} = 3.6 V, V_{CC} = 3.6 V, Enable pins		02, 03, 04, 05, 06, 07		±10	
		EN, $\overline{EN}$ = 3.6 V, V_{CC} = 0 V		07, 08		±10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Device type 01 conditions: $-55°C \le T_A \le +85°C$, V_{CC} = 3.15 V, 3.30 V, 3.45 V, C_L = 20 pF; Device types 02, 03, 04, 05, 06, 07 and 08 conditions: $-55°C \le T_A \le +125°C$ 1/, V_{CC} = 3.0 V to 3.6 V, C_L = 10 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current, no load, receivers enabled	I_{CC}	EN, $\overline{EN}$ = V_{CC} or GND, inputs open	1, 2, 3	All		15	mA
		EN, $\overline{EN}$ = 2.4 V or 0.5V, inputs open		01		15	
Supply current, no load, receivers disabled	I_{CCZ}	EN = GND, $\overline{EN}$ = V_{CC}, inputs open	1, 2, 3	01		5	mA
				02, 03, 04, 05, 06, 07, 08		4	
Propagation delay, differential, high to low	t_{PHLD}	V_{ID} = 200 mV, input pulse = 1.1 V to 1.3 V, V_{IN} = 1.2 V (0 V differential) to V_{OUT} = ½ V_{CC}, see figure 2	9, 10, 11	01	0.5	3.5	ns
				02, 03, 06	1.0	4.0	
				04, 05	1.0	1.9	
				07	1.0	2.5	
				08	1.0	3.5	
Propagation delay, differential, low to high	t_{PLHD}	V_{ID} = 200 mV, input pulse =1.1 V to 1.3 V, V_{IN} = 1.2 V (0 V differential) to V_{OUT} = ½ V_{CC}, see figure 2	9, 10, 11	01	0.5	3.5	ns
				02, 03, 06	1.0	4.0	
				04, 05	1.0	1.9	
				07	1.0	2.5	
				08	1.0	3.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Device type 01 conditions: $-55°C \le T_A \le +85°C$, V_{CC} = 3.15 V, 3.30 V, 3.45 V, C_L = 20 pF. Device types 02, 03, 04, 05, 06, 07 and 08 conditions: $-55°C \le T_A \le +125°C$ 1/, V_{CC} = 3.0 V to 3.6 V, C_L = 10 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential skew $\lvert t_{PHLD} - t_{PLHD} \rvert$	t_{SKD}	V_{ID} = 200 mV	9, 10, 11	01		1.5	ns
				02, 03, 06		0.35	
				04, 05		0.21	
				07		0.3	
				08		0.6	
Channel to channel skew	t_{SK1}	V_{ID} = 200 mV 8/	9, 10, 11	01		1.75	ns
				02, 03, 06		0.5	
				04, 05		0.2	
				07		0.25	
				08		0.6	
Chip to chip skew	t_{SK2}	V_{ID} = 200 mV 9/	9, 10, 11	01, 02, 03, 06, 08		3.0	ns
				04, 05		0.9	
				07		0.7	
Disable time low to Z	t_{PLZ}	Input pulse = 0 V to 3.0 V, V_{IN} = 1.5 V, R_L = 1 kΩ, $V_{OUT} = V_{OL}$ + 0.5 V, see figure 2	9, 10, 11	01, 08		12	ns
				02, 03, 06		12	
				04, 05, 07		3.8	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Device type 01 conditions: $-55°C \le T_A \le +85°C$, V_{CC} = 3.15 V, 3.30 V, 3.45 V, C_L = 20 pF; Device types 02, 03, 04, 05, 06, 07 and 08 conditions: $-55°C \le T_A \le +125°C$ 1/, V_{CC} = 3.0 V to 3.6 V, C_L = 10 pF unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Disable time high to Z	t_{PHZ}	Input pulse = 0 V to 3.0 V, V_{IN} = 1.5 V, R_L = 1 kΩ, $V_{OUT} = V_{OH}$ - 0.5 V, see figure 2	9, 10, 11	01, 08		12	ns
				02, 03, 06		12	
				04, 05, 07		3.8	
Enable time Z to high	t_{PZH}	Input pulse = 0 V to 3.0 V, V_{IN} = 1.5 V, V_{OUT} = 50%, R_L = 1 kΩ, see figure 2	9, 10, 11	01		20	ns
				02, 03, 06		17	
				04, 05, 07		3.8	
				08		12	
Enable time Z to low	t_{PZL}	Input pulse = 0 V to 3.0 V, V_{IN} = 1.5 V, V_{OUT} = 50%, R_L = 1 kΩ, see figure 2	9, 10, 11	01		20	ns
				02, 03, 06		17	
				04, 05, 07		3.8	
				08		12	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

1/ Device types 02 and 04 supplied to this drawing will meet all levels M, D, P, L, R, F, G, H of irradiation. However, this device is only tested at the 'H' levels. Device types 03, 05, and 06 supplied to this drawing will meet all levels M, D, P, L, R of irradiation. However, this device is only tested at the 'R' levels. Device types 07 and 08 supplied to this drawing will meet all levels M, D, P, L, R, F of irradiation. However, this device is only tested at the 'F' levels. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Tested during V_{OH}/V_{OL} tests by applying appropriate voltage levels to the input pins of the device under test. For device type 07, tested during V_{TL}/V_{TH} tests by applying appropriate voltage levels to the input pins of the device under test.

3/ The VCMR range is reduced for larger input differential voltage (V_{ID}). Example: If V_{ID} = 400 mV, the VCMR is 0.2 V to 2.2 V. A V_{ID} up to V_{CC} – 0 V may be applied to the $R_{IN}+/R_{IN}-$ inputs with the common-mode voltage set to $V_{CC}/2$.

4/ Guaranteed by characterization, device types 02, 03, 04, 05, 06, 07, and 08.

5/ The VCMR range is reduced for larger input differential voltage (V_{ID}). Example: If V_{ID} = 400 mV, the VCMR = -3.8 V to 4.8 V.

6/ Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction of current. Only one output should be shorted at a time, do not exceed maximum junction temperature.

7/ Tested during I_{OZ} tests by applying appropriate threshold voltage levels to the EN and $\overline{EN}$ pins.

8/ Channel to channel skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

9/ Chip to chip skew is defined as the difference between the minimum and maximum specified differential propagation delays.

TABLE IB. SEP test limits. 1/ 2/

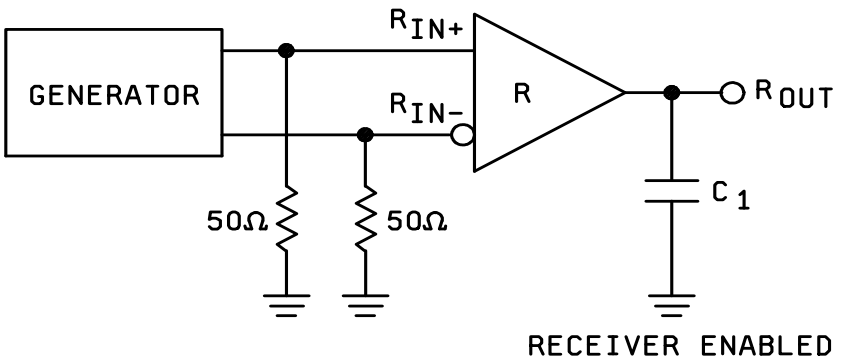
Device types	SEP	Temperature (T_C)	Bias V_{CC} = 3.0 V for latch up (SEL) test no latch up effective linear energy transfer (LET)
02, 03, 04, 05	No SEL	+125°C	LET ≤ 100 MeV-cm^2/mg
07, 08	No SEL	+125°C	LET ≤ 120 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.4 herein.

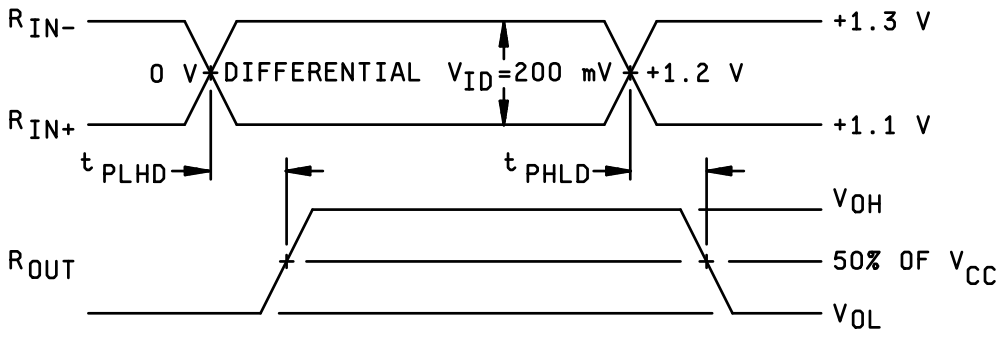
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

Device types	01, 02, 03, 04, 05, 06, 07, and 08
Case outlines	F, X, Y and Z
Terminal number	Terminal symbol
1	R_{IN1}-
2	R_{IN1}+
3	R_{OUT1}
4	EN
5	R_{OUT2}
6	R_{IN2}+
7	R_{IN2}-
8	GND
9	R_{IN3}-
10	R_{IN3}+
11	R_{OUT3}
12	$\overline{EN}$
13	R_{OUT4}
14	R_{IN4}+
15	R_{IN4}-
16	V_{CC}

FIGURE 1. Terminal connections.

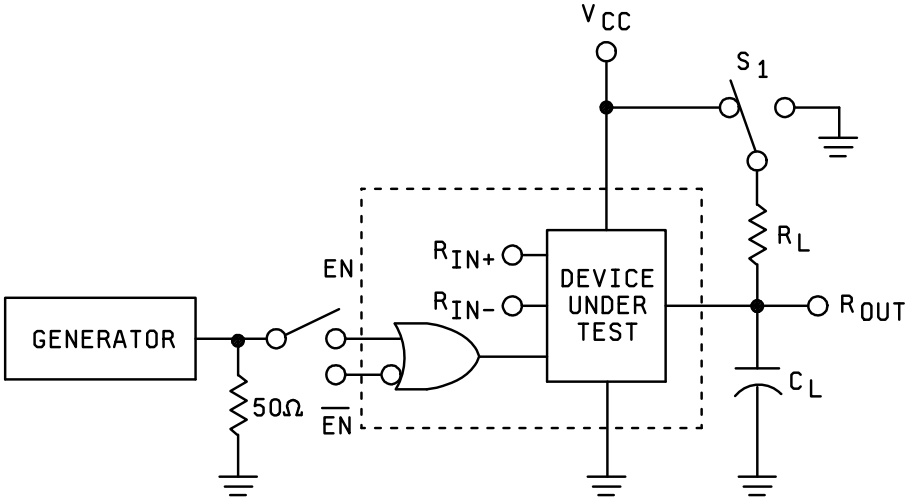


Receiver Propagation Delay Test Circuit



Receiver Propagation Delay Waveforms

FIGURE 2. Timing circuits and waveforms .

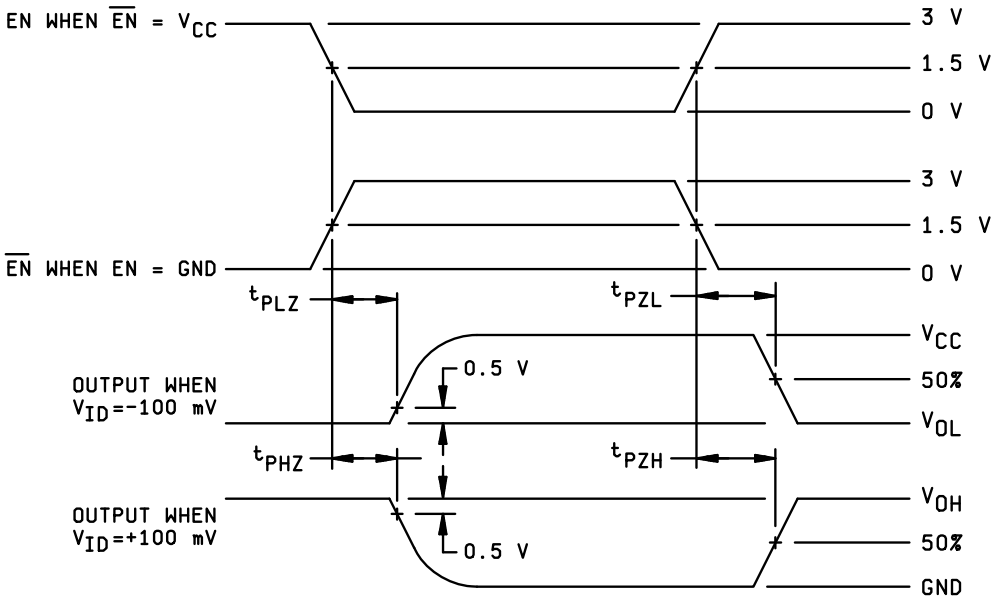


C_L includes load and test jig capacitance.

S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

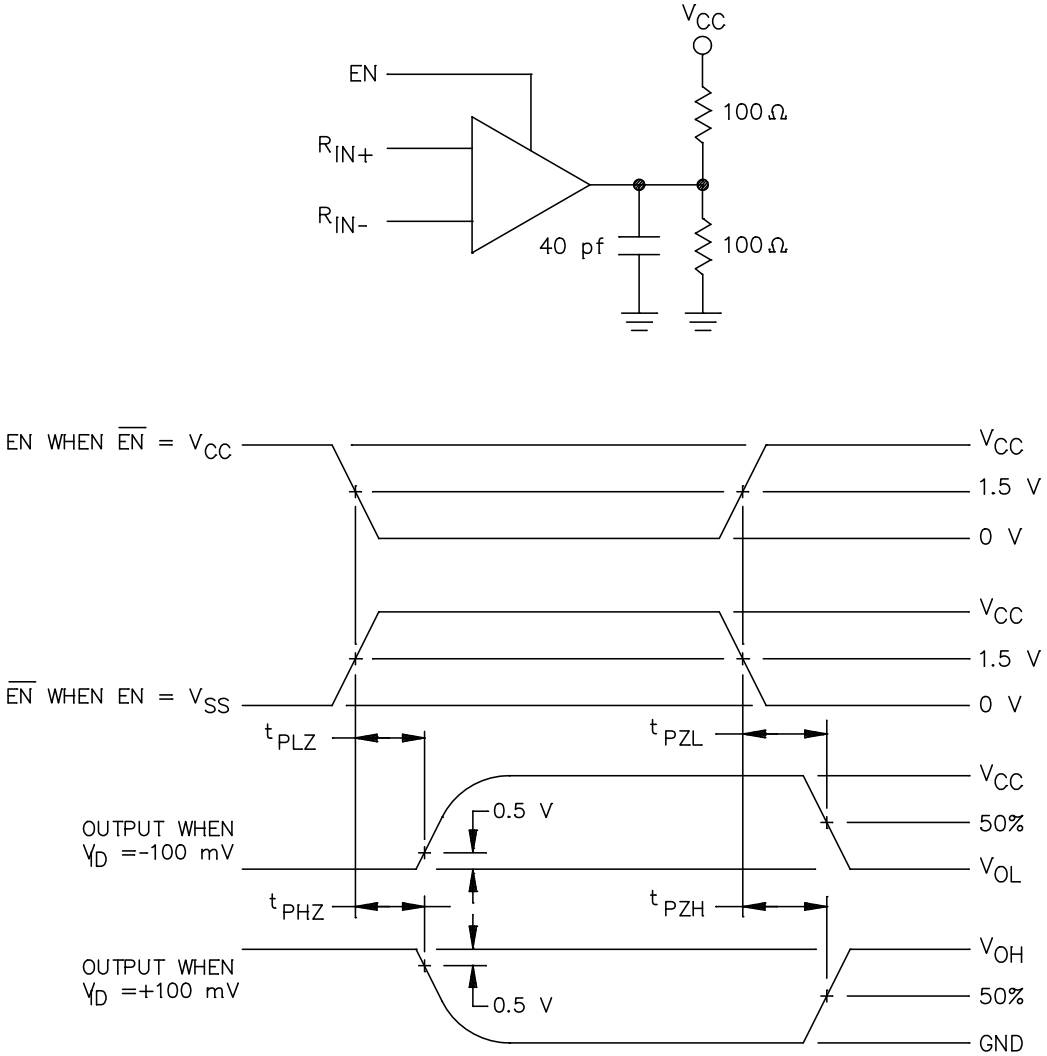
S_1 = GND for t_{PZH}, and t_{PHZ} measurements.

Device Type 01, Receiver TRI-STATE Delay Test Circuit



Device Type 01, Receiver TRI-STATE Delay Waveforms

FIGURE 2. Timing circuits and waveforms – continued.



DEVICE TYPES 02, 03, 04, 05, 06, 07 and 08
RECEIVER THREE-STATE DELAY WAVEFORMS AND TEST CIRCUIT

NOTE: For device types 07 and 08, C_L = 10 pF and R_L = 400 Ω.

FIGURE 2. Timing circuits and waveforms – continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 8, 2/ 3/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Conditions	Device types	Limit
Supply current, no load, receiver enabled	I_{CC}		02, 03, 04, 05	±1.5 mA
Input current low	I_{IL}		06	±150 nA
Input current high	I_{IH}			±150 nA
Low impedance output current	I_{OZL}			±1 µA
High impedance output current	I_{OZH}			±1 µA
Drivers enabled supply current, no loads	I_{CC}			±1 mA
Drivers enabled supply current, loaded	I_{CCL}		06, 07, 08	±1 mA
Drivers disabled supply current, loaded or no load	I_{CCZ}			±0.4 mA

1/ Deltas are performed at room temperature.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. For device types 02, 03, 04, and 05 total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition "A" and as specified herein (see paragraph 1.5). For device types 06, 07, and 08 total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition "A" and as specified herein (see paragraph 1.5).

4.4.4.2 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25 ºC ±5ºC after an exposure of 2×10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see paragraph 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be 25°C for the latchup measurements.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

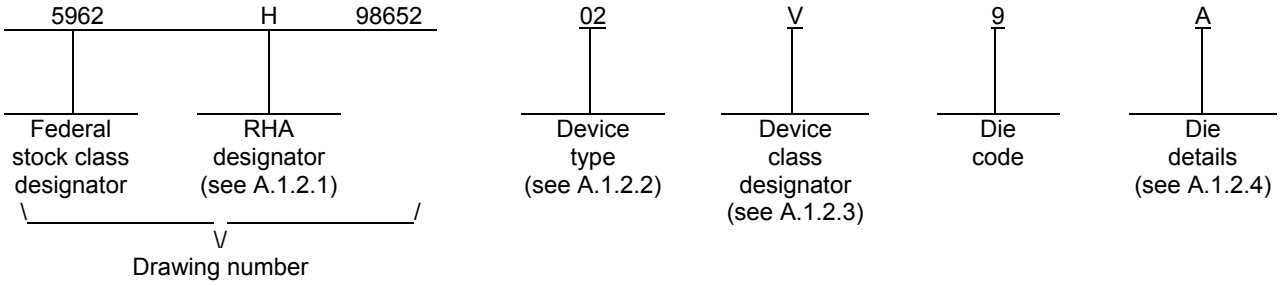
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-98652

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
02	UT54LVDS032LV	Radiation hardened, (dose rate ≤ 1 rad(Si)/s), quad differential line receiver, LVDS
03	UT54LVDS032LV	Radiation hardened, (dose rate ≤ 5 rad(Si)/s), quad differential line receiver, LVDS
04	UT54LVDS032LVE	Radiation hardened, (dose rate ≤ 1 rad(Si)/s), quad differential line receiver, LVDS, with enhanced AC parameters
05	UT54LVDS032LVE	Radiation hardened, (dose rate ≤ 5 rad(Si)/s), quad differential line receiver, LVDS, with enhanced AC parameters
07	RHFLVDS32	Radiation hardened, (dose rate 50 to 300 rad(Si)/s), quad differential line receiver, LVDS
08	RHFLVDS32	Radiation hardened, LVDS quad differential line receiver.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad locations and related electrical functions, interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
02, 03, 04, 05	A-1
07, 08	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02, 03, 04, 05	A-1
07, 08	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
02, 03, 04, 05	A-1
07, 08	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
02, 03, 04, 05	A-1
07, 08	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1 and A-2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1 and A-2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1 and A-2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1 and A-2.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.3 and 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

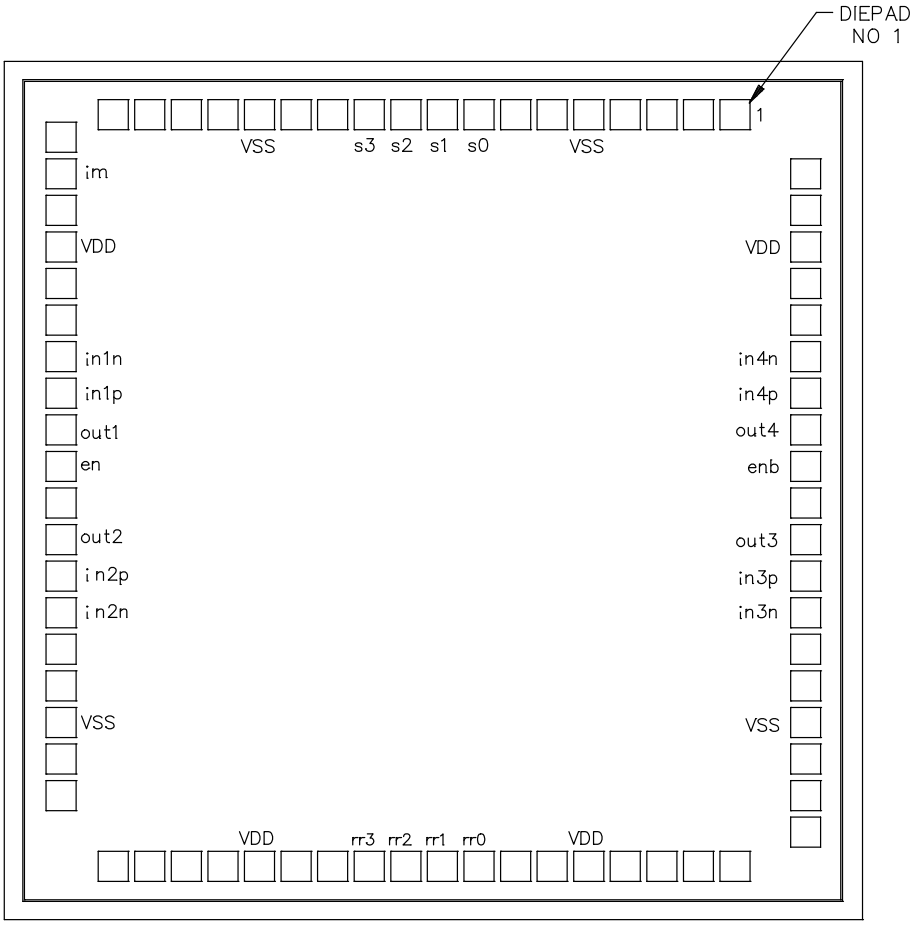
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: On a wafer lot basis, the die manufacturer will determine the bonding for die pads ro3, r02, ro1, ro0, rr3, rr2, rr1, rr0. These pads must be bonded to V_{CC} or GND per the die manufacturer provided bonding instructions. Die pad one located counter clockwise next to fiducial "1" marking. Die pads count counter clockwise with every fifth die pad fiducially marked.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 0.085 inch X 0.085 inch
Die thickness: 17.5 +/-0.5 mils

Interface materials.
Top metallization: Al 99.5%, Cu 0.5% + barrier + W plugs
Backside metallization: None

Glassivation.
Type: Sio_2/Si_3N_4
Thickness: 2600Å < Thickness < 10,000Å

FIGURE A-1. Die bonding pad locations and electrical functions.

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: V_{SS}/Ground
Special assembly instructions: None

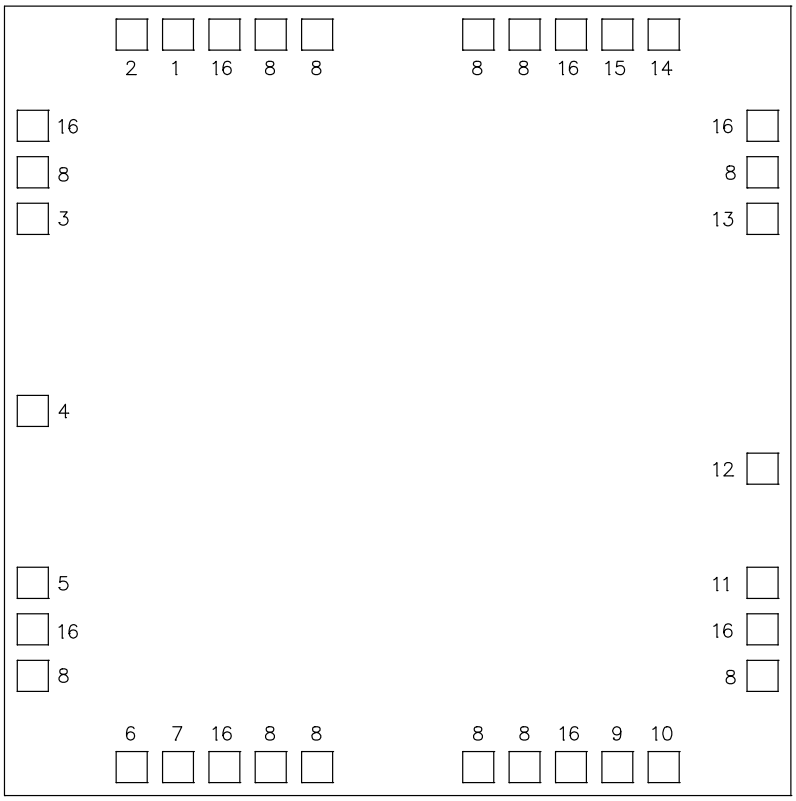
Units: Mils
Origin (0,0) = die Center

Die Pad	X center	Y center	Signal Name
1	29.3	35.9	N/C
2	25.7	35.9	N/C
3	22.2	35.9	N/C
4	18.6	35.9	N/C
5	15.1	35.9	VSS
6	11.5	35.9	N/C
7	8.0	35.9	N/C
8	4.5	35.9	Note 1
9	0.9	35.9	Note 1
10	-2.6	35.9	Note 1
11	-6.2	35.9	Note 1
12	-9.7	35.9	N/C
13	-13.3	35.9	N/C
14	-16.8	35.9	VSS
15	-20.4	35.9	N/C
16	-23.9	35.9	N/C
17	-27.4	35.9	N/C
18	-31.0	35.9	N/C
19	-35.9	34.2	N/C
20	-35.9	30.7	N/C
21	-35.9	27.1	N/C
22	-35.9	23.6	VDD
23	-35.9	20.0	N/C
24	-35.9	16.5	N/C
25	-35.9	12.9	RIN1-
26	-35.9	9.4	RIN1+
27	-35.9	5.9	ROUT1
28	-35.9	2.3	EN
29	-35.9	-1.2	N/C
30	-35.9	-4.8	ROUT2
31	-35.9	-8.3	RIN2+
32	-35.9	-11.9	RIN2-
33	-35.9	-15.4	N/C
34	-35.9	-19.0	N/C
35	-35.9	-22.5	VSS
36	-35.9	-26.0	N/C
37	-35.9	-29.6	N/C

Die Pad	X center	Y center	Signal Name
38	-31.0	-35.9	N/C
39	-27.4	-35.9	N/C
40	-23.9	-35.9	N/C
41	-20.4	-35.9	N/C
42	-16.8	-35.9	VDD
43	-13.3	-35.9	N/C
44	-9.7	-35.9	N/C
45	-6.2	-35.9	Note 1
46	-2.6	-35.9	Note 1
47	0.9	-35.9	Note 1
48	4.5	-35.9	Note 1
49	8.0	-35.9	N/C
50	11.5	-35.9	N/C
51	15.1	-35.9	VDD
52	18.6	-35.9	N/C
53	22.2	-35.9	N/C
54	25.7	-35.9	N/C
55	29.3	-35.9	N/C
56	35.9	-33.1	N/C
57	35.9	-29.6	N/C
58	35.9	-26.0	N/C
59	35.9	-22.5	VSS
60	35.9	-19.0	N/C
61	35.9	-15.4	N/C
62	35.9	-11.9	RIN3-
63	35.9	-8.3	RIN3+
64	35.9	-4.8	ROUT3
65	35.9	-1.2	N/C
66	35.9	2.3	EN/
67	35.9	5.9	ROUT4
68	35.9	9.4	RIN4+
69	35.9	12.9	RIN4-
70	35.9	16.5	N/C
71	35.9	20.0	N/C
72	35.9	23.6	VDD
73	35.9	27.1	N/C
74	35.9	30.7	N/C

NOTE 1: Contact factory for bonding information on these pads.

FIGURE A-1. Die bonding pad locations and electrical functions – continued.



Pad numbers are those of the flat pack pin numbers

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2100 µm X 2100 µm
Die thickness: 280 +/-25 µm
Bond pad size: 80 µm X 80 µm

Interface materials.
Top metallization: Al Cu (0.5% Cu)
Backside metallization: None

Glassivation.
Type: Phosphorous Silicon Glass (PSG) 5000Å, Nitride (SiN) 6000Å.

Substrate: Silicon

Assembly related information.
Substrate potential: V_{SS}/Ground
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

All dimensions are in Microns

Lead	Pad name	X =	Y =
2	A1	-734.03	980.0
1	B1	-584.03	980.0
16	AVCC1	-451.73	980.0
8	AGND1	-311.01	980.0
8	GNDESD	-201.01	980.0
8	GNDESD	201.01	980.0
8	AGND4	311.01	980.0
16	AVCC4	451.73	980.0
15	B4	584.03	980.0
14	A4	734.03	980.0
16	DVCC4	980.0	737.5
8	DGND4	980.0	599.5
13	Y4	980.0	477.5
12	Gb	980.0	-174.2
11	Y3	980.0	-477.5
16	DVCC3	980.0	-599.5
8	DGND3	980.0	-737.5
10	A3	734.03	-980.0
9	B3	584.03	-980.0
16	AVCC3	451.73	-980.0
8	AGND3	311.01	-980.0
8	GNDESD	201.01	-980.0
8	GNDESD	-194.31	-980.0
8	AGND2	-304.31	-980.0
16	AVCC2	-445.03	-980.0
7	B2	-584.03	-980.0
6	A2	-727.33	-980.0
8	DGND2	-980.0	-737.5
16	DVCC2	-980.0	-599.5
5	Y2	-980.0	-477.5
4	G	-980.0	-31.2
3	Y1	-980.0	477.5
8	DGND1	-980.0	599.5
16	DVCC1	-980.0	737.5

Note: Placement values correspond to each pad center coordinates. Pad placement origin is the center of the die.

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-11-02

Approved sources of supply for SMD 5962-98652 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9865201QFA	27014	DS90LV032AW-QML
5962-9865201QXA	3/	DS90LV032AWGQML
5962H9865202Q9A	65342	UT54LVDS032LV_QDIE
5962H9865202QYA	65342	UT54LVDS032LVUCA
5962H9865202QYC	65342	UT54LVDS032LVUCC
5962H9865202V9A	65342	UT54LVDS032LV_VDIE
5962H9865202VYA	65342	UT54LVDS032LVUCA
5962H9865202VYC	65342	UT54LVDS032LVUCC
5962R9865203Q9A	65342	UT54LVDS032LV_QDIE
5962R9865203QYA	65342	UT54LVDS032LVUCA
5962R9865203QYC	65342	UT54LVDS032LVUCC
5962R9865203V9A	65342	UT54LVDS032LV_VDIE
5962R9865203VYA	65342	UT54LVDS032LVUCA
5962R9865203VYC	65342	UT54LVDS032LVUCC
5962H9865204Q9A	65342	UT54LVDS032LVE_QDIE
5962H9865204QYA	65342	UT54LVDS032LVEUCA
5962H9865204QYC	65342	UT54LVDS032LVEUCC
5962H9865204V9A	65342	UT54LVDS032LVE_VDIE
5962H9865204VYA	65342	UT54LVDS032LVEUCA
5962H9865204VYC	65342	UT54LVDS032LVEUCC
5962R9865205Q9A	65342	UT54LVDS032LVE_QDIE
5962R9865205QYA	65342	UT54LVDS032LVEUCA
5962R9865205QYC	65342	UT54LVDS032LVEUCC
5962R9865205V9A	65342	UT54LVDS032LVE_VDIE
5962R9865205VYA	65342	UT54LVDS032LVEUCA
5962R9865205VYC	65342	UT54LVDS032LVEUCC

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9865206VYC	F8859	RH-LVDS32K
5962F9865207VZA	F8859	RHFLVDS32AK02V
5962F9865207VZC	F8859	RHFLVDS32AK01V
5962F9865207V9A	F8859	RHFLVDS32AD2V
5962F9865208VZA	F8859	RHFLVDS325K02V
5962F9865208VZC	F8859	RHFLVDS325K01V
5962F9865208V9A	F8859	RHFLVDS325D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Dr PO Box 58090 Santa Clara, CA 95052-8090
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486
F8859	STMicroelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE