

# MC10E141

## 5 V ECL 8-Bit Shift Register

### Description

The MC10E/100E141 is an 8-bit full-function shift register. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs  $D_0 - D_7$  accept parallel input data, while DL/DR accept serial input data for left/right shifting. The  $Q_n$  outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any  $Q$  output not used should be left unterminated.

The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

The 100 Series contains temperature compensation.

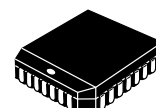
### Features

- 700 MHz Min. Shift Frequency
- 8-Bit
- Full-Function, Bi-Directional
- Asynchronous Master Reset
- Pin-Compatible with E241
- PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V to }5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection:
  - ◆ > 2 kV Human Body Model
  - ◆ > 200 V Machine Model
- Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)  
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 565 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



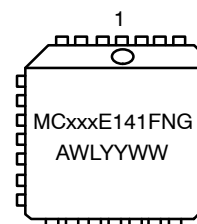
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PLCC-28  
FN SUFFIX  
CASE 776-02

### MARKING DIAGRAM\*



xxx = 10  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

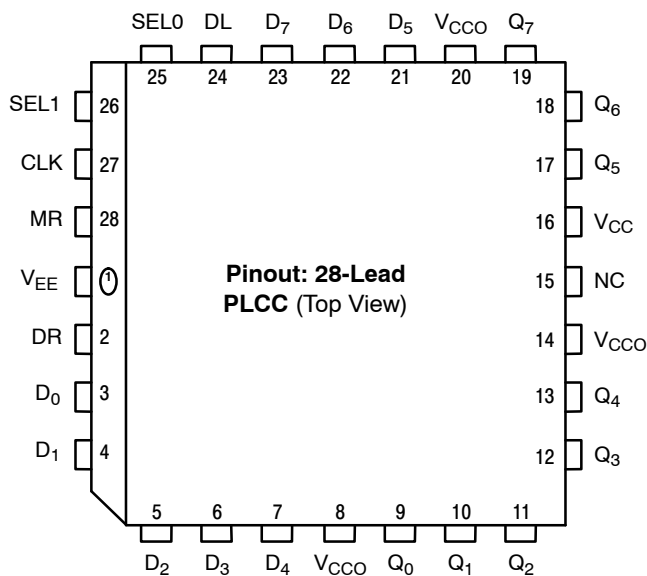
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC10E141FNG	PLCC-28 (Pb-Free)	37 Units / Tube
MC10E141FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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\* All V<sub>CC</sub> and V<sub>CCO</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub>, V<sub>CCO</sub>, and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Table 1. PIN DESCRIPTION**

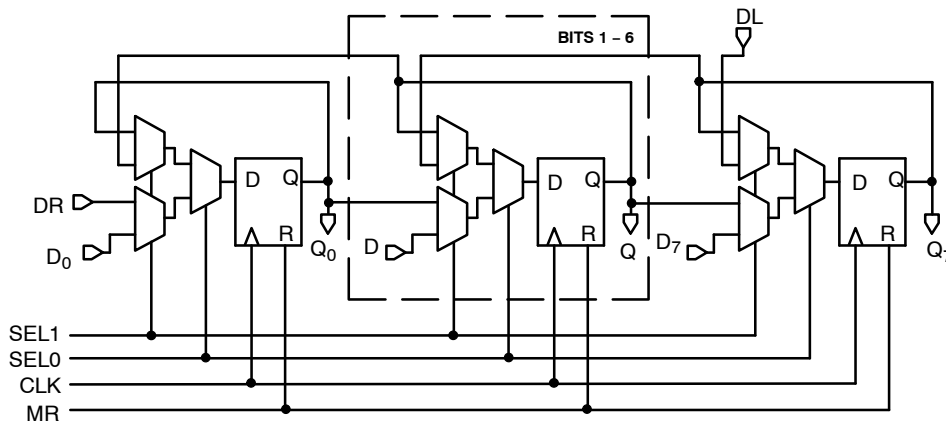
PIN	FUNCTION
D <sub>0</sub> - D <sub>7</sub>	ECL Parallel Data Inputs
DL, DR	ECL Serial Data Inputs
SEL0, SEL1	ECL Mode Select In Inputs
CLK	ECL Clock
Q <sub>0</sub> - Q <sub>7</sub>	ECL Data Outputs
MR	ECL Master Reset
V <sub>CC</sub> , V <sub>CCO</sub>	Positive Supply*
V <sub>EE</sub>	Negative Supply
NC	No Connect

\*From V<sub>CC</sub> pin to each V<sub>CCO</sub> pin is an internal 100 Ω resistor.

**Table 2. FUNCTION TABLE**

SEL0	SEL1	FUNCTION
L	L	Load
L	H	Shift Right (D <sub>n</sub> to D <sub>n+1</sub> )
H	L	Shift Left (D <sub>n</sub> to D <sub>n-1</sub> )
H	H	Hold

**Figure 1. 28-Lead Pinout**



**Figure 2. Logic Diagram**

**Table 3. EXPANDED FUNCTION TABLE**

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

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**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$T_A$	Operating Temperature Range			0 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfm 500 lfm	PLCC-28 PLCC-28	63.5 43.5	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
$V_{EE}$	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V
$T_{sol}$	Wave Solder (Pb-Free)			265 265	°C

**Table 5. 10E SERIES PECL DC CHARACTERISTICS** ( $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		131	181		131	181		131	181	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
$V_{IL}$	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary -0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to  $V_{CC} - 2.0\text{ V}$ .

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**Table 6. 10E SERIES NECL DC CHARACTERISTICS** ( $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		131	181		131	181		131	181	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
$V_{IH}$	Input HIGH Voltage	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
$V_{IL}$	Input LOW Voltage	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 100E SERIES PECL DC CHARACTERISTICS** ( $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		131	181		131	181		151	181	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
$V_{IH}$	Input HIGH Voltage	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
$V_{IL}$	Input LOW Voltage	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

**Table 8. 100E SERIES NECL DC CHARACTERISTICS** ( $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		131	181		131	181		151	181	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
$V_{IH}$	Input HIGH Voltage	-1165	-1025	-880	-1165	-1025	-880	-1165	-880	-1025	mV
$V_{IL}$	Input LOW Voltage	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1475	-1645	mV
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

# MC10E141

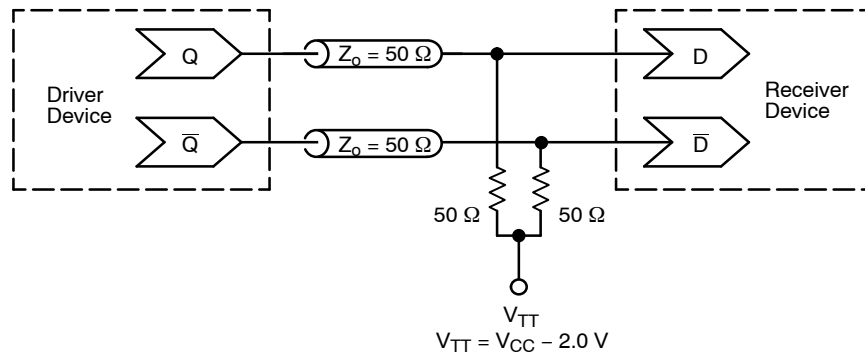
**Table 9. AC CHARACTERISTICS** ( $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{SHIFT}}$	Max. Shift Frequency	700	900		700	900		700	900		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay To Output Clk MR	625 600	750 725	975 975	625 600	750 725	975 975	625 600	750 725	975 975	ps
$t_s$	Setup Time D SEL0 SEL1	175 350 300	25 200 150		175 350 300	25 200 150		175 350 300	25 200 150		ps
$t_h$	Hold Time D SEL0 SEL1	200 100 100	-25 -200 -150		200 100 100	-25 -200 -150		200 100 100	-25 -200 -150		ps
$t_{\text{RR}}$	Reset Recovery Time	900	700		900	700		900	700		ps
$t_{\text{PW}}$	Minimum Pulse Width Clk, MR	400			400			400			ps
$t_{\text{SKEW}}$	Within-Device Skew (Note 2)		60			60			60		ps
$t_{\text{JITTER}}$	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
$t_r$ $t_f$	Rise/Fall Times (20–80%)	300	525	800	300	525	800	300	525	800	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 10 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .  
100 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .
- Within-device skew is defined as identical transitions on similar paths through a device.

## MC10E141



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

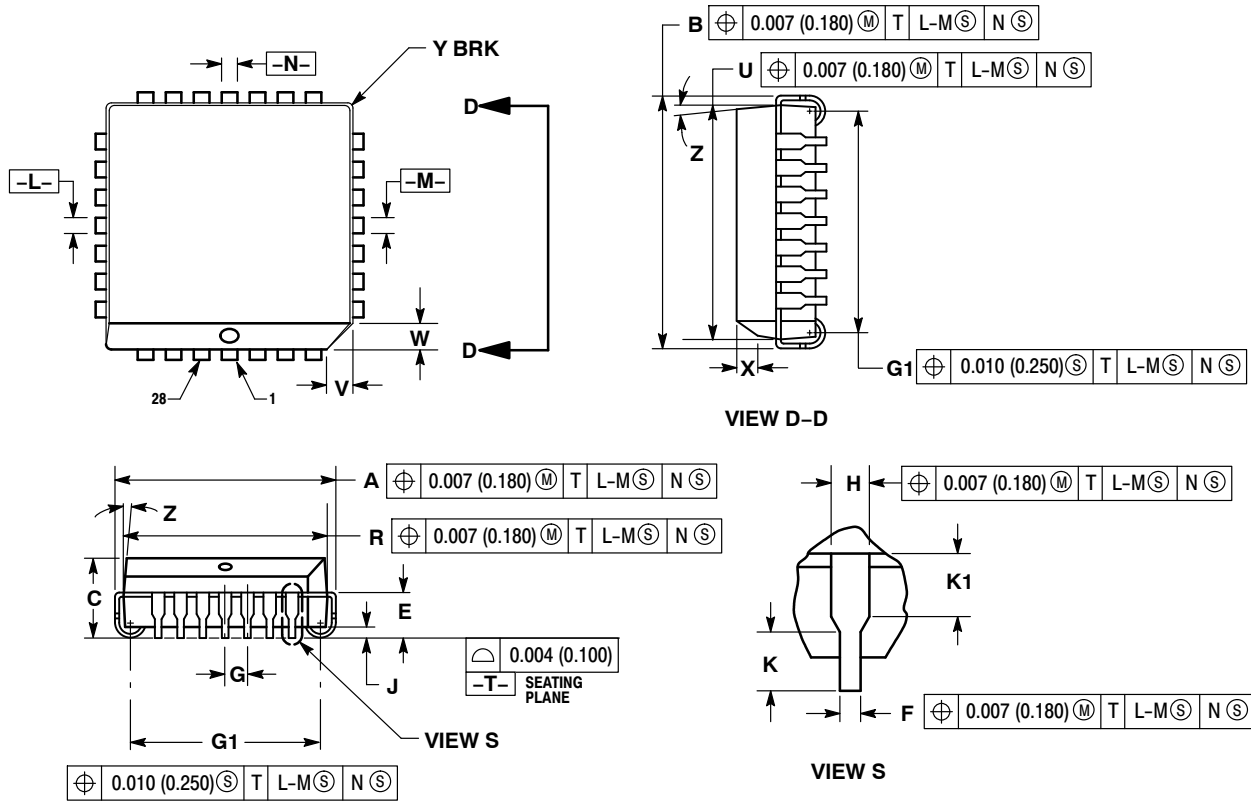
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10E141

## PACKAGE DIMENSIONS

28 LEAD PLLC  
FN SUFFIX  
CASE 776-02  
ISSUE F




### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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