



UTOPIA ADSL2+ SOLUTION FOR CPE

DATA BRIEF

1 Applications

- Medium/high-end routers
- Business routers with modular and/or multiple WAN access
- Security applications
- Voice and data gateways
- Wireless access points
- Convergence of gateways and IP set-top-box
- Home servers with storage capabilities, smart card interfaces, unified mailboxes, etc

2 Features

- Multi-standard capability
 - G.992.1 annexA, B
 - G.992.2 . g.Lite
 - G.992.3 annexA, B, I, J, L (extended reach), M (double upstream)
 - G.992.4 . g.Lite.bis
 - G.992.5 annexA, B, I, J, M
 - ANSI T1.413 Issue2
 - ETSI TS 101 388 ADSL-over-ISDN
- Downstream bit rates up to 24 Mbps and upstream bit rates up to 2.5 Mbps
- Designed to meet standardized and specific operator requirements.
- CATII functionality with echo cancellation and Trellis coding
- Word wide reference for interoperability
- Integrated of line driver, filtering and voltage regulation
- Embedded controller allowing easy, straight forward integration with external network processors

3 Utopia Description

The new ADSL2+ standards will accelerate broadband applications beyond e-mail, web browsing and data streaming. Internet Service Providers are exploring several ways to increase their revenues by offering new services and applications, and enlarging their customer base. This can be accomplished using the increased quantity of new

Figure 1. Packages

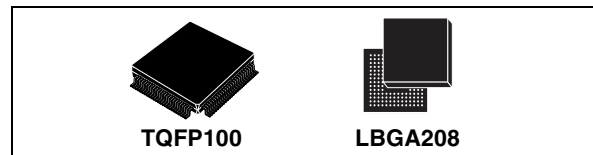


Table 1. Order Codes

Part Number	Package
ST20184	TQFP100
ST20196	LPGA208

features and annexes included in ADSL2+ products.

- Triple-play product offerings.
- On a 24+Mbps copper line link, several high-definition video channels can be broadcasted with new options offered to manage different latency paths.

Increased subscribers base through extended reach capabilities.

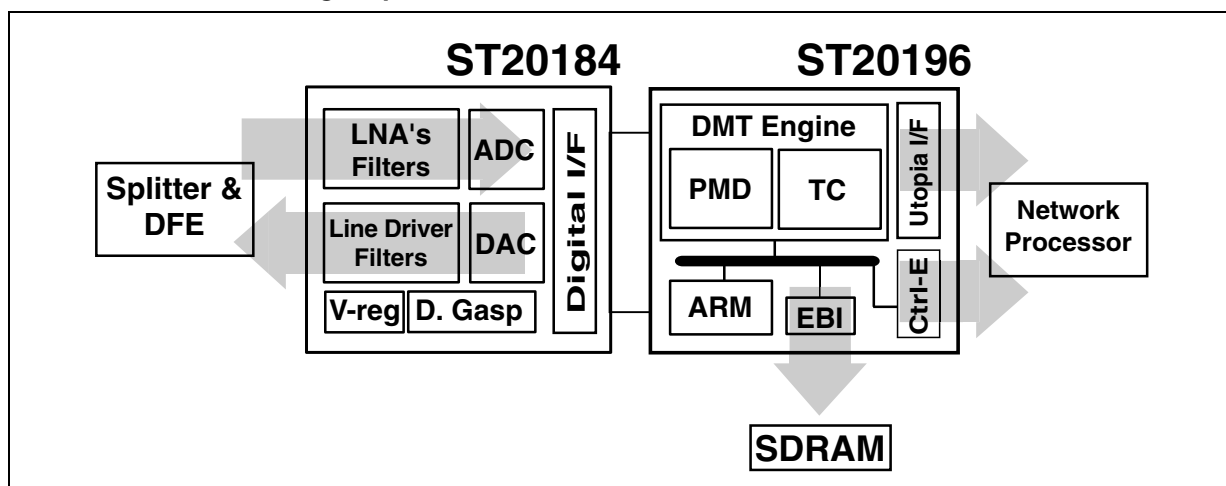
Reduced field deployment issues due to enhanced diagnostics capabilities and improved interoperability.

Increased upstream speeds at lower costs for teleworking and business symmetrical transmission segments. By implementing bonding, both upstream and downstream bit-rates can be doubled or further multiplied for high-end business applications.

The chipset allows OEM/ODM designers to address the new services and applications needed for the residential and SOHO markets up to the large business segment. The chipset consists of a new generation analog front-end chip (ST20184) and digital chip (ST20196) integrating the DMT modem and dedicated controller. When used together with an external network processor, a flexible and scalable platform can be developed to handle the rapidly increasing bit rate demands and the continuous introduction of additional multimedia functionalities and sophisticated networking protocols. State-of-the-art ADSL2+ performance is

achieved due to a new generation analog front end chip that includes a high resolution ADC/DAC, integrated and programmable filters and low noise/high linearity amplifiers and line driver. Advanced equalization techniques are developed both in the time and frequency domain (PTEQ) and are implemented both in the analog and digital part of the chipset. In addition, with the introduction of echo cancellation, digital clock recovery and innovative system algorithms, users receive best in class performance against the newest generation DSLAMs.

Figure 2. The ST20190 is available with multi-mode software ranging from ADSL2+ for short loops to ADSL2 annexL for long loops.



4 Chipset Functions

The functions performed by each IC are as follows:

4.1 Analog front-end (ST20184) description

Compared to its widely deployed predecessors, the ST20184 has been designed in a shorter gate-length, advanced analog CMOS technology. Due to the transition in semiconductor technology and the introduction of advanced design techniques, CAD tools and simulation software, the performance has been optimized to define the next generation requirements.

The ST20184 contains a powerful 5V line driver. In the receiving path great care has been taken to lower the noise floor, increase the dynamic range and linearity of the programmable gain amplifiers (LNAs). In both Rx and Tx path tunable, active filters have been integrated to deal with the different frequency allocations for upstream and downstream bands. The analog/digital conversions are accomplished by a more than 14bit resolution ADC and DAC. External BOM cost reduction, a 2.5V voltage regulator and dying gasp comparator are integrated and digital clock recovery or time domain interpolation has been implemented only requiring a X-tal to be attached to the chip.

- Package : TQFP-100
- Supply voltages: 3.3V and 5V
- Temperature range: -40°C to 85°C
- Typical power consumption 900 mW

4.2 DMT engine (ST20196) description

The ST20196 is designed in main stream digital CMOS technology. The major building blocks are the DMT engine including the PMD and TC layer, the ARM. microcontroller and the different interfaces, including Utopia levels I&II, Ctrl-E, interfacing to the ST20184 and memory.

The DMT engine is compliant with the new ADSL2+ standards and supports features like diagnostics mode, enhanced power management (L2), 1 bit constellation, relocatable and modulated pilot, etc. In ad-

dition to the mandatory new features, the DMT engine includes some advanced techniques that differentiate the product from its competitors; these include innovative Per Tone Equalizer (PTEQ) optimizing short loop and bridge tap performances and reducing the impact of RFI in ADSL2+ mode. A high performance echo canceller (EC) and a fully digital clock recovery scheme (TDI) further differentiate the ST20190 ADSL2+ performances.

To be prepared for triple-play applications, a flexible TC-layer has been implemented. The cached ARM micro-controller allows further improvement of the performances and allows fast and simple integration with major third party network processors. Data is exchanged over the Utopia level 1 or 2 interface and the commands via the ST Ctrl-E modem control command protocol.

- Package : LBGA-208
- Supply voltages: 3.3V and 1.2V
- Temperature range: -40°C to 85°C
- Typical power consumption: 700mW

5 Development support

ST Utopia chipsets are designed for OEM customers to minimize product development effort, to reduce the implementation risks and to decrease time-to-market. Ease of integration has been implemented for system designs. Including the use of standard Utopia and Ctrl-E interface for data and control, modem software runs on the embedded controller separated from other system-related and application-specific functions. The boundary between the two domains is provided by means of a simple modem control protocol (CTRL-E).

This “packaged modem” approach provides a self-contained ADSL modem solution, allowing system manufacturers to concentrate on system issues.

Customers are supported through a complete kit which includes datasheets, application notes, schematics, bill of materials, layout information and modem software. In addition PC test and control software is available to ease the evaluation and debugging phase.

6 Revision History

Table 2. Revision History

Date	Revision	Description of Changes
June 2004	1	First Issue.
May 2005	2	Updated textes and figures.

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