REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29				
REV STATUS				REV															
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
15-01-29

REVISION LEVEL

MICROCIRCUIT, LINEAR, DUAL 4 X 4, 400 MBPS CROSSPOINT SWITCH, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-14234**

SHEET 1 OF 29

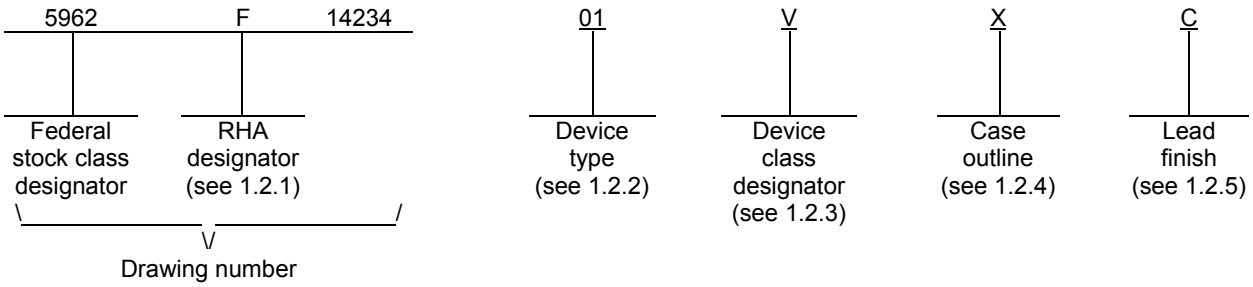
DSCC FORM 2233
APR 97

5962-E466-14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHFLVDS2281	Radiation hardened dual 4 x 4, 400 Mbps cross point switch

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	64	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	4.8 V
Input voltage (IN+, IN-, CLK+, CLK-)	-5 V to 6 V
Enable input voltage (EN, EN/)	-0.3 V to 4.8 V
Power dissipation (P_D)	1040 mW 2/
Junction temperature (T_J)	+150°C 3/
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	21°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	120°C/W

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD})	3 V to 3.6 V
DC input voltage, receiver inputs (V_{IN})	-4 V to 5.0 V
DC input voltage, logic inputs (V_{IN})	0 V to V_{DD} for EN, SEL
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (effective dose rate = 0.50 rad(Si)/s)	300 krads(Si)/s 4/
Single event phenomenon (SEP):	
No single event latchup (SEL) occurs at effective LET (see 4.4.4.2)	≤ 120 MeV/mg/cm^2

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Power dissipation measured at T_A = +25°C and derate 8.32 mW/°C above T_A = +25°C.

3/ Maximum junction temperature may be increased to +175°C during burn-in and life test.

4/ Device type 01 is irradiated at a dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose as specified. The effective dose rate after extended room temperature anneal is 0.5 rad(Si)/s for device type 01, per MIL-STD-883, method 1019, condition A, paragraph 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit of die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC specifications (EN)							
High level input voltage	V_{IH}		1,2,3	01	2.0	V_{CC}	V
Low level input voltage	V_{IL}		1,2,3	01	GND	0.8	V
High level input current	I_{IH}	V_{IN} = 3.6 V, V_{DD} = 3.6 V	1,2,3	01	-10	+10	µA
Low level input current	I_{IL}	V_{IN} = 0 V, V_{DD} = 3.6 V	1,2,3	01	-10	+10	µA
Input clamp voltage	V_{CL}	I_{CL} = -18 mA	1,2,3	01		-1.5	V
Cold spare leakage	I_{CS}	V_{IN} = 3.6 V, V_{DD} = V_{SS}	1,2,3	01	-10	+10	µA
LVDS output DC specifications (OUT+, OUT-)							
Differential output voltage	V_{OD}	R_L = 100 Ω, see figure 5	1,2,3	01	250	400	mV
Change in V_{OD} between complimentary output states	ΔV_{OD}	R_L = 100 Ω	1,2,3	01		10	mV
Offset voltage	V_{OS}	R_L = 100 Ω, see figure 5	1,2,3	01	1.125	1.45	V
Change in V_{OS} between complimentary output states	ΔV_{OS}	R_L = 100 Ω	1,2,3	01		25	mV
Output three-state current	I_{OZ}	Three-state output, V_{DD} = 3.6 V, V_{OUT} = V_{DD} or GND	1,2,3	01		±10	µA
Cold sparing leakage current	I_{CSOUT}	V_{OUT} = 3.6 V, V_{DD} = V_{SS}	1,2,3	01	-50	+50	µA
Output short circuit 3/ 4/ current	I_{OS}	V_{OUT+} or V_{OUT-} = 0 V	1,2,3	01		-9	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVDS receiver dc specifications (IN+, IN-)							
Differential input high 4/ threshold voltage	V_{TH}	V_{CM} = +1.2 V	1,2,3	01		+100	mV
		-4 V < V_{CM} < +5 V				+130	
Differential input low 4/ threshold voltage	V_{TL}	V_{CM} = +1.2 V	1,2,3	01	-100		mV
		-4 V < V_{CM} < +5 V			-130		
Common mode voltage range	V_{CMR}	V_{ID} = 200 mV	1,2,3	01	-4	+5	V
Input current	I_{IN}	V_{IN} = - 4 V to + 5 V, V_{CC} = 3.6 V	1,2,3	01	-70	+70	µA
Cold sparing leakage current	I_{CSIN}	V_{IN} = -4 V to +5 V, V_{CC} = 3.6 V	1,2,3	01	-60	+60	µA
Supply current section							
Total supply current	I_{CCD}	R_L = 100 Ω	1,2,3	01		80	mA
Three-state supply current	I_{CCZ}	EN1 – EN8, ENCK = V_{SS}	1,2,3	01		20	mA
Functional test							
Functional test		See 4.4.1c	7,8	01			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC switching characteristics.							
Input to SEL setup time 4/ 5/	t_{SET}	See figures 6 and 7	9,10,11	01	1.6		ns
Input to SEL hold time 4/ 5/	t_{HOLD}	See figures 6 and 7	9,10,11	01	1.5		ns
SEL to switch output 4/	t_{SWITCH}	See figures 6 and 7	9,10,11	01		5.0	ns
Disable time (active to three-state) high to Z 4/	t_{PHZ}	See figures 8 and 9	9,10,11	01		2.8	ns
Disable time (active to three-state) low to Z 4/	t_{PLZ}	See figures 8 and 9	9,10,11	01		2.8	ns
Enable time (three-state to active) Z to high 4/ 6/	t_{PZH}	See figures 8 and 9	9,10,11	01		2.5	ns
Enable time (three-state to active) Z to low 4/ 6/	t_{PZL}	See figures 8 and 9	9,10,11	01		2.5	ns
Output low-to-high transition time, 20 % to 80 % 7/	t_{LHT}	See figures 10 and 9	9,10,11	01		1.2	ps
Output high-to-low transition time, 80 % to 20 % 7/	t_{HLT}	See figures 10 and 9	9,10,11	01		1.2	ps
Propagation low to high delay	t_{PLHD}	R_L = 100 Ω, C_L = 10 pF, see figures 9 and 11	9,10,11	01		4.2	ns
Propagation high to low delay	t_{PHLD}	R_L = 100 Ω, C_L = 10 pF, see figures 9 and 11	9,10,11	01		4.2	ns
Pulse skew t_{PHLD} - t_{PLHD}	t_{SKEW}	See figures 9 and 11	9,10,11	01		600	ps
Output channel-to-channel skew	t_{CCS}	See figures 9 and 12	9,10,11	01		600	ps

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

1/ RHA device type 01 supplied to this drawing has been characterized through all levels P, L, R, and F of irradiation. However device type 01 tested at RHA level P, L, R and F.

Device type 01 are irradiated at dose rate = 50 - 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose as specified. The effective dose rate after extended room temperature anneal is 0.5 rad(Si)/s for device type 01 per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Unless otherwise specified, V_{DD} = 3.3 V ±0.3 V.

3/ Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

4/ Guaranteed by characterization only.

5/ t_{SET} and t_{HOLD} time specify that data must be in a stable state before and after SEL transition.

6/ Maximum t_{PZH} and t_{PZL} = 4.5 ns when En or ENCL = V_{DD} on another channel.

7/ Guaranteed by design.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Bias V_{CC} = 3.6 V for single event latchup (SEL) test No SEL occurs at effective linear energy transfer (LET)
01	No SEL	LET ≤ 120 MeV/mg/cm^2

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Tested at worst case operating temperature, T_A = +125°C ± 10°C for latch-up.

Case outline X

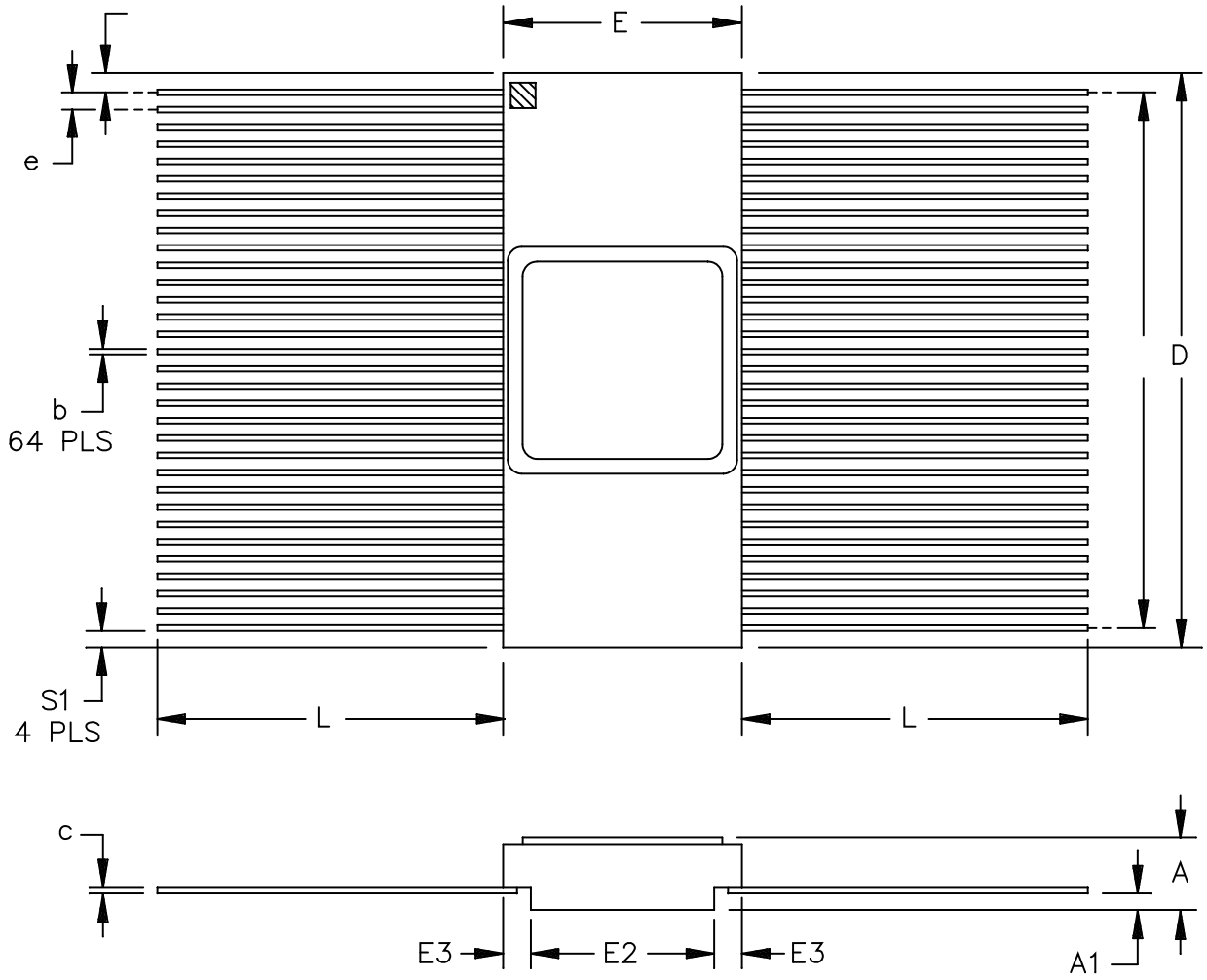


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.095	0.115	2.41	2.92
A1	0.013	--	0.33	--
b	0.007	0.009	0.18	0.23
c	0.006	0.010	0.15	0.25
D	0.823	0.839	20.91	21.31
E	0.340	0.350	8.64	8.89
E2	0.259	0.270	6.57	6.87
E3	0.040 BSC		1.02 BSC	
e	0.025 BSC		0.635 BSC	
L	0.49	0.51	12.45	12.95
S1	0.024 BSC		0.61 BSC	

Note:
The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - continued.

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	EN1	23	IN6+	45	OUT5+
2	IN1+	24	IN6-	46	SEL5
3	IN1-	25	V_{DD}	47	V_{SS}
4	EN2	26	V_{SS}	48	CLK OUT-
5	IN2+	27	IN7+	49	CLK OUT+
6	IN2-	28	IN7-	50	V_{DD}
7	V_{DD}	29	EN7	51	OUT4-
8	V_{SS}	30	IN8+	52	OUT4+
9	IN3+	31	IN8-	53	SEL4
10	IN3-	32	EN8	54	OUT3-
11	EN3	33	OUT8-	55	OUT3+
12	IN4+	34	OUT8+	56	SEL3
13	IN4-	35	SEL8	57	V_{SS}
14	EN4	36	OUT7-	58	V_{DD}
15	ENCK	37	OUT7+	59	OUT2-
16	CLK IN+	38	SEL7	60	OUT2+
17	CLK IN-	39	V_{SS}	61	SEL2
18	V_{SS}	40	V_{DD}	62	OUT1-
19	EN5	41	OUT6-	63	OUT1+
20	IN5+	42	OUT6+	64	SEL1
21	IN5-	43	SEL6	---	---
22	EN6	44	OUT5-	---	---

FIGURE 2. Terminal connections.

Terminal symbol	Number of pins	Description
INn+	8	Non-inverting LVDS input
INn-	8	Inverting LVDS input
OUTn+	8	Non-inverting LVDS output
OUTn-	8	Inverting LVDS output
ENn	8	A logic low on the enable puts the LVDS output into tri-state and reduces the supply current.
ENCK	1	A logic low on the enable puts the LVDS output into tri-state and reduces the supply current.
SEL	8	2:1 mux input select
V_{SS}	6	Ground
V_{DD}	5	Power supply
CLK IN+	1	Non-inverting clock LVDS input
CLK IN-	1	Inverting clock LVDS input
CLK OUT+	1	Non-inverting clock LVDS output
CLK OUT-	1	Inverting clock LVDS output

FIGURE 2. Terminal connections – Continued.

SEL1	SEL2	SEL3	SEL4	OUT1	OUT2	OUT3	OUT4	Mode
0	0	0	0	IN1	IN1	IN3	IN3	Splitter
0	0	0	1	IN1	IN1	IN3	IN4	Splitter/Repeater
0	0	1	0	IN1	IN1	IN1	IN1	Splitter
0	0	1	1	IN1	IN1	IN4	IN4	Splitter
0	1	0	0	IN1	IN2	IN3	IN3	Splitter/Repeater
0	1	0	1	IN1	IN2	IN3	IN4	Repeater
0	1	1	0	IN1	IN2	IN4	IN3	Repeater/Switch
0	1	1	1	IN1	IN2	IN4	IN4	Splitter/Repeater
1	0	0	0	IN2	IN2	IN2	IN2	Splitter
1	0	0	1	IN2	IN1	IN3	IN4	Switch/Repeater
1	0	1	0	IN2	IN1	IN4	IN3	Switch
1	0	1	1	IN3	IN3	IN3	IN3	Splitter
1	1	0	0	IN2	IN2	IN3	IN3	Splitter
1	1	0	1	IN2	IN2	IN3	IN4	Splitter/Repeater
1	1	1	0	IN4	IN4	IN4	IN4	Splitter
1	1	1	1	IN2	IN2	IN4	IN4	Splitter

FIGURE 3. Truth table.

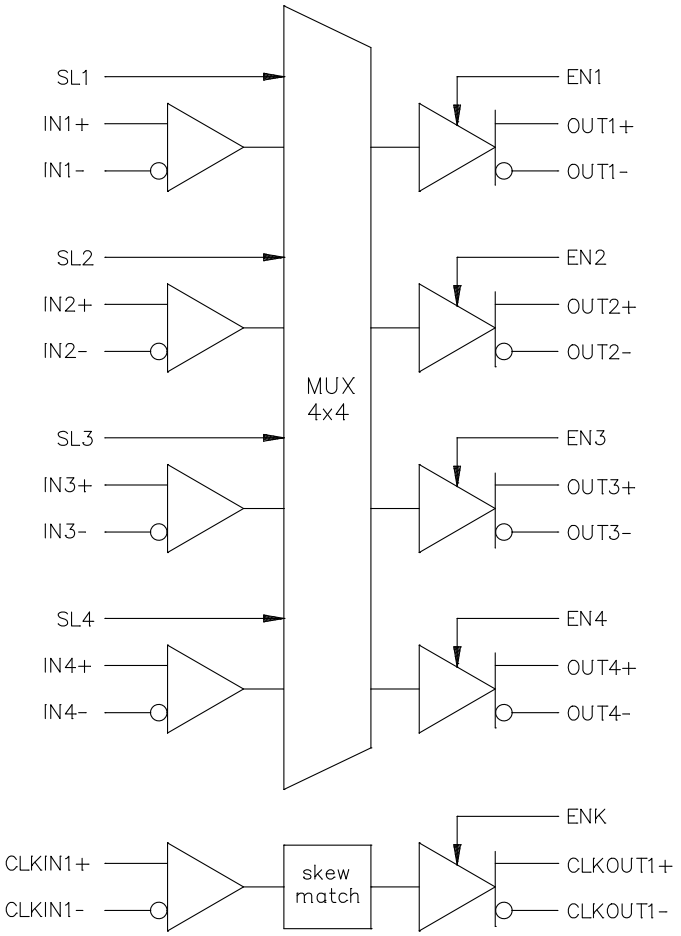


FIGURE 4. Block diagram.

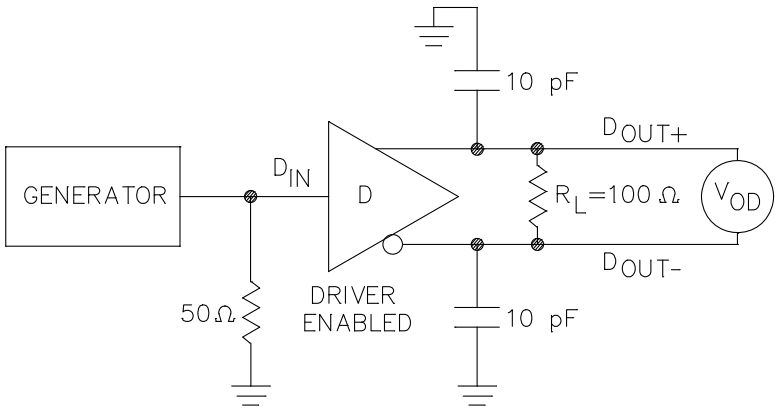


FIGURE 5. Driver V_{OD} and V_{OS} test circuit or equivalent circuit.

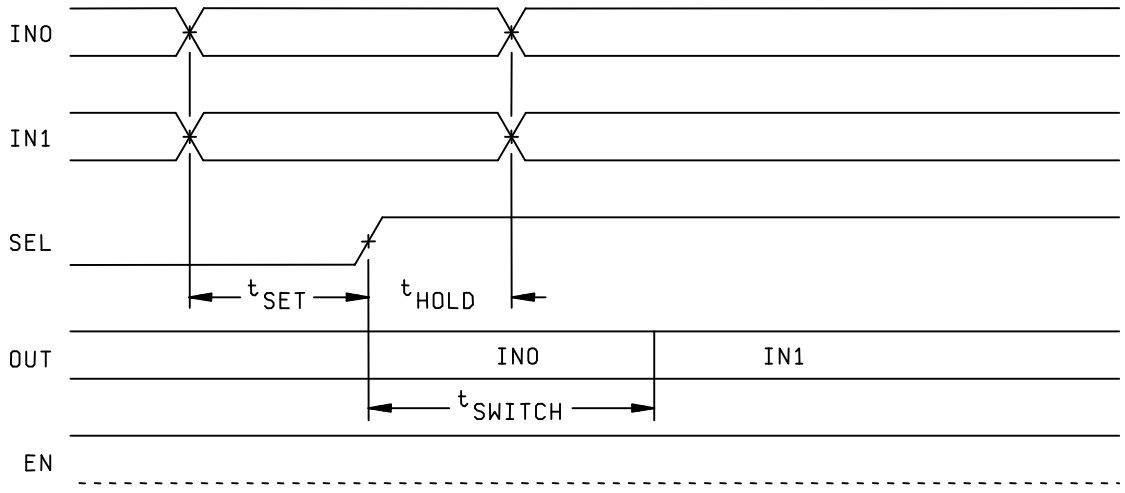


FIGURE 6. Input-to-select rising edge setup and hold times and mux switch time.

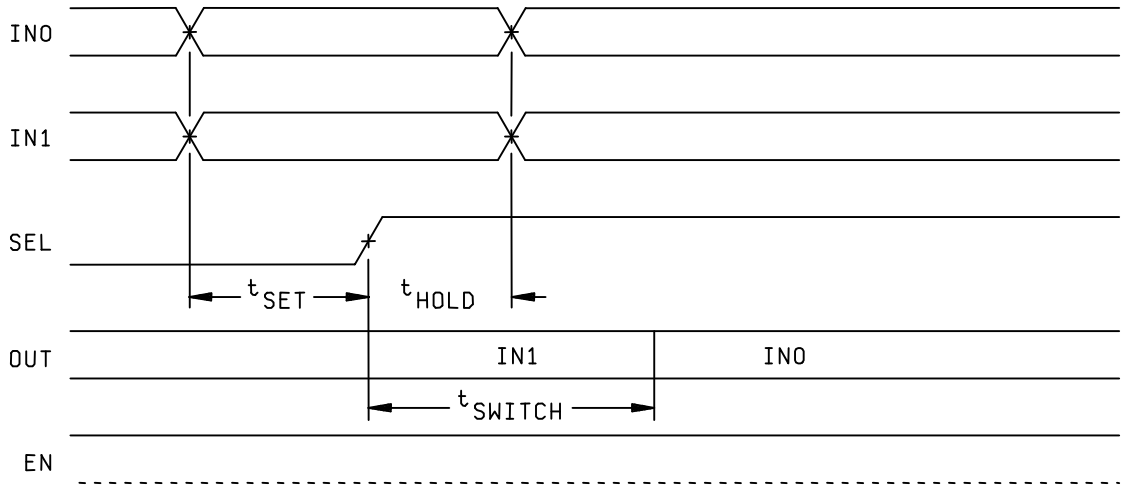


FIGURE 7. Input-to-select falling edge setup and hold times and mux switch time.

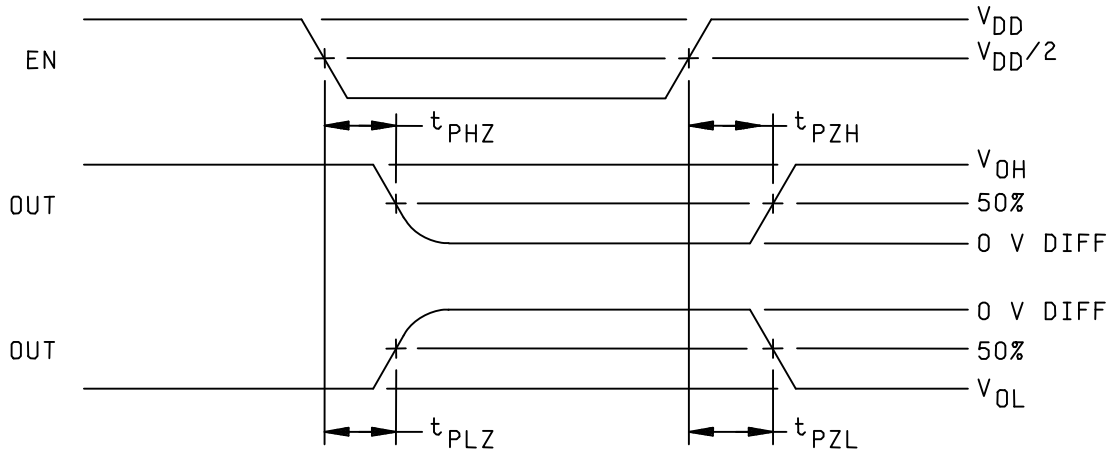


FIGURE 8. Output active to three-state and three-state to active.

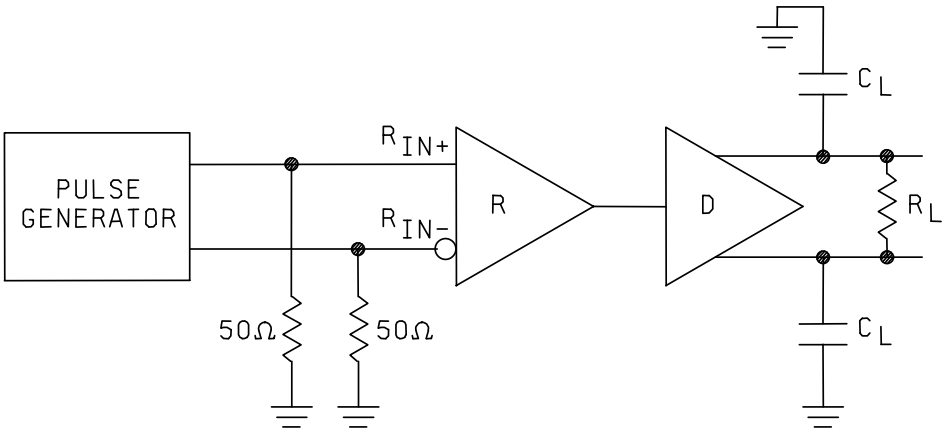


FIGURE 9. LVDS output load.

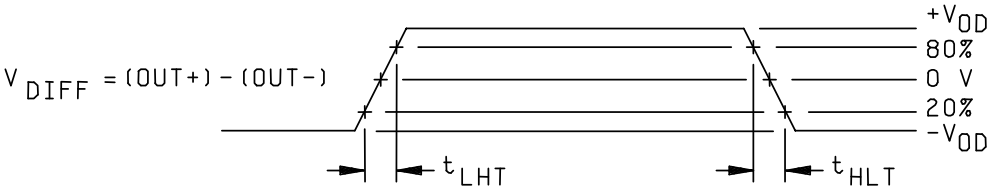


FIGURE 10. LVDS output transition time.

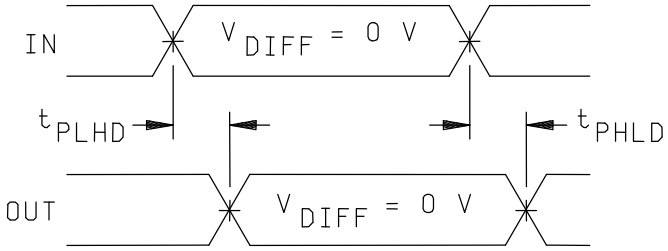


FIGURE 11. Propagation delay low-to-high and high-to-low.

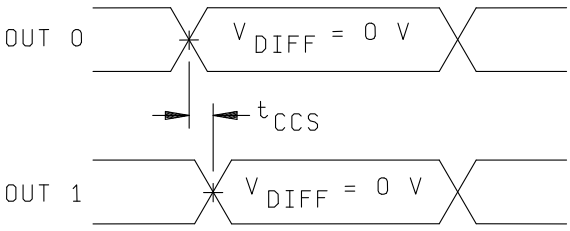


FIGURE 12. Output channel-to-channel skew in 1:2 splitter mode.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. (T_A = +25°C).

Parameters 1/	Symbol	Device type	Delta limit	Unit
Total supply current	I_{CCD}	01	±2	mA
Three state supply current	I_{CCZ}	01	±1	mA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A for device type 01 as specified herein (see 1.5).

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 3.0 V dc for the upset measurements and V_{DD} = 3.6 V dc for the latchup measurements.

g. For SEP test limits see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

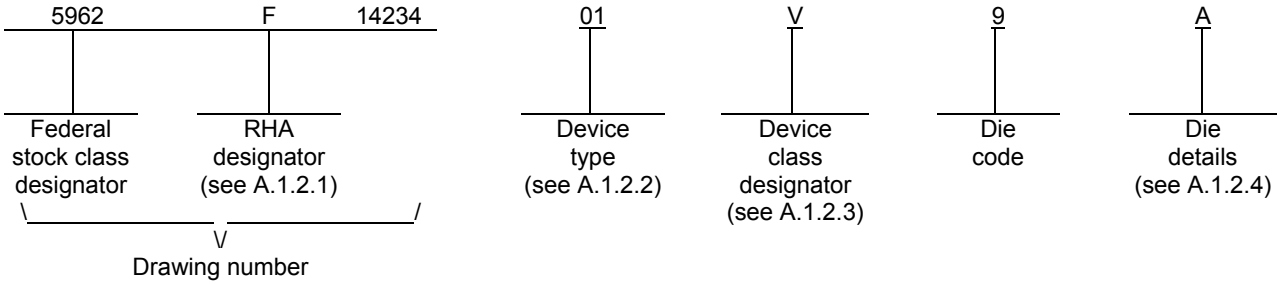
c. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-14234

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHFLVDS2281	Radiation hardened dual 4 x 4, 400 Mbps cross point switch

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

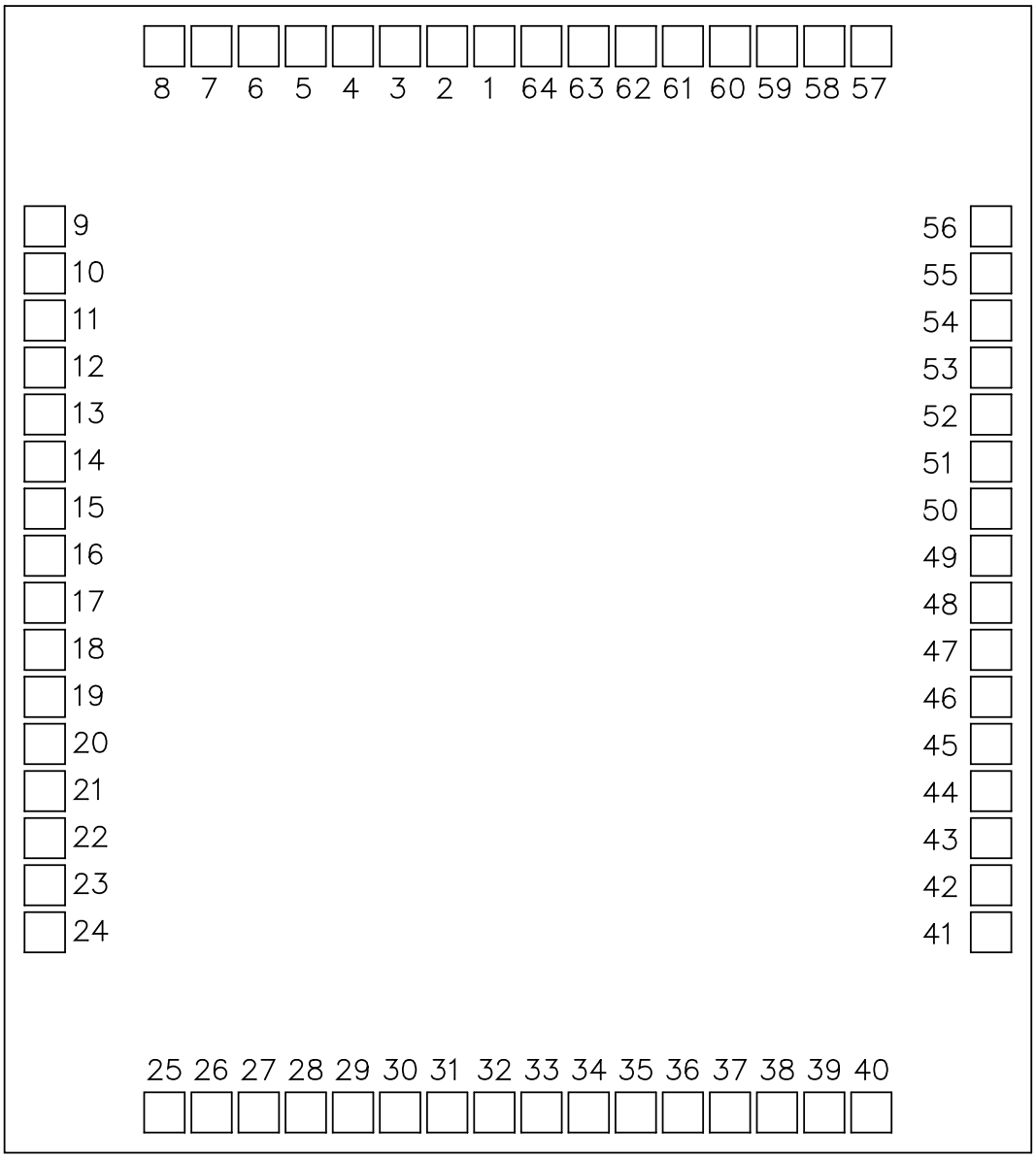


FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	2100 μm x 235 μm
Die thickness:	280 μm ± 25 μm
Pad size:	80 μm x 80 μm
Interface materials.	
Top metallization:	Al Cu (0.5% Cu)
Backside metallization:	None
Glassivation.	PSG (5000 Å) + nitride (6000 Å).
Substrate:	Silicon
Assembly related information.	
Substrate potential:	V_{SS} / ground
Special assembly instructions:	None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-01-29

Approved sources of supply for SMD 5962-14234 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1423401VXC	F8859	RHFLVDS2281K01V
5962F1423401V9A	F8859	RHFLVDS2281D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	STMicroelectronics 3, Rue de Suisse CS 60816 35208 Rennes Cedex 2 - France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.