



## PRESETTABLE DIVIDE-BY-N COUNTER

- MEDIUM SPEED OPERATION 10 MHz (Typ.) at  $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100nA$  (MAX) AT  $V_{DD} = 18V$   $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



### ORDER CODES

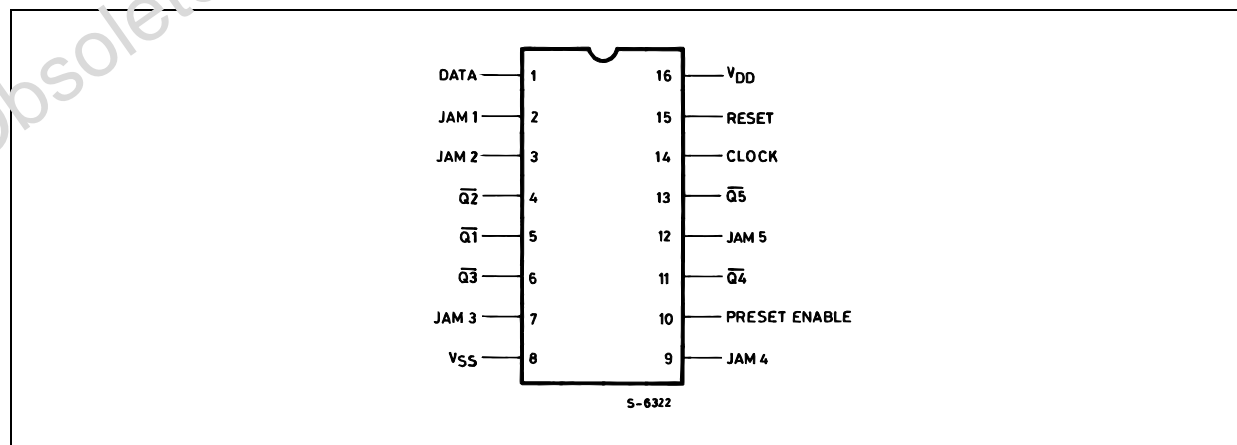
PACKAGE	TUBE	T & R
DIP	HCF4018BEY	
SOP	HCF4018BM1	HCF4018M013TR

### DESCRIPTION

The HCF4018B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4018B consists of 5 Johnson counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4 or 2 counter configuration can be implemented by feeding the  $\overline{Q}_5$ ,  $\overline{Q}_4$ ,  $\overline{Q}_3$ ,  $\overline{Q}_2$ ,  $\overline{Q}_1$  signals, respectively, back to the data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a HCF4011B gate

package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple HCF4018B units. The counter is advanced one count at the positive clock signal transition. Schmitt trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

### PIN CONNECTION



# HCF4018B

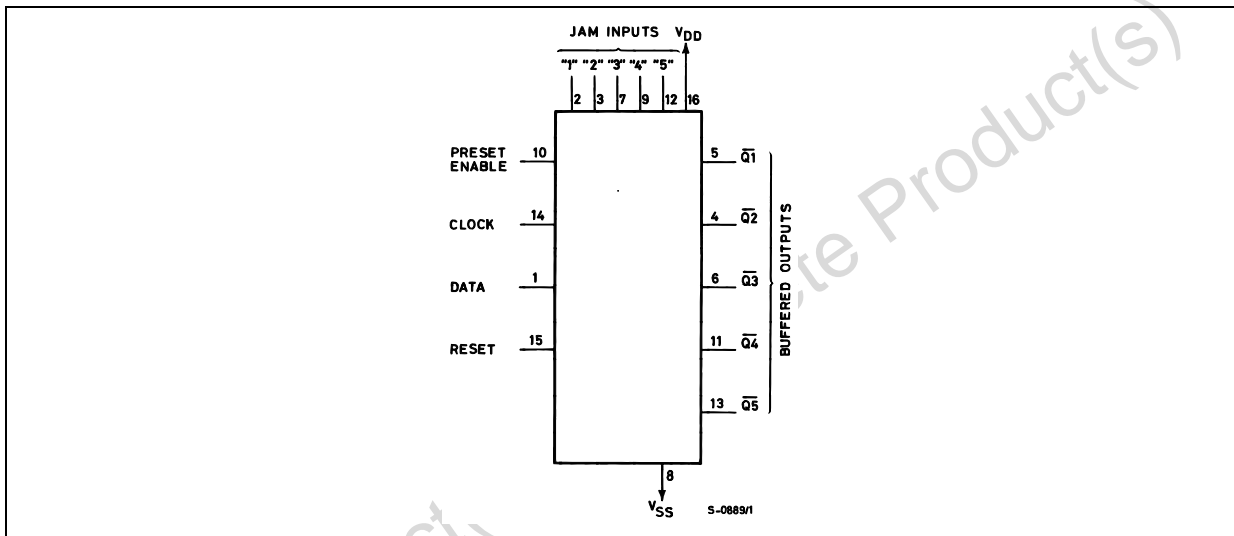
## INPUT EQUIVALENT CIRCUIT



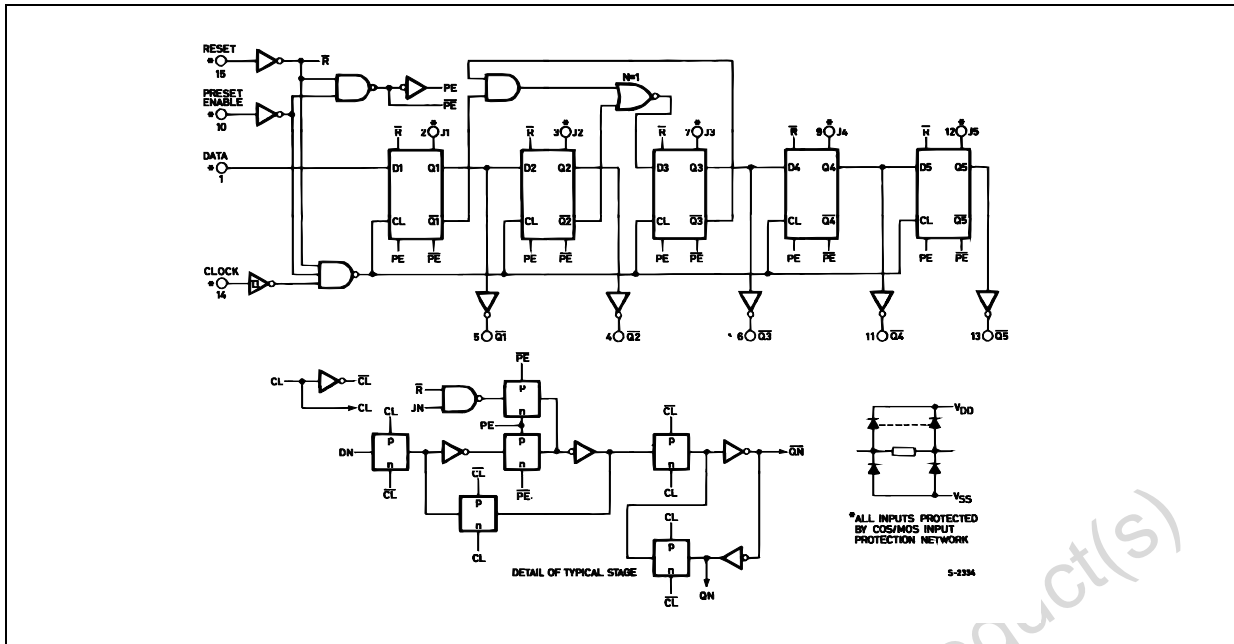
## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 3, 7, 9, 12	JAM1 to JAM5	Jam Inputs
1	DATA	Data Input
4, 5, 6, 11, 13	$\overline{Q1}$ to $\overline{Q5}$	Buffered Outputs
15	RESET	Reset Input
14	CLOCK	Clock Input
10	PRESET ENABLE	Preset Enable Input
8	$V_{SS}$	Negative Supply Voltage
16	$V_{DD}$	Positive Supply Voltage

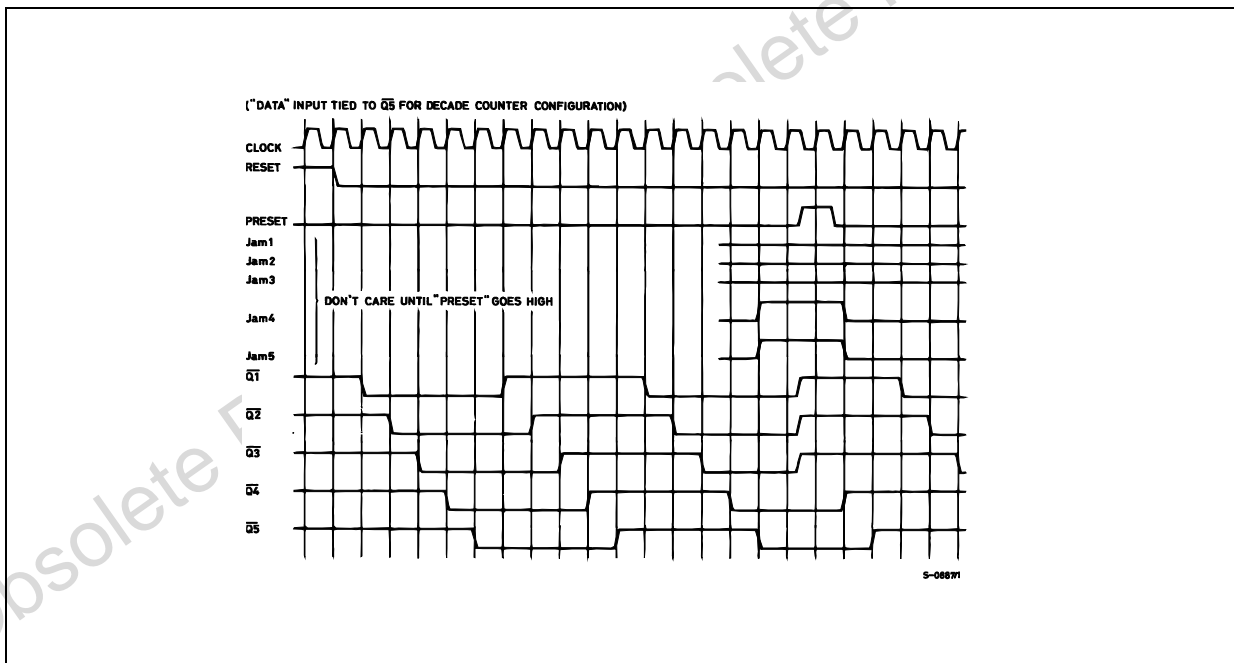
## FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TIMING CHART



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>ol</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	$\mu$ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

## HCF4018B

### DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ , $C_L = 50\text{pF}$ , $R_L = 200\text{K}\Omega$ , $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time	5			200	400	ns
		10			90	180	
		15			65	130	
$t_{THL}$ $t_{TLH}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$f_{CL}$	Maximum Clock Input Frequency	5		3	6		MHz
		10		7	14		
		15		8.5	17		
$t_W$	Minimum Clock Pulse Width	5		160	80		ns
		10		70	35		
		15		50	25		
$t_r$ , $t_f$	Clock Input Rise or Fall Time	5		unlimited			$\mu\text{s}$
		10					
		15					
$t_{setup}$	Data Setup Time Minimum Clock Inhibit	5		40	20		ns
		10		12	6		
		15		6	3		
$t_H$	Data Input Hold-Time	5		140	70		ns
		10		80	40		
		15		60	30		
<b>PRESET<sup>(1)</sup> or RESET OPERATION</b>							
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time (reset or reset to Q)	5			275	550	ns
		10			125	250	
		15			90	180	
$t_W$	Preset or Reset Pulse Width	5		160	80		ns
		10		70	35		
		15		50	25		
$t_{REM}$	Preset or Reset Removal Time	5		80	40		ns
		10		30	15		
		15		20	10		

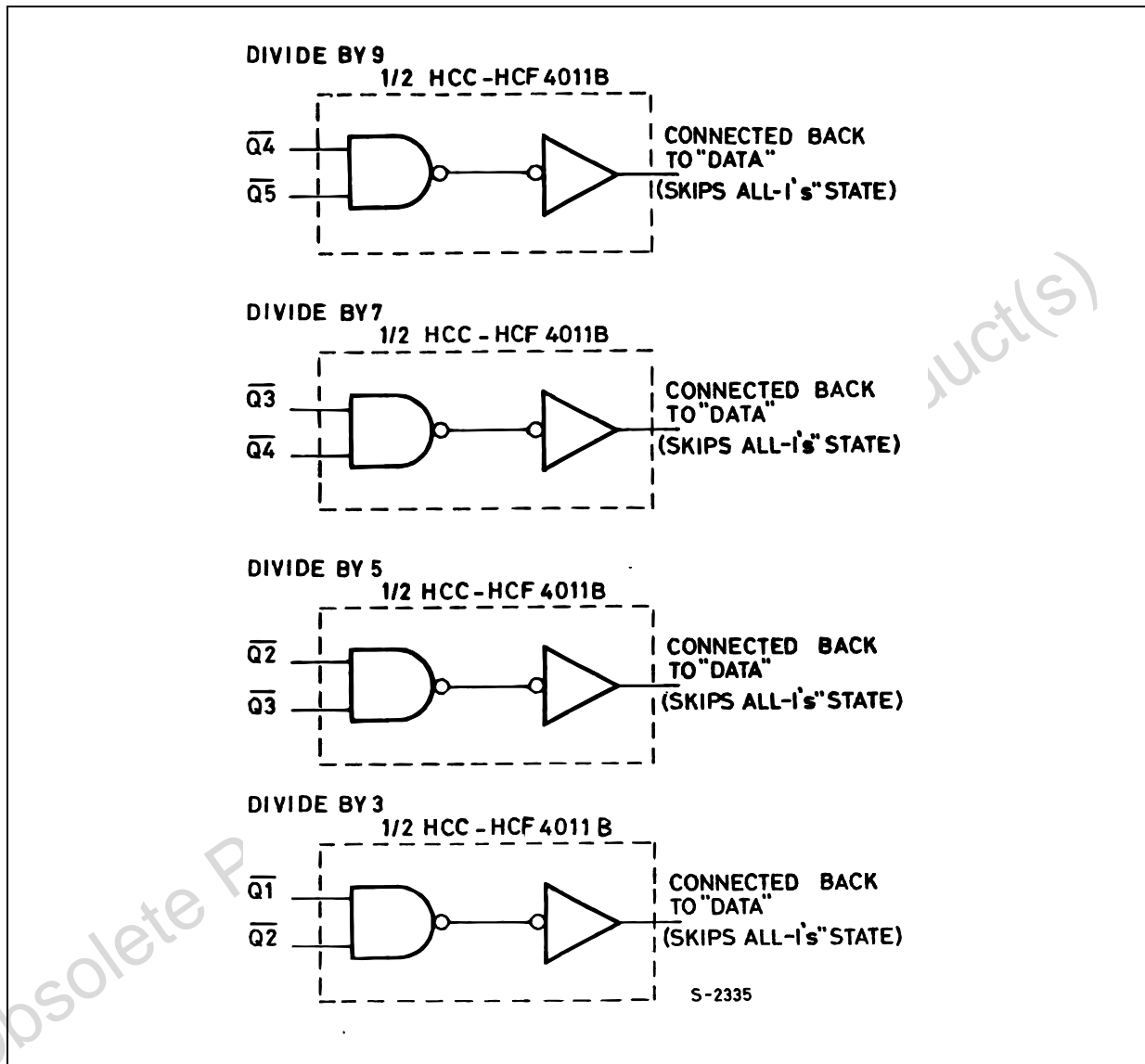
(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

(1) At PRESET ENABLE or JAM inputs

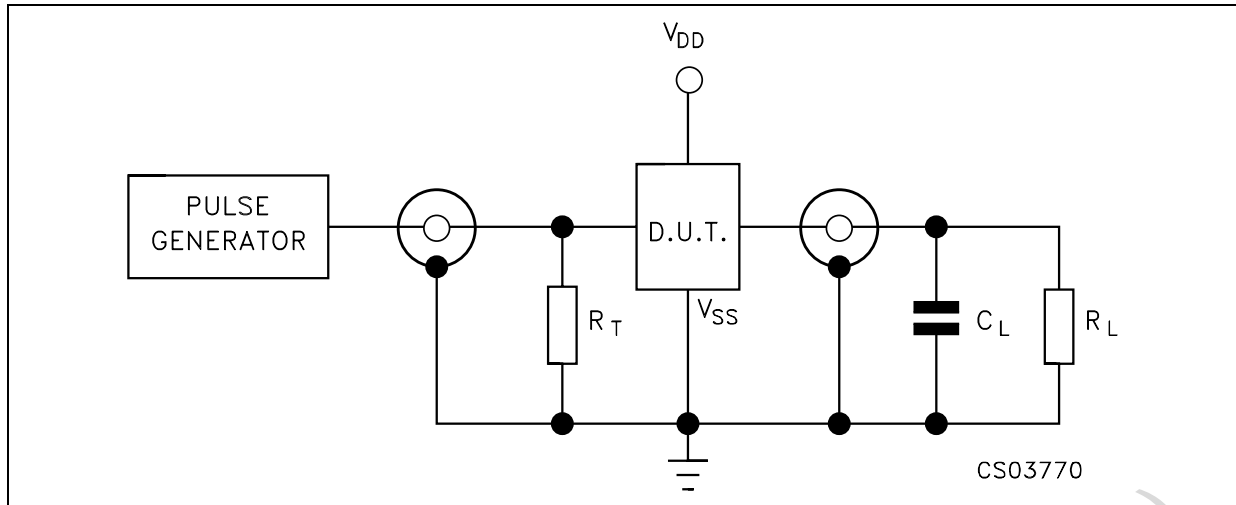
**TYPICAL APPLICATION**

External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation

DIVIDE BY 10 Q5	CONNECTED BACK TO "DATA"	NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 8 Q4		
DIVIDE BY 6 Q3		
DIVIDE BY 4 Q2		
DIVIDE BY 2 Q1	NO CONNECTED	



TEST CIRCUIT



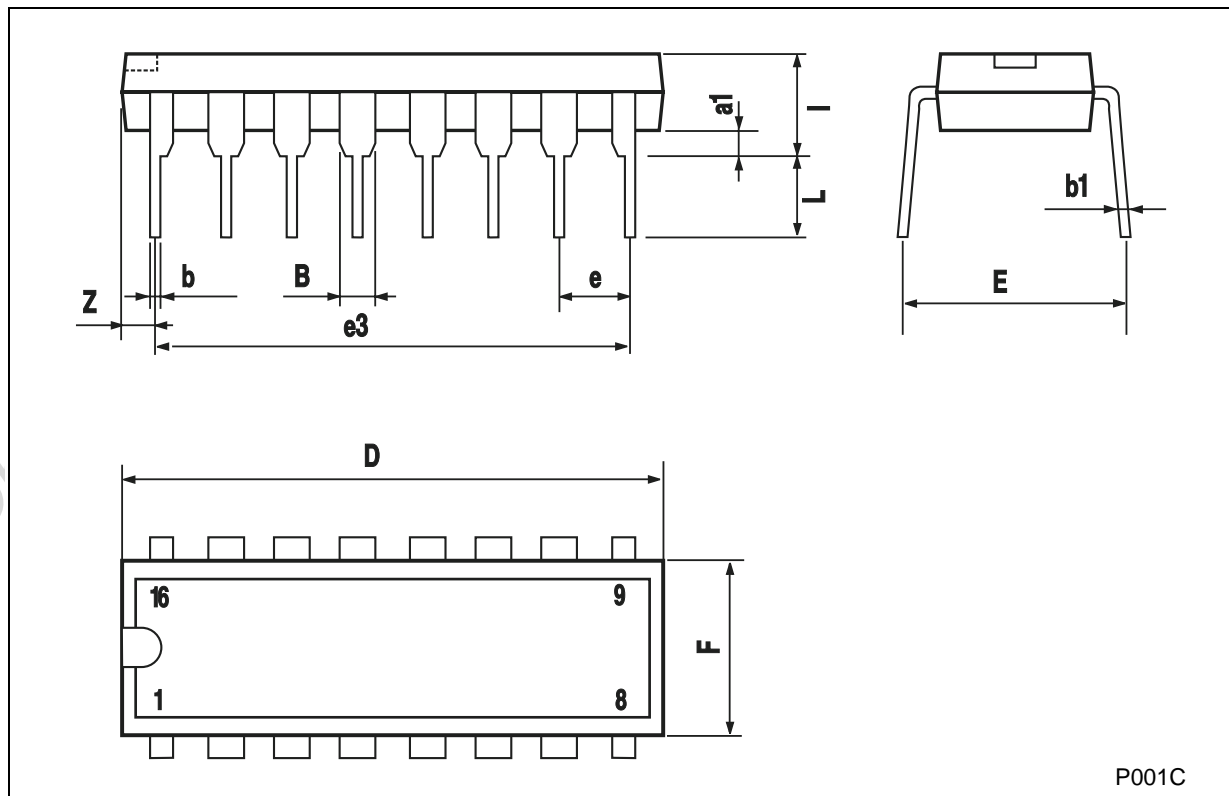
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{\text{OUT}}$  of pulse generator (typically  $50\Omega$ )

Obsolete Product(s) - Obsolete Product(s)



### Plastic DIP-16 (0.25) MECHANICAL DATA

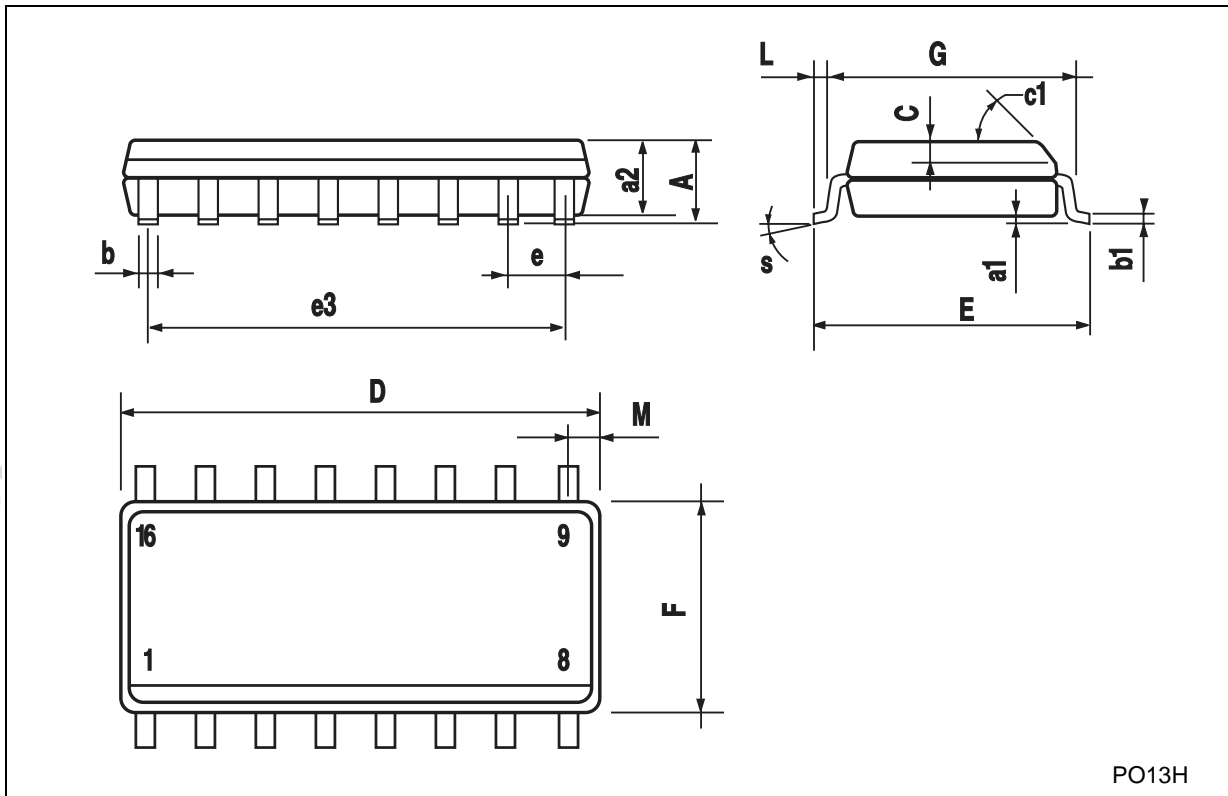
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Obsolete Product(s) - Obsolete Product(s)

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