REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21												
REV STATUS				REV															
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Muhammad Akbar

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
18-08-28

REVISION LEVEL

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, 8-CHANNEL 12-BIT ANALOG TO DIGITAL CONVERTER (50Ksps to 1Msps), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-18204**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

5962-E285-18

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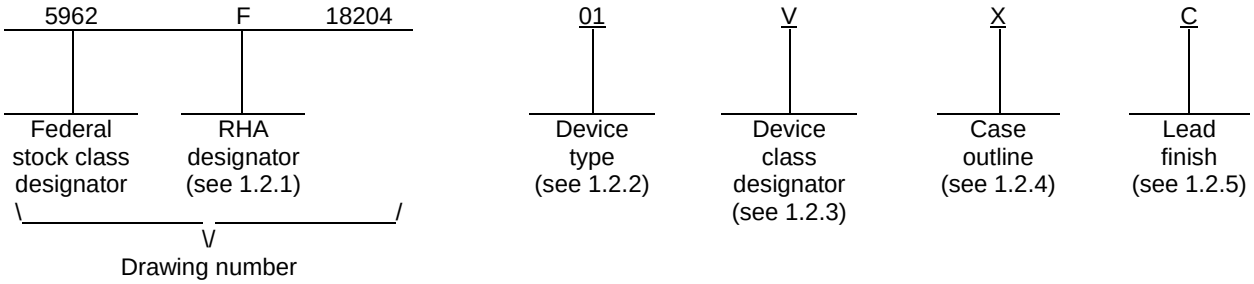
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHFAD128	8-Channel, 12 Bit A/D Converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16	Flat pack 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package case outline X with grounded lid.

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1.3 Absolute maximum ratings. 1/ 2/ 3/

Maximum analog power supply voltage between AVCC and AGND ..... -0.3 V to 4.8 V
Maximum digital power supply voltage between DVCC and DGND ..... -0.3 V to AVCC + 0.3V (4.8 V max)
Maximum voltage on any pin vs GND (V_I) ..... -0.3 V to AVCC + 0.3V (4.8 V max)
Maximum input current at any pin (I_I) ..... ± 10 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 22°C/W
Junction temperature (T_J) .....+150°C
Thermal resistance, junction-to-ambient(θ_{JA}) ..... 120°C/W
ESD at Human body model (HBM) ..... 4000 V

1.4 Recommended operating conditions. 2/ 3/

Analog Supply voltage range (AVCC) ..... 2.7 V to 3.6 V
Digital Supply voltage range (DVCC) ..... AV_{CC} - 0.15 V dc to AV_{CC} + 0.15 V dc
Input voltage any pin (V_{IN}):
Analog input voltage in single ended ..... +0.0 V to AVCC
Analog input voltage in differential configuration, and VICM= AVCC/2 ..... - AVCC to AVCC
Common mode in differential configuration (VICM) ..... 0 to AVCC
Digital input voltage (VIND) ..... 0 to AVCC
Ambient operating temperature range (T_A) ..... -55°C to +125°C
Clock frequency (SCLK) ..... 0.1 MHz to 16 MHz

1.5 Radiation features. 4/

Maximum total dose available: (effective dose rate = 0.35 Rad (Si)/s) ..... 300 krad(Si) 5/

Single event phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.3) ..... ≤ 125 MeV/(mg/cm^2) 6/
No SEU observed at LET (see 4.4.4.3) ..... ≤ 32.4 MeV/(mg/cm^2) 6/
No SEFI observed at LET (see 4.4.4.3) ..... ≤ 62.5 MeV/(mg/cm^2) 6

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ The limits for the parameters specified herein shall apply over the full specified AVCC range and case temperature range of -55°C to +125°C unless otherwise specified.
3/ Per MIL-STD-883 method 1012.1 section 3.4.1, P_D (Package) = (T_J(max) - T_C (max))/θJC
4/ Radiation testing is performed on the standard evaluation circuit.
5/ Device type 01 is irradiated at high dose rate = 50 - 300 Rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A. The effective dose rate after extended room temperature anneal is 0.35 Rad(Si)/s for device type 01, per MIL-STD-883, method 1019, condition A, paragraph 3.11.2. The total ionizing dose for this device only applies to the specified effective dose rate, or lower, environment.
6/ Manufacturer also performed heavy ion single event effects (SEE) test at U.C.L. Heavy Ion Test Facility (Université Catholique de Louvain - Belgium) with Xenon (Xe) ion beam and observed no SEL occurs at effective LET ≤ 125 MeV/(mg/cm^2). No SEU observed with sample frequency set to 50ksps until a LET of 32.4 MeV.cm^2/mg with a saturation cross-section of 4x10^{-6} cm^2. No SEFI observed with a LET of 62.5 MeV.cm^2/mg. For more information on SEE test, contact manufacturer.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959 https://www.astm.org).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy-Ion Irradiation.

JEP163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Copies of these documents are available online at https:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block or logic diagram. The block or logic diagram(s) shall be as specified on figures 2. .

3.2.4 Timing Waveforms. The timing waveforms shall be as specified on figures 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le Ta \le +125°C$ AVCC=DVCC= 3.30 AGND=DGND= 0 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Electrical characteristics in single ended input							
Digital input Characteristics							
Input high voltage	V_{IH}		All	1, 2, 3	2.1		V
Input low voltage	V_{IL}		All	1, 2, 3		0.8	V
Digital input current	I_{IN}	VIN = 0 V or DVCC	All	1, 2, 3	-1	+1	µA
Digital output characteristics							
Output high voltage 5/	V_{OH}	Isource= 1mA	All	1, 2, 3	2.8		V
Output low voltage 5/	V_{OL}	Isink= 1mA	All	1, 2, 3		0.4	V
High impedance output leakage current	I_{OZH}		All	1, 2, 3	-1	+1	µA
Low impedance output leakage current	I_{OZL}		All	1, 2, 3	-1	+1	µA
Power Supply Characteristics							
Total supply current (normal mode, CS low)	I_{AVCC} + I_{DVCC}	AVCC=DVCC= +2.7 to 3.6V, fS=1MSPS, FIN=40 kHz, CL = 10 pF	All	1, 2, 3		2.0	mA
Total supply current (shutdown mode, CS high)	I_{AVCC} + I_{DVCC}	AVCC=DVCC= +2.7 to 3.6V, fS=0, CL = 10 pF	All	1, 2, 3		10.0	µA
Analog input static Characteristics							
DC leakage current	I_{DCL}		All	1, 2, 3	-1	+1	µA
Static Characteristics							
Integral non-linearity (end point method)	INL		All	4, 5, 6	-1.10	+1.10	LSB
Differential non-linearity	DNL		All	4, 5, 6	-0.90	+0.90	LSB
Offset error	OE		All	4, 5, 6	-2.3	+2.3	LSB
Offset error match	OEM		All	4, 5, 6	-2.0	+2.0	LSB
Full scale error	FSE		All	4, 5, 6	-2.0	+2.0	LSB
Full scale error match	FSEM		All	4, 5, 6	-2.0	+2.0	LSB

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2 -55°C ≤ Ta ≤ +125°C AVCC=DVCC= 3.30 AGND=DGND= 0 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Dynamic Characteristics							
Signal to noise plus distortion ratio (0 to Fs/2)	SINAD	FIN= 40.2 KHz, -0.02 dBFS	All	4, 5, 6	68		dB
Signal to noise ratio (0 to Fs/2)	SNR		All	4, 5, 6	69		dB
Total harmonic distortion	THD		All	4, 5, 6		-74	dB
Spurious free dynamic range (0 to Fs/2)	SFDR		All	4, 5, 6	75		dB
Effective numbers of Bits	Enob		All	4, 5, 6	11.1		Bits
Channel to channel isolation	ISO	FIN= 20 KHz, -0.02 dBFS	All	4, 5, 6	80		dB
2nd order intermodulation	IM2	fa= 19.5 MHz, fb=20.5 MHz, VINA=VINB= -6.02 dBFS	All	4, 5, 6		-78	dB
3rd order intermodulation	IM3	fa= 19.5 MHz, fb=20.5 MHz, VINA=VINB= -6.02 dBFS	All	4, 5, 6		-72	dB
AC characteristics							
SCLK duty cycle	DC		All	9, 10, 11	40	60	%
Timing Characteristics 5/							
CS/hold time after SCLK rising edge 4/	t_{CSH}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11	10		ns
CS/setup time prior SCLK rising edge 4/	t_{CSS}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11	10		ns
CS/falling edge to DOUT enable	t_{EN}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11		30	ns
DOUT access time after SCLK falling edge	t_{DACC}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11		27	ns
DOUT hold time after SCLK falling edge	t_{DHLD}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11	7		ns
DIN hold/setup time prior/after SCLK rising edge	t_{DH}, t_{DS}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11	10		ns
CS/rising edge to DOUT rising/falling	t_{DIS}	AVCC = DVCC = +2.7V to +3.6V	All	9, 10, 11		20	ns

See footnote next page

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2 -55°C ≤ Ta ≤ +125°C AVCC=DVCC= 3.30 AGND=DGND= 0 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Electrical characteristics in Differential input							
Static Characteristics							
Integral non-linearity (end point method)	INL	VICM = AVCC / 2	All	4, 5, 6	-0.90	+0.90	LSB
Differential non-linearity	DNL		All	4, 5, 6	-0.80	+0.80	LSB
Offset error	OE		All	4, 5, 6	-1.5	+1.5	LSB
Offset error match	OEM		All	4, 5, 6	-1.5	+1.5	LSB
Full scale error	FSE		All	4, 5, 6	-2.0	+2.0	LSB
Full scale error match	FSEM		All	4, 5, 6	-2.0	+2.0	LSB
Dynamic Characteristics							
Signal to noise plus distortion ratio (0 to Fs/2)	SINAD	FIN= 40.2 KHz, -0.02 dBFS	All	4, 5, 6	69.3		dB
Signal to noise ratio (0 to Fs/2)	SNR		All	4, 5, 6	71		dB
Total harmonic distortion	THD		All	4, 5, 6		-74	dB
Spurious free dynamic range (0 to Fs/2)	SFDR		All	4, 5, 6	75		dB
Effective numbers of Bits	Enob		All	4, 5, 6	11.2		Bits
Channel to channel isolation	ISO	FIN= 20 KHz, -0.02 dBFS	All	4, 5, 6	85		dB
2nd order intermodulation	IM2	fa= 19.5 MHz, fb=20.5 MHz, VINA=VINB= -6.02 dBFS	All	4, 5, 6		-78	dB
3rd order intermodulation	IM3	fa= 19.5 MHz, fb=20.5 MHz, VINA=VINB= -6.02 dBFS	All	4, 5, 6		-72	dB

1/ Device type 01 is irradiated at dose rate = 50 - 300 Rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A. RHA device type 01 supplied to this drawing has been characterized through all levels L, R and F, irradiation, but is only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.

2/ AVCC=DVCC=3.3V, single ended input, AGND=DGND=0 V, fSCLK=0.8 MHz to 16MHz , fSAMPLE = 50ksps to 1Mpsps, CL = 50 pF, typical value at +25°C.25C, minimum/maximum values -55°C/+125°C unless otherwise specified.

3/ AVCC=DVCC=3.3V, differential input (see figure 4 for configuration), AGND=DGND=0 V, fSCLK=16 MHz , fSAMPLE = 1Mpsps, CL = 50 pF, typical value at +25°C.25C, minimum/maximum values -55°C/+125°C unless otherwise specified.

4/ Clock may be in any state (high or low) when CS/ goes high. Setup and hold time restrictions apply only to CS/ going low.

5/ Limits are guaranteed by functional test.

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TABLE IB. SEP test limits. 1/ 2/ 3/

Device Type	V_{DD} = 3.6 V 4/		Bias V_{DD} = 3.6 V for Single event latch-up (SEL) test no SEL occurs at effective LET 5/	No SEFI observed at LET MeV/(mg/cm^2)
	No upsets at LET MeV/(mg/cm2)	Maximum device cross section		
All	LET ≤ 32.4	4 x 10^{-6} cm^2/bit 6/	LET ≤ 125 MeV/(mg/cm^2)	LET ≤ 62.5

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Manufacturer also performed heavy ion single event effects (SEE) test at U.C.L. Heavy Ion Test Facility (Université Catholique de Louvain - Belgium) with Xenon (Xe) ion beam and observed no SEL occurs at effective LET ≤ 125 MeV/(mg/cm^2). No SEU observed with sample frequency set to 50ksps until a LET of 32.4 MeV.cm^2/mg with a saturation cross-section of 4x10^{-6} cm^2. No SEFI observed with a LET of 62.5 MeV.cm^2/mg. For more information on SEE test, contact manufacturer.
4/ Tested for upsets at worst case temperature, T_A = +25°C ± 10°C.
5/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up and SEFI.

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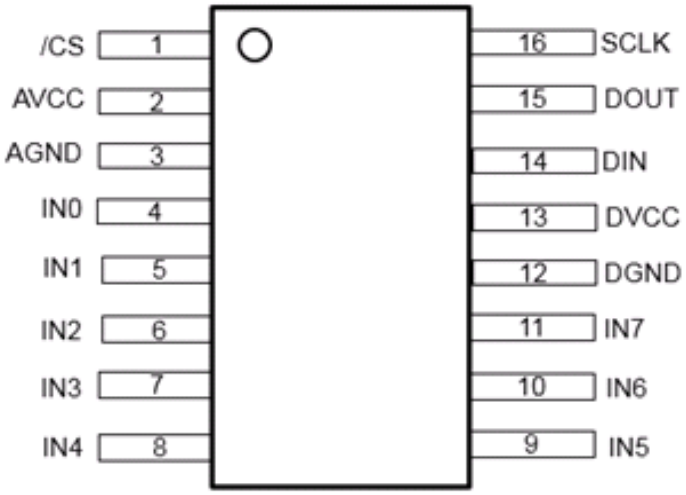

Figure 1: Pin description

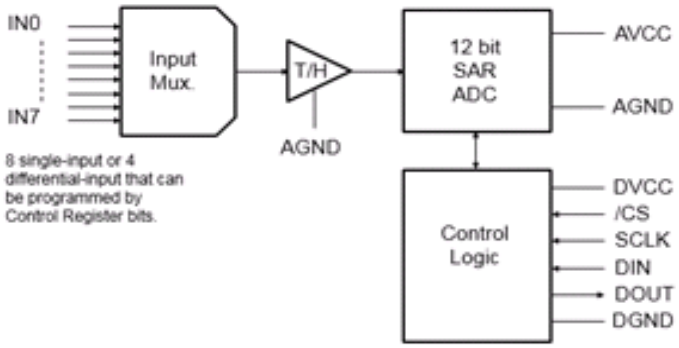

Figure 2: Block diagram

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Bit #	7 (MSB)	6	5	4	3	2	1	0
Symbol for single input	Any code except 11		ADD2	ADD1	ADD0	Any code except 001		
Symbol for differential input	1	1	0	ADD1	ADD0	0	0	1

TABLE: Control register bits

ADD2	ADD1	ADD0	Input channel
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

TABLE: Single input channel description.

ADD1	ADD0	Input channel
0	0	IN0-IN1
0	1	IN2-IN3
1	0	IN4-IN5
1	1	IN6-IN7

TABLE: Differential input channel description.

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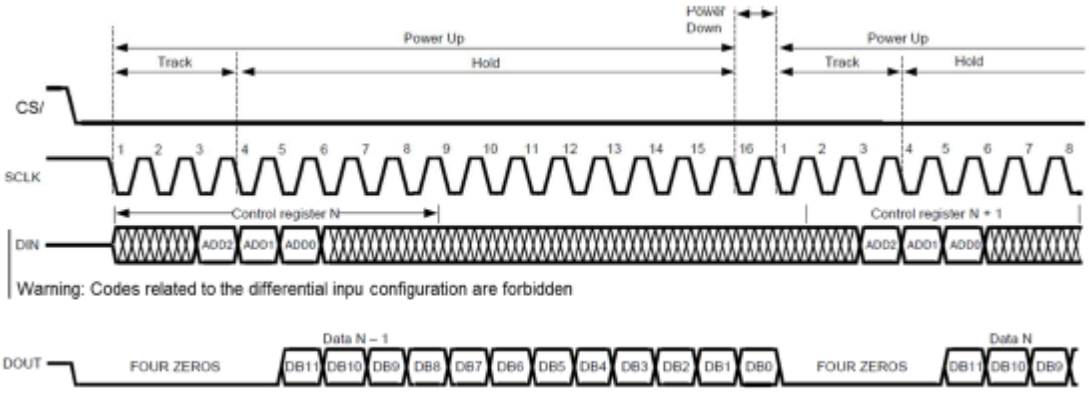

FIGURE 3: Operational timing diagram in single ended input.

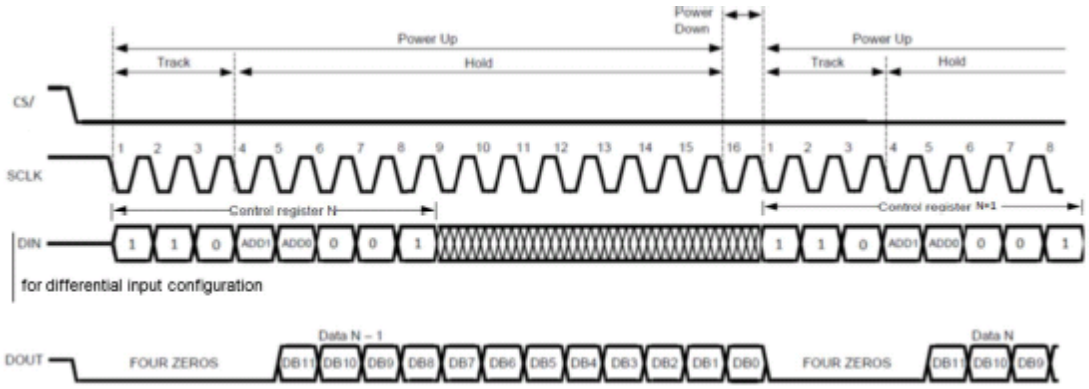

FIGURE 4: Operational timing diagram in differential input.-continued.

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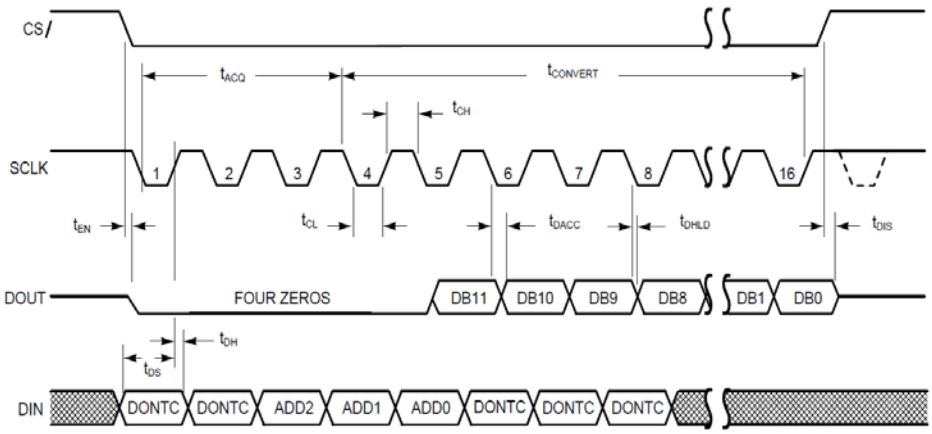


FIGURE 5: Serial timing diagram -continued.

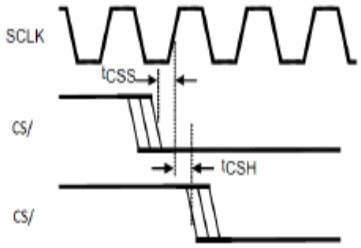
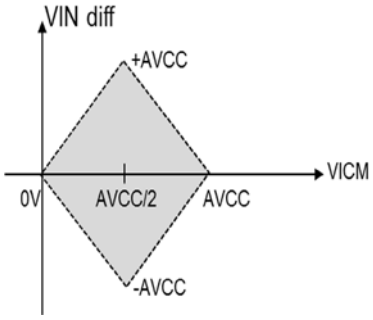


FIGURE 6: SCLK and CS/ timing diagram -continued.



Note: The maximum differential input swing is limited by the input common mode value (VICM) and it is limited by the grey area as shown in figure 7. The maximum value equals to +/-AVCC for VICM=AVCC/2.

FIGURE 7:True deferential input range -continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535 and JEDEC JEP163. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Unless otherwise specified in the QM plan, for devices class Q and V dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

e. For devices class V , interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} , C_{OUT} , C_{ON} , C_{OFF1} , and C_{OFF2} shall be measured in accordance with MIL-STD-883, M3012 and only for the initial test and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all pins on one device and then test four additional devices on worst case pin for each I/O type.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A(high dose rate = 50 - 300 Rad (Si)/s). The effective dose rate after extended room temperature anneal is 0.35 rad(Si)/s for device type 01, per MIL-STD-883, method 1019, condition A, paragraph 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. When specified in the purchase order or contract, Neutron irradiation test shall be conducted by using a neutron fluence of approximately 2 x 10^{12} neutrons/cm^2.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature 25°C ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

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TABLE IIA. Electrical test requirements. 2/ 3/ 4/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, TABLE III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4, 9	1, 4, 9
Dynamic burn-in (method 1015)	Required	Required
Post burn-in interim electrical parameters	1, 4, 9 1/	1, 4, 9 1/ 5/
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11 5/
Group D end-point electrical parameters (see 4.4.3)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group E end-point electrical parameters (see 4.4.4)	1, 4, 9	1, 4, 9

1/ PDA applies to subgroup 1 (see 4.2). For device class V, PDA applies to subgroups 1 and 7 (see 4.2).
2/ The burn-in shall meet the requirements of 4.2.1a herein.
3/ On all class V lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
4/ If the device operates in a dynamic mode, then dynamic burn-in test shall be performed per TM 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).
5/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.

TABLE IIB. Burn-in and operating life test delta parameters (+25°C).

Parameter 1/	Device electrical parameters	Delta limit
Total supply current (Normal mode, Cs low)	IAVCC+IDVAC	± 150 µA
Total supply current (shutdown mode, Cs high)	IAVCC+IDVAC	± 300 nA
Digital input current	I_{IN}	± 100 nA
High and Low impedance output leakage current	I_{OZH}, I_{OZL}	± 250 nA
Dc leakage current	I_{DCL}	± 250 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 General applications: The manufacturer is supplying this SMD device as a high-performance CMOS technology analog to digital converter (ADC) capable of converting analog input signals into 12-bit digital words at rate 50 KSPS to 1 Mega Samples Per Second (MSPS). This device can be used in many applications/systems but general applications are telemetry communication instruments, radar systems, test and measurement equipment, multi carrier/multi-mode receivers in space and harsh environments.

6.1.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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APPENDIX A

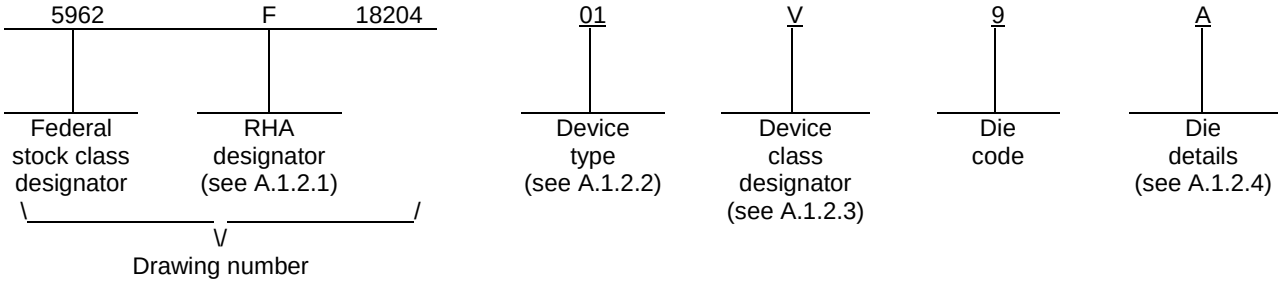
APPENDIX A FORMS A PART OF SMD 5962-18204

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:

For device class V:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHFAD128	8-Channel, 12 Bit A/D Converter

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

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A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, P.O. Box 3990, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA, and have agreed to this drawing.

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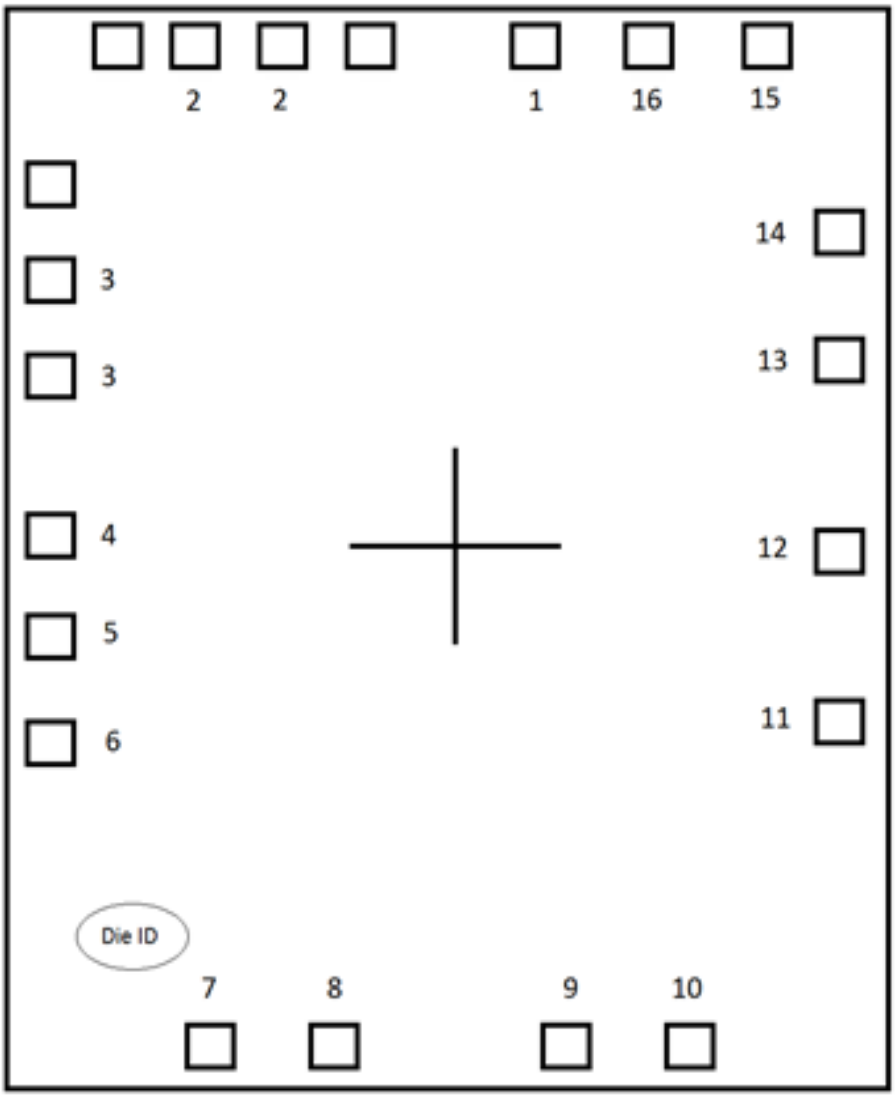

Bond Pad size: All pads are 100 x 100 μm

NOTE:

1. Pad numbers reflect terminal numbers when placed in case outline X (see 1.2.4).
2. All VCC's pads have to be connected to the same voltage level.
3. All GND's pads have to be connected to the same voltage level.

FIGURE A-1.. Die bonding pad locations and electrical functions

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Die physical dimensions.

Die size:	2120 x 2520 μm
Die thickness:	280 ±10 μm

Interface materials.

Top metallization:	AlCu (thickness = 1.2 μm)
Backside metallization:	Raw silicon and back grinding.

Glassivation.

Type:	PSG + Nitride
Thickness:	PSG 5000 Å + Silicon nitride(SiN) 6000Å
Substrate:	Silicon

Assembly related information.

Substrate potential:	V_{SS}
Special assembly instructions:	None

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-08-28

Approved sources of supply for SMD 5962-18204 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1820401VXC	F8859	RHFAD128K01V
5962F1820401VXA	F8859	RHFAD128K02V
5962F1820401V9A	F8859	RHFAD128D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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