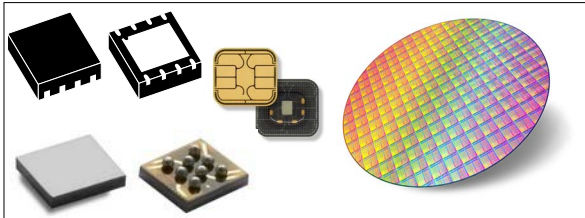


Secure MCU with 32-bit ARM® SecurCore® SC300™ CPU, SWP, ISO, SPI and GPIO interfaces and high-density Flash memory

Data brief



Features

Hardware features

- ARM® SecurCore® SC300™ 32-bit RISC core cadenced at up to 33 MHz (ST33Ixxx devices)
- 30 Kbytes of user RAM
- Up to 1280 Kbytes of user Flash memory with OTP area
- Asynchronous receiver transmitter supporting ISO/IEC 7816-3 T=0 and T=1 protocols (Slave mode supported)
- Single wire protocol (SWP) interface for communications with NFC router (ETSI 102-613 compliant)
- Serial peripheral interface (SPI) master/slave interface
- Three 16-bit timers with interrupt capability including one 16-bit timer with watchdog capability
- Seven general-purpose I/Os enabling proprietary protocol implementation
- 1.8 V, 3 V and 5 V supply voltage ranges
- External clock frequency from 1 up to 10 MHz
- Current consumption compatible with:
 - GSM specifications
 - ETSI specifications (ST33Gxxx devices)
- Power-saving standby state
- Contact assignment compatible with ISO/IEC 7816-2
- ESD protection greater than 4 kV (HBM)

Software features

- Secure Flash memory loader
- Flash memory drivers

Security features

- Active shield
- Memory protection unit (MPU)
- Monitoring of environmental parameters
- Protection against faults
- 16- and 32-bit CRC calculation block (ISO 13239, IEEE 802.3, etc.)
- True random number generator
- Unique serial number on each die
- Hardware security-enhanced DES accelerator
- Hardware security-enhanced AES accelerator
- NESCRYPT coprocessor for public key cryptography algorithm

Applications

Major ST33Gxxx/ST33Ixxx applications include:

- Mobile communications (GSM, 3G and CDMA)
- Secure element
- NFC mobile transactions
- Java Card™ applications
- Multimedia

Table 1. Device summary

Part number	Memory size in Kbytes
ST33G1M2, ST33I1M2	1280
ST33G1M0, ST33I1M0	1024
ST33G896, ST33I896	896
ST33G768, ST33I768	768
ST33G640, ST33I640	640
ST33G512, ST33I512	512

1 Description

The ST33Gxxx and ST33lxxx are serial access microcontrollers designed for secure mobile applications. They incorporate the most recent generation of ARM[®] processors for embedded secure systems. Their SecurCore[®] SC300[™] 32-bit RISC core is built on the Cortex[®] M3 core with additional security features to help to protect against advanced forms of attacks.

Cadenced at 25 MHz (ST33Gxxx) or 33 MHz (ST33lxxx), the SC300[™] core brings great performance and excellent code density thanks to the Thumb[®]-2 instruction set.

The high-speed embedded Flash memory introduces more flexibility to the system.

The ST33Gxxx and ST33lxxx also offer a serial communication interface fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1) and a single-wire protocol (SWP) interface for communication with a near field communication (NFC) router in SIM/NFC applications.

An SPI Master/Slave interface is also available for communication in non-SIM applications.

Three general purpose 16-bit timers are available; one is configurable as a watchdog.

The ST33Gxxx and ST33lxxx feature hardware accelerators for advanced cryptographic functions. The EDES peripheral provides a secure DES (Data Encryption Standard) algorithm implementation, while the NESCRYPT cryptoprocessor efficiently supports the public key algorithm. The AES peripheral ensures secure and fast AES algorithm implementation.

The device operates in the –25 to +85 °C temperature range and 1.8 V, 3 V and 5 V supply voltage ranges. A comprehensive range of power-saving modes enables the design of efficient low-power applications.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



2 Software development tool description

Dedicated SecurCore® SC300™ software development tools are provided by ARM and Keil®. This includes the Instruction Set Simulator (ISS) and C compiler. The documentation is available on the ARM and Keil websites.

Moreover, STMicroelectronics provides:

- A time-accurate hardware emulator controlled by the Keil debugger and the STMicroelectronics development environment.
- A complete product simulator based on Keil's ISS simulator for the SecurCore® SC300™ CPU.
- A secured ROMed Flash memory loader with very high-speed software downloading capabilities.

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
01-Oct-2013	1	Initial release.
20-Jun-2014	2	Added derivative devices.
18-Feb-2016	3	Added ST33Ixxx products (see Table 1: Device summary). Indicated the ECOPACK® compliance of packages.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

