REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - LTG	05-02-23	Thomas M. Hess
B	Add device type 02. Add device Class V criteria. Add radiation hardened assurance features in section 1.5 and SEP limits in table IB. Update boilerplate paragraphs to the current requirements as specified in MIL-PRF-38535. - jak	10-02-17	Thomas M. Hess
C	Change case outline X (flat pack) dimension A and add dimensions E2 and E3 to figure 1. Update radiation features in section 1.5 and SEP table IB. - MAA	13-07-16	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C															
SHEET	15	16	17	18	19															

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
87-12-08

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL BUFFER/LINE DRIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87695**

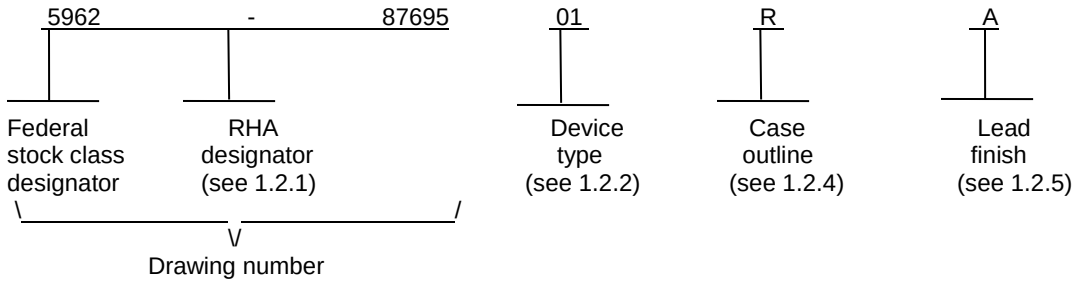
SHEET 1 OF 19

1. SCOPE

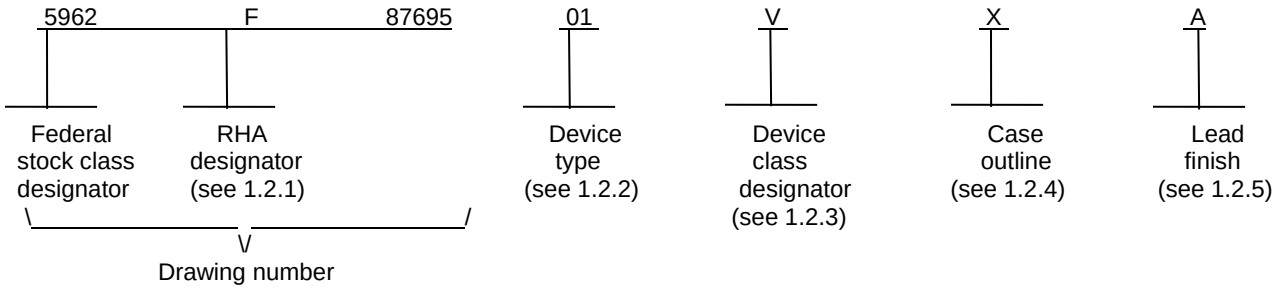
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC540	Octal buffer/line driver with three-state outputs
02	54AC540	Radiation hardened octal buffer/line driver with three-state outputs

1.2.3 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
X	See figure 1	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 4/

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC}) ..... +3.0 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times:
V_{CC} = 3.6 V ..... 0 to 116 ns (10% to 90%, 40 ns/V)
V_{CC} = 5.5 V ..... 0 to 88 ns (10% to 90%, 20 ns/V)

1.5 Radiation features.

Device type 02:
Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) ..... 300 krads (Si)
Single event phenomenon (SEP):
No SEU occurs at effective LET (see 4.4.4.2) ..... ≤ 110 MeV–cm^2/mg
No SEL occurs at effective LET (see 4.4.4.2) ..... ≤ 110 MeV–cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%\ V_{CC}$, $V_{IL} \leq 30\%\ V_{CC}$, $V_{OH} \geq 70\%\ V_{CC}$ @ -20 μA, $V_{OL} \leq 30\%\ V_{CC}$ @ 20 μA.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

EIA/JEDEC Standard JESD78 - IC Latch-up Test

JEDEC Standard JESD20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein, or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH} 2/	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu A$	$V_{CC} = 3.0$ V	1, 2, 3	All	2.90		V
			$V_{CC} = 4.5$ V			4.40		
			$V_{CC} = 5.5$ V			5.40		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA	$V_{CC} = 3.0$ V	1, 2, 3	01	2.40		
				1	02	2..56		
				2, 3		2.40		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -24$ mA	$V_{CC} = 4.5$ V	1, 2, 3	01	3.70		
				1	02	3.86		
				2, 3		3.70		
			$V_{CC} = 5.5$ V	1, 2, 3	01	4.70		
				1	02	4.86		
				2, 3		4.70		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ mA	$V_{CC} = 5.5$ V	1, 2, 3	All	3.85		
Low level output voltage	V_{OL} 2/	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	$V_{CC} = 3.0$ V	1, 2, 3	All		0.10	V
			$V_{CC} = 4.5$ V				0.10	
			$V_{CC} = 5.5$ V				0.10	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 12$ mA	$V_{CC} = 3.0$ V	1, 2, 3	01		0.50	
				1	02		0.36	
				2, 3			0.50	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 24$ mA	$V_{CC} = 4.5$ V	1, 2, 3	01		0.50	
				1	02		0.36	
				2, 3			0.50	
			$V_{CC} = 5.5$ V	1, 2, 3	01		0.50	
				1	02		0.36	
				2, 3			0.50	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ mA	$V_{CC} = 5.5$ V	1, 2, 3	All		1.65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level input voltage	V_{IH} 3/		V_{CC} = 3.0 V	1, 2, 3	All	2.1		V
			V_{CC} = 4.5 V			3.15		
			V_{CC} = 5.5 V			3.85		
Low level input voltage	V_{IL} 3/		V_{CC} = 3.0 V	1, 2, 3	All		0.9	V
			V_{CC} = 4.5 V				1.35	
			V_{CC} = 5.5 V				1.65	
Input leakage current low	I_{IL}	V_{IN} = 0.0 V V_{CC} = 5.5 V		1, 2, 3	01		-1.0	µA
				1	02		-0.1	
				2, 3			-1.0	
Input leakage current high	I_{IH}	V_{IN} = 5.5 V V_{CC} = 5.5 V		1, 2, 3	01		1.0	
				1	02		+0.1	
				2, 3			+1.0	
Quiescent supply current, output high	I_{CCH}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V		1, 2, 3	01		160	µA
				1	02		2	
				2, 3			40	
			M, D, P, L, R, F 4/	1			50	
Quiescent supply current, output low	I_{CCL}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V		1, 2, 3	01		160	
				1	02		2	
				2, 3			40	
			M, D, P, L, R, F 4/	1			50	
Quiescent supply current, output three-state	I_{CCZ}	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V		1, 2, 3	01		160	
				1	02		2	
				2, 3			40	
			M, D, P, L, R, F 4/	1			50	
Off-state output leakage current high	I_{OZH}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND V_{OUT} = 5.5 V		1, 2, 3	01		10.0	µA
				1	02		+0.5	
				2, 3			+5.0	
			M, D, P, L, R, F	1			+5.0	
Off-state output leakage current low	I_{OZL}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND V_{OUT} = 0.0 V		1, 2, 3	01		-10.0	
				1	02		-0.5	
				2, 3			-5.0	
			M, D, P, L, R, F	1			-5.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input capacitance	C_{IN}	See 4.3.1c		4	All		8.0	pF
Power dissipation capacitance	C_{PD} 5/	See 4.3.1c		4	All		65.0	pF
Functional tests		Tested at V_{CC} = 3.0 V and repeated at V_{CC} = 5.5 V See 4.3.1d		7, 8	All	L	H	
Propagation delay time, An to $\overline{Yn}$	t_{PHL} 6/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	01	1.0	7.0	ns
				10, 11	01	1.0	8.0	
				9	02	1.0	11.0	
				10, 11	02	1.0	13.5	
			V_{CC} = 4.5 V	9	01	1.0	5.5	
				10, 11	01	1.0	6.5	
				9	02	1.0	7.5	
				10, 11	02	1.0	8.5	
	t_{PLH} 6/		V_{CC} = 3.0 V	9	01	1.0	7.5	
				10, 11	01	1.0	9.0	
				9	02	1.0	8.5	
				10, 11	02	1.0	9.5	
			V_{CC} = 4.5 V	9	01	1.0	6.0	
				10, 11	01	1.0	7.0	
				9	02	1.0	7.0	
				10, 11	02	1.0	8.0	
Propagation delay time, output enable, $\overline{OE1}$ or $\overline{OE2}$ to $\overline{Yn}$	t_{PZH} 6/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	01	1.0	11.0	ns
				10, 11	01	1.0	13.0	
				9	02	1.0	11.0	
				10, 11	02	1.0	13.5	
			V_{CC} = 4.5 V	9	01	1.0	8.5	
				10, 11	01	1.0	10.0	
				9	02	1.0	9.0	
				10, 11	02	1.0	11.0	
	t_{PZL} 6/		V_{CC} = 3.0 V	9	01	1.0	10.0	
				10, 11	01	1.0	12.0	
				9	02	1.0	12.0	
				10, 11	02	1.0	14.5	
			V_{CC} = 4.5 V	9	01	1.0	7.5	
				10, 11	01	1.0	9.0	
				9	02	1.0	10.0	
				10, 11	02	1.0	12.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, output disable, $\overline{OE}1$ or $\overline{OE}2$ to $\overline{Yn}$	t_{PHZ} 6/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	01	1.0	13.0	ns
				10, 11	01	1.0	15.5	
				9	02	1.0	12.0	
				10, 11	02	1.0	13.0	
			V_{CC} = 4.5 V	9	01	1.0	10.5	
				10, 11	01	1.0	12.0	
				9	02	1.0	10.5	
				10, 11	02	1.0	11.5	
	t_{PLZ} 6/		V_{CC} = 3.0 V	9	01	1.0	10.0	
				10, 11	01	1.0	12.0	
				9	02	1.0	10.0	
				10, 11	02	1.0	12.0	
			V_{CC} = 4.5 V	9	01	1.0	8.0	
				10, 11	01	1.0	10.0	
				9	02	1.0	9.0	
				10, 11	02	1.0	10.0	

1/ RHA parts for device type 01 of this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V. All other voltages are guaranteed, but not tested. Limits shown apply to operation at V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

3/ V_{IH} and V_{IL} tests are guaranteed by the V_{OH} and V_{OL} tests.

4/ The maximum limit for this parameter at 100 kRAD is 4 µA.

5/ Power dissipation capacitance (C_{PD}) determines both the dynamic power consumption (P_D) and the dynamic current consumption (I_S).

Where:

$P_D = (C_{PD} + C_L) (V_{CC}^2)f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$.

f is the frequency of the input signal and C_L is the external load capacitance.

6/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to the limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

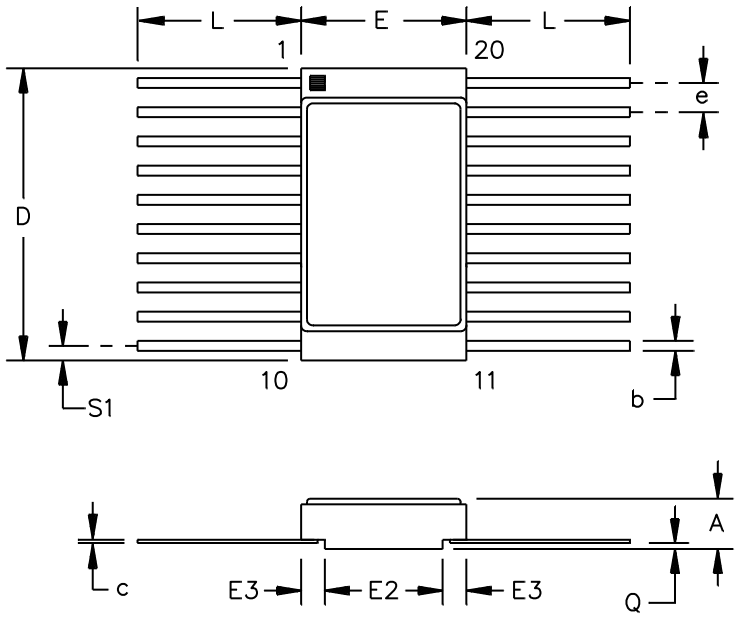
TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	T_A = temperature ±10°C	Bias V_{CC}	Effective LET
02	No SEL	+125°C	3.6 V and 5.5 V	≤ 110 MeV-cm^2/mg
	No SEU	+25°C	3.0 V	≤ 110 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

Case outline X



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note: Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches minimum instead of 0.026 inches minimum.

FIGURE 1. Case outlines X

Device type	All
Case outlines	R, S, X, and 2
Terminal number	Terminal symbol
1	$\overline{OE1}$
2	A0
3	A1
4	A2
5	A3
6	A4
7	A5
8	A6
9	A7
10	GND
11	$\overline{Y7}$
12	$\overline{Y6}$
13	$\overline{Y5}$
14	$\overline{Y4}$
15	$\overline{Y3}$
16	Y2
17	$\overline{Y1}$
18	Y0
19	$\overline{OE2}$
20	V_{CC}

FIGURE 2. Terminal connections.

Inputs			Output
$\overline{OE1}$	$\overline{OE2}$	An	$\overline{Yn}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 3. Truth table.

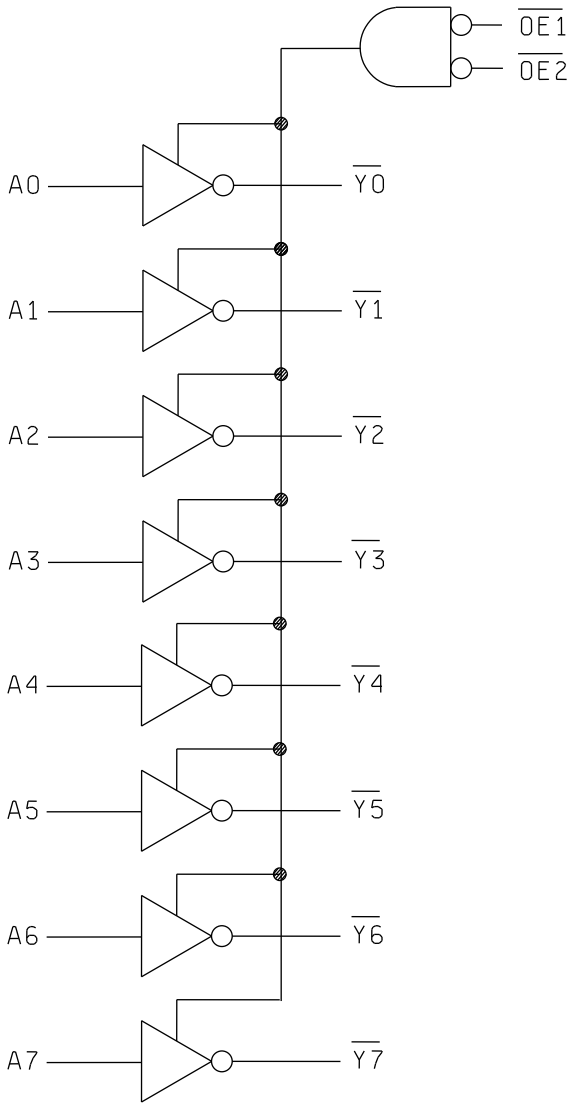


FIGURE 4. Logic diagram.

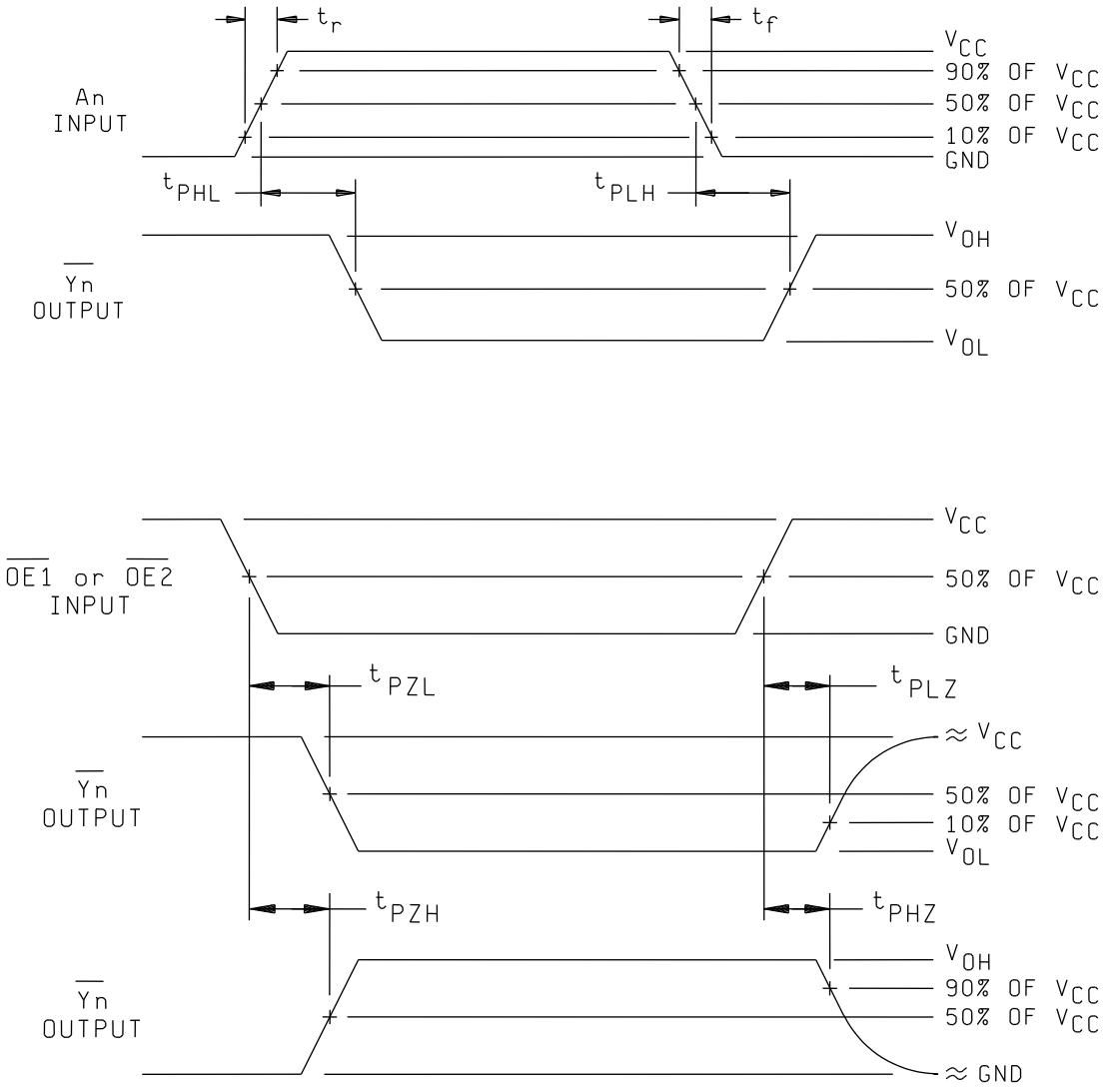
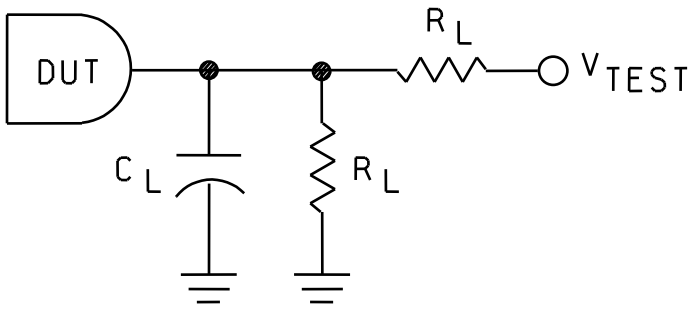


FIGURE 5. Switching waveforms and test circuit.



NOTES:
1. When measuring t_{PLH}, t_{PHL}, t_{PZH}, and t_{PHZ}: V_{TEST} = open. When measuring t_{PZL} and t_{PLZ}: $V_{TEST} = 2xV_{CC}$.
2. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
3. $R_L = 500\Omega$ or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum frequency of 1MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4)

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table I A herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I A at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualification package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

Device type 02:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on classes M, Q, and V devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9	1/ 1, 2, 3, 7, 8, 9	2/, 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C). 1/

Parameter 2/	Symbol	Delta limits
Supply current	I_{CCH}, I_{CCL}, I_{CCZ}	±300 nA
Input current low level	I_{IL}	±20 nA
Input current high level	I_{IH}	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	±0.20 V

1/ This table is representation of what vendor CAGE F8859 has experienced and is guaranteed and not meant to be construed as a quality assurance requirement for any other vendor.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor- prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

c. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-07-16

Approved sources of supply for SMD 5962-87695 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8769501RA	0C7V7	54AC540DMQB
5962-8769501SA	0C7V7	54AC540FMQB
5962-87695012A	0C7V7	54AC540LMQB
5962F8769502VXA	F8859	RHFAC540K02V
5962F8769502VXC	F8859	RHFAC540K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	e2v Aerospace and Defense, Inc. (dba QP Semiconductor, Inc) 765 Sycamore Drive Milpitas, CA 95035
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2 - FRANCE

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