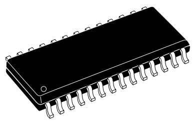
TDA7461

Car radio signal processor

Not For New Design

Features

- High performance signal processor for car radio systems
- Device includes audio processor, stereo decoder, noise blanker and multipath detector
- No external components required
- Fully programmable via I^2C bus
- Low distortion
- Low noise



SO-28

Description

The TDA7461 is a high performance signal processor specifically designed for car radio applications.

The device includes a complete audioprocessor and a stereo decoder with noise blanker, stereo blend and all signal processing functions necessary for state-of-the-art as well as future car radio systems.

Switched-capacitors design technique allows to obtain all these features without external components or adjustments. This means that higher quality and reliability walks alongside an overall cost saving. The CSP is fully programmable by I^2C bus interface allowing to customize key device parameters and especially filter characteristics.

The BiCMOS process combined with the optimized signal processing assure low noise and low distortion performances.

Table 1. Device summary

Order code	Package	Packing
TDA7461ND	SO-28	Tube
TDA7461NDTR	SO-28	Tape and reel
E-TDA7461ND(1)	SO-28	Tube
E-TDA7461NDTR(1)	SO-28	Tape and reel

1. Device in ECOPACK® package, see *Chapter 7: Package information on page 46*.

This is information on a product still in production but not recommended for new designs.

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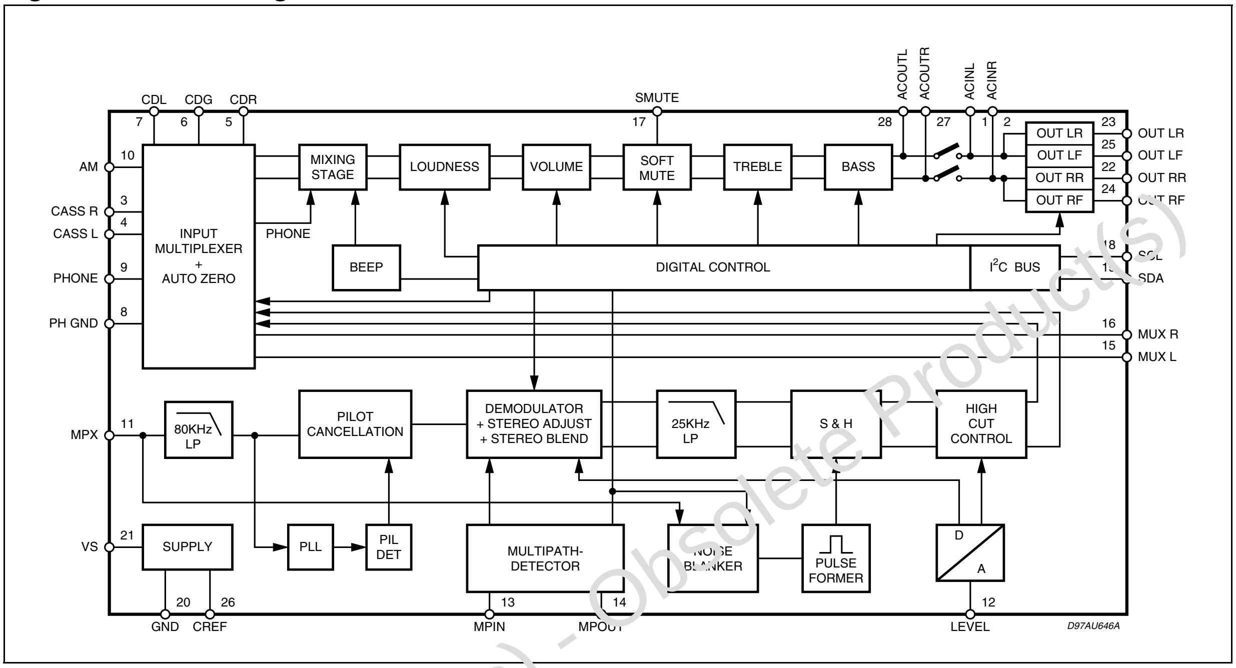
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

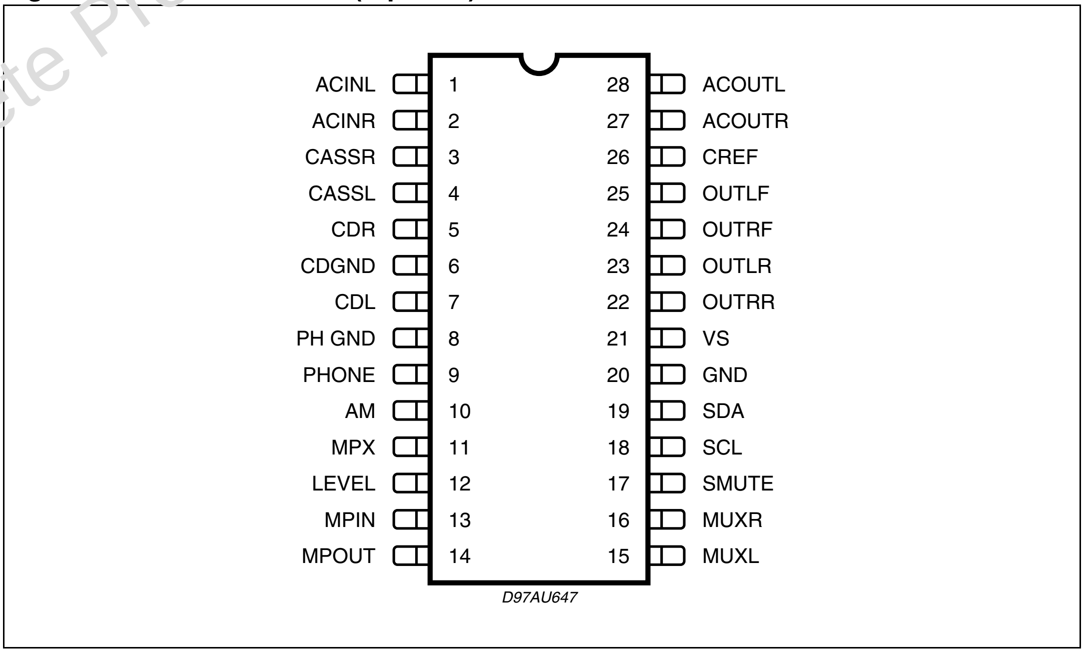


Table 2. Pin description

N.	Name	Function	Type
1	ACINL	Speaker stage input left	I
2	ACINR	Speaker stage input right	I
3	CASSR	Cassette input right	I
4	CASSL	Cassette input left	I
5	CDR	CD right channel input	I
6	CDGND	Ground reference CD	I
7	CDL	CD left channel input	I
8	PHGND	Phone ground	I
9	PHONE	Phone input	I
10	AM	AM input	I
11	MPX	FM input (MPX)	I
12	LEVEL	Level input stereo decoder	I
13	MPIN	Multipath detector input	I
14	MPOUT	Multipath detector output	O
15	MUXL	Multiplexer output left channel (stereo decoder output left selectable [1]	O
16	MUXR	Multiplexer output right channel (stereo decoder output right selectable [1])	O
17	SMUTE	Soft mute drive	I
18	SCL	I^2C clock line	I/O
19	SDA	I^2C data line	I/O
20	GND	Supply ground	S
21	VS	Supply voltage	S
22	OUTRR	Right rear speaker output	O
23	OUTLR	Left rear speaker output	O
24	OUTRF	Right front speaker output	O
25	OUTLF	Left front speaker output	O
26	CREF	Reference capacitor pin	S
27	ACOUTR	Pre-speaker AC output right channel	O
28	ACOUTL	Pre-speaker AC output left channel	O

1. See data byte specification - speaker attenuator

Pin type:

I = Input
O = Output
I/O = Input/Output
S = Supply

2 Electrical specification

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

2.2 Supply

Table 4. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		7.5	9	10	V
I_S	Supply current	V_S = 9V	25	30	35	mA
SVRR	Ripple rejection @ 1 kHz	Audioprocessor (all filters flat)		60		dB
		Stereo decoder + Audioprocessor		45		dB

2.3 ESD

All pins are protected against ESD according to the MIL883 standard.

2.4 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance junction to pins max	85	°C/W

2.5 Audio processor part feature

2.5.1 Input multiplexer

- Fully differential or quasi-differential CD and cassette stereo input
- AM mono or stereo input
- Phone differential or single ended input
- Internal beep with 2 frequencies (selectable)
- Mixable phone and beep signals
- Loudness
- Second order frequency response
- Programmable center frequency and quality factor
- 15 x 1 dB steps
- Selectable flat-mode (constant attenuation)

2.5.2 Volume control

- 1 dB attenuator
- Max. gain 20 dB
- Max. attenuation 79 dB
- Soft-step gain control

2.5.3 Bass control

- 2^{nd} order frequency response
- Center frequency programmable in 4 (5) steps
- DC gain programmable
- 7 x 2 dB steps

2.5.4 Treble control

- 2^{nd} order frequency response
- Center frequency programmable in 4 steps
- 7 x 2 dB steps

2.5.5 Speaker control

4 independent speaker controls (1 dB steps control range 50 dB)

2.5.6 Mute function

- Direct mute
- Digitally controlled softmute with 4 programmable time constants

2.6 Audio processor electrical characteristics

Table 6. Audio processor electrical characteristics
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	all inputs except phone	70	100	130	KΩ
V_{CL}	Clipping level		2.2	2.6		V_{RMS}
S_{IN}	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. input gain		13	14	15	dB
G_{STEP}	Step resolution		1	2	3	dB
V_{DC}	DC Steps	Adjacent gain step	-5	0	+5	mV
		G_{MIN} to G_{MAX}	-5	1	+5	mV
Differential CD stereo input						
R_{in}	Input resistance	Differential	70	100	130	KΩ
		Common mode	20	30	40	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1 V_{RMS} @ 1 kHz	45	70		dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	45	60		dB
e_N	Output noise @ speaker output	20 Hz to 20 kHz flat; all stages 0dB		9	15	µV
Differential phone input						
R_{in}	Input resistance	Differential	10	15	20	KΩ
		Common mode	20	30	40	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1 V_{RMS} @ 1 kHz	45	70		dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	45	60		dB
Beep control						
V_{RMS}	Beep level		250	350	500	mV
f_{BMIN}	Lower beep frequency		570	600	630	Hz
f_{BMAX}	Higher beep frequency		1.15	1.2	1.25	KHz
Mixing control						
M_{LEVEL}	Mixing level	Source	-1	0	1	dB
		Source	-5	-6	-7	dB
		Source	-10	-12	-14	dB
		Beep/Phone	-1	0	1	dB
Volume control						
G_{MAX}	Max gain		19	20	21	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB

Table 6. Audio processor electrical characteristics (continued)
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to 20 dB	-1.25	0	1.25	dB
		G = -60 to 20 dB	-4	0	3	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0 dB to GMIN	-7	0.5	+7	mV
LOudness control						
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MAX}	Max. attenuation		-16	-15	-14	dB
f_{CMIN}	Lower center frequency		180	200	220	Hz
f_{CMAX}	Higher center frequency		360	400	440	Hz
Soft mute						
A_{MUTE}	Mute attenuation		60	100		dB
T_D	Delay time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	20	40.4	60	ms
		T4	200	324	600	ms
V_{THlow}	Low threshold for SM pin(1)				1	V
V_{THhigh}	High threshold for SM pin		2.5			V
R_{PU}	Internal pull-up resistor		70	100	130	KΩ
V_{PU}	Pull-up voltage			4.7		V
Soft step						
T_{SW}	Switch time		5	10	15	ms
Bass control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
f_C	Center frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100(2)	110	Hz
Q_{BASS}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	

Table 6. Audio processor electrical characteristics (continued)
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on	4	4.4	6	dB
Treble control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
f_C	Center frequency	f_{C1}	8	10	12	KHz
		f_{C2}	10	12.5	15	KHz
		f_{C3}	12	15	18	KHz
		f_{C4}	14	17.5	21	KHz
Speaker attenuator						
C_{RANGE}	Control range		-53	-50	-47	dB
A_{STEP}	Step resolution		0.5	1	2	dB
A_{MUTE}	Output mute attenuation		80	90		dB
E_E	Attenuation set error		-2		2	dB
V_{DC}	DC steps			0.1	5	mV
Audio outputs						
V_{CLIP}	Clipping level		2.2	2.6		V_{RMS}
R_L	Output load resistance		2			KΩ
C_L	Output load capacitance				10	nF
R_{OUT}	Output Impedance			30	100	W
V_{DC}	DC voltage level		3.6	3.8	4.0	V
General						
e_{NO}	Output noise	BW = 20 Hz to 20 kHz output muted		3	15	µV
		all gain = 0 dB BW = 20 Hz to 20 kHz		6.5	15	µV
S/N	Signal to noise ratio	all gain = 0 dB flat; V_O = 2 V_{RMS}		106		dB
		bass treble at 12 dB; V_O = 2.6V_{RMS}		100		dB
d	Distortion	V_{IN}= 1 V_{RMS}; all stages 0 dB		0.002	0.1	%
		V_{IN}= 1 V_{RMS}; bass & treble = 12 dB		0.05	0.1	%
S_C	Channel separation left/right		80	100		dB
E_T	Total tracking error	A_V = 0 to -20 dB	-1	0	1	dB
		A_V= -20 to -60 dB	-2	0	2	dB

1. The SM pin is active low (Mute = 0)
2. See description of audioprocessor part - bass & treble filter characteristics programming

3 Description of the audio processor part

3.1 Programmable input matrix

The programmable input matrix of the TDA7461 offers several possibilities to adapt the audioprocessor to the desired application. In to the standard application we have:

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereo decoder input.

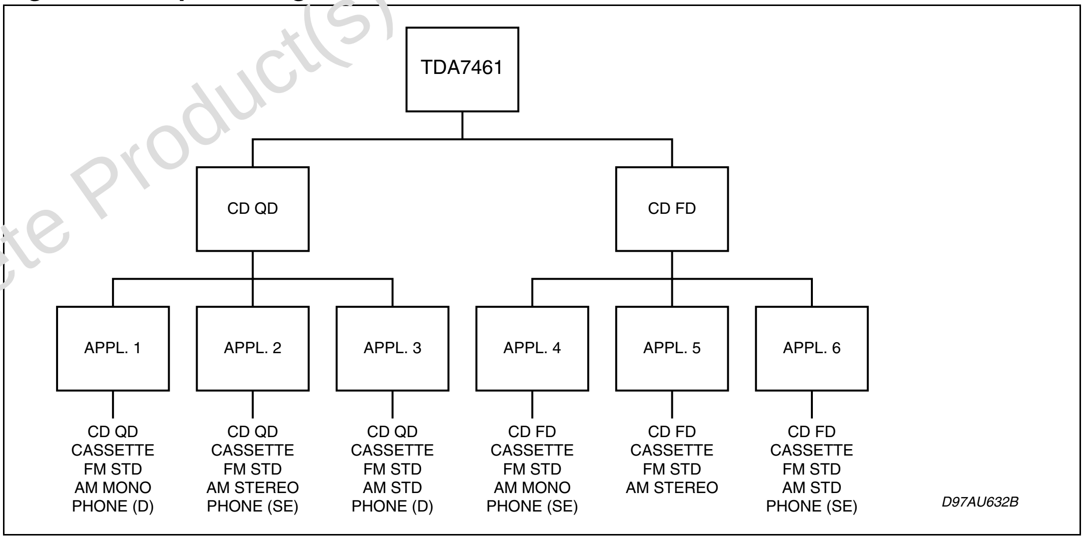
The input matrix can be configured by only 2 bits: bits 3 and 4 of subaddress 0. Basically the bit of subaddress 13 is fixed by the application and has to be programmed only once at the startup of the IC.

For many configurations the two bits are also fixed during one application (e.g. the standard application) and a change of the input source can be done by loading the first three bits of subaddress 0.

In other configurations for some sources a programming of bit 3 and 4 of subaddress 0 is necessary in addition to the three source selection bits. In every case only the subaddress 0 has to be changed to switch from one source to another.

The following picture shows the input and source programming flow:

Figure 3. Input configuration tree



1. In AMSTD configuration the AM mono signal is lead through the FM stereo decoder part to use its additional filters.

Table 7. Input and source programming

Appl. N#	Pin number				Programming [(1)]	
	6	8	9	10		
1	CD_{GND}	$Phone_{GND}$	Phone	AM_{MONO}	Startup	0/xxx11xxx
2	CD_{GND}	$Phone_{GND}$	AMRIGHT	AM_{LEFT}	Startup	0/xxxx1xxx
					FM	0/xxx11100
					AM	0/xxx01011
					Phone	0/xxx11010
3	CD_{GND}	$Phone_{GND}$	Phone	AMSTD	Startup	0/xxxx1xxx
					FM	0/xxx11100
					AM	0/xxx01100
					Phone	0/xxx11010
4	CDR_{GND}	CDL_{GND}	Phone	AM_{MONO}	Startup	0/xxxx0xxx
5	CDR_{GND}	CDL_{GND}	AMRIGHT	AM_{LEFT}	Startup	0/xxxx0xxx
					FM	0/xxx10100
					AM	0/xxx00011
6	CDR_{GND}	CDL_{GND}	Phone	AM_{STD}	Startup	0/xxxx0xxx
					FM	0/xxx10100
					AM	0/xxx00100
					Phone	0/xxx10010

1. Syntax 0/xxx11100 means: SUBADDRESS = 0 - DATA BYTE = xxx11100 (x - don't care).

3.1.1 How to find the right input configuration

The best way to come to the desired configuration may be to go through the application tree from the top to the bottom while making the specific decisions.

This way will lead to one of the six possible applications. Then take the number of the application and go into the pinning table. Here you will find the special pinout as well as the special programming codes for selecting sources.

For example in Appl. 6 the TDA7461 has to be configured while startup with the data byte 0/xxxx0xxx.

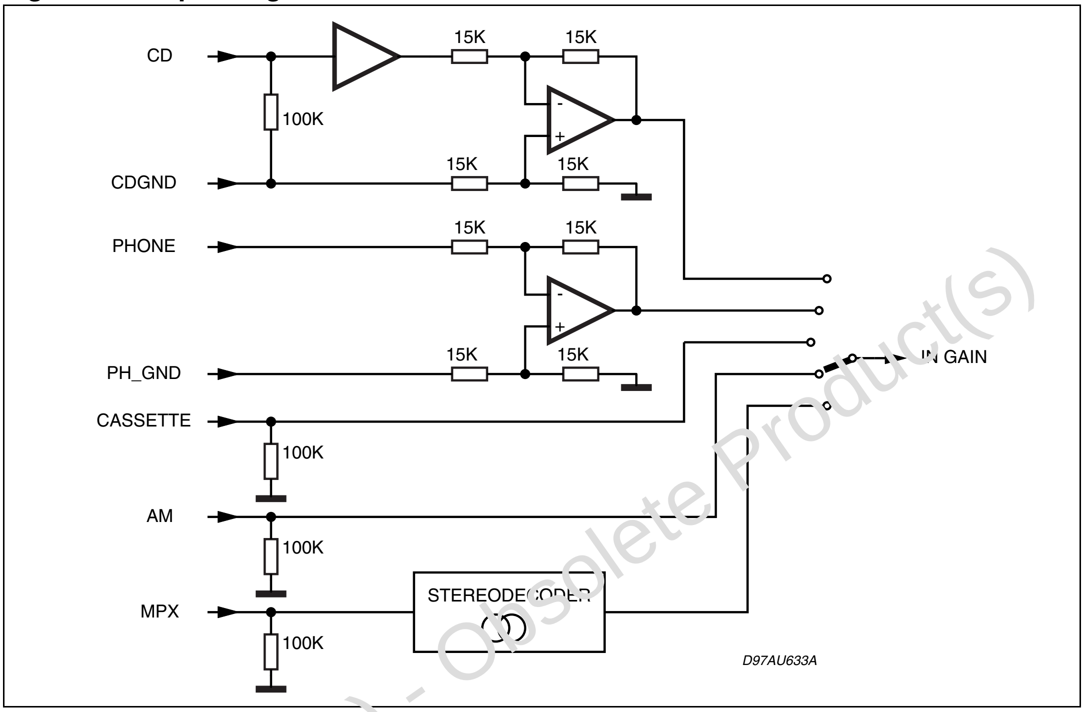
To select the FM, AM or phone source the last five significant bits of subaddress 0 have to be changed, for any other source the last three bits are sufficient (see data byte specification).

3.1.2 Input stages

Most of the input circuits are the same as in previous ST audio processors with exception of the CD inputs (see *Figure 4*). In the meantime there are some CD players in the market having a significant high source impedance which affects strongly the common mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common mode rejection even with those CD players.

The TDA7461 can be configured with an additional input; if the AC coupling before the speaker stage is not used (bit 7 in subaddress 5 set to "1") ACINL and ACINR pins can be used as an additional stereo input.

Figure 4. Input stages



3.1.3 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid that effect a special offset cancellation stage called AutoZero is implemented.

To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the µP is executing a refresh cycle of the I^2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7461 could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

3.2 Mux output

The MUX_L and MUX_R outputs can provide selectively the output of the input multiplexer (Speaker RF register, Byte 8, bit 6=1) or the output of the stereo decoder (Speaker RF register Byte 8 bit 6=0).

If bit D3 byte 10 (Stdec Register) is set to 1, then the stdec signal is automatically muted, when another source is selected at the input multiplexer.

If bit D3 byte 10 (Stdec Register) is set to 0, then the stdec signal will be always available at the Mux out pins, no matter which is the selected source.

The selection of the stereodecoder input, via a special procedure, is recommended.

1. Soft Mute or Mute the signal path
2. Temporary deselect the stereodec
3. Wait 100-200 ms to allow the stdec internal filters to settle
4. Select sterodec input (with automatic autozero)

This procedure guarantees an optimum offsetcancellation, avoiding big DC offsets due to the autozero circuitry, which otherwise could try to compensate the signal sourced at the MPX input instead of the stereodecoder intrinsic offset.

3.3 Mixing stage

This stage offers the possibility to mix the internal beep or the phone signal to any other source.

Due to the fact that the mixing stage is also located behind the In-Gain stage fine adjustments of the main source level can be done in this way.

3.3.1 Loudness

There are four parameters programmable in the loudness stage (see *Figure 5*, *6* and *7*):

- Attenuation
- Center frequency
- Loudness Q
- Flat Mode: in this mode the loudness stage works as a 0 - 15dB attenuator.

Figure 5. Loudness attenuation @ fc = 400 Hz (second order)

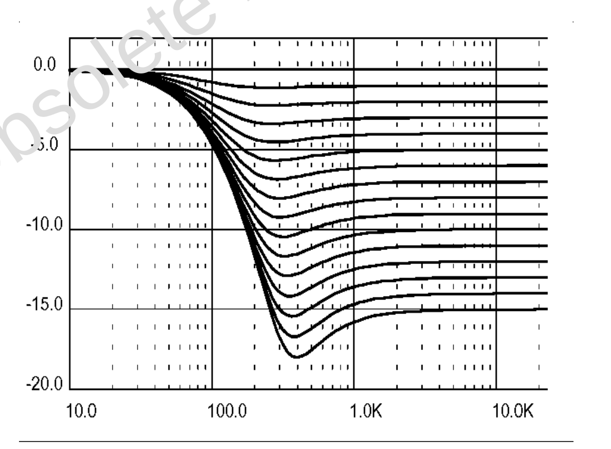


Figure 6. Loudness center frequency @ Atten. = 15 dB (second order)

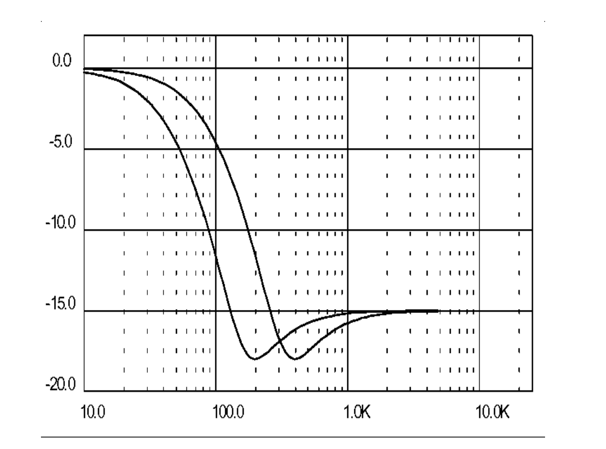
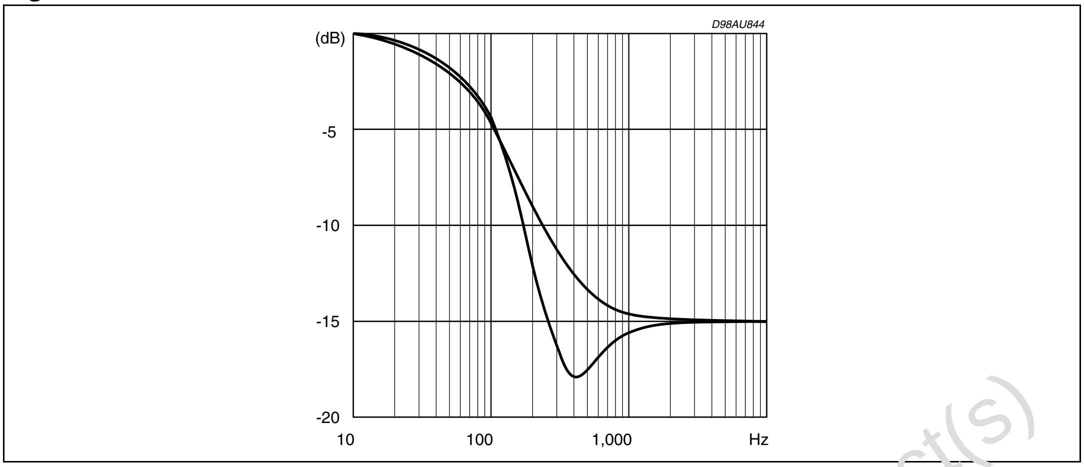


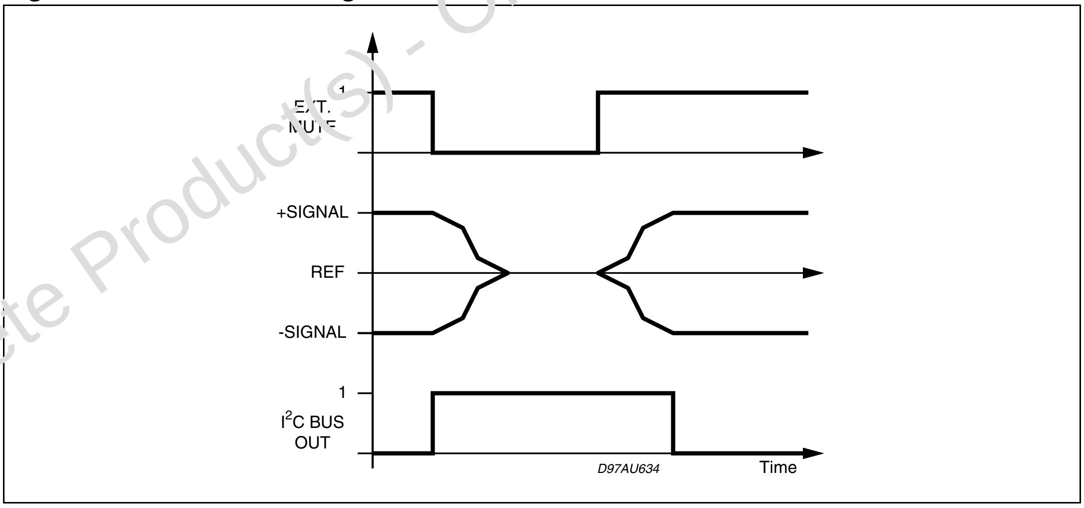
Figure 7. Loudness attenuation = 15 dB @ fc = 400 Hz



3.3.2 Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^{2}C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^{2}C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see *Figure 8*). For timing purposes the Bit 3 of the I^{2}C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 8. Softmute timing

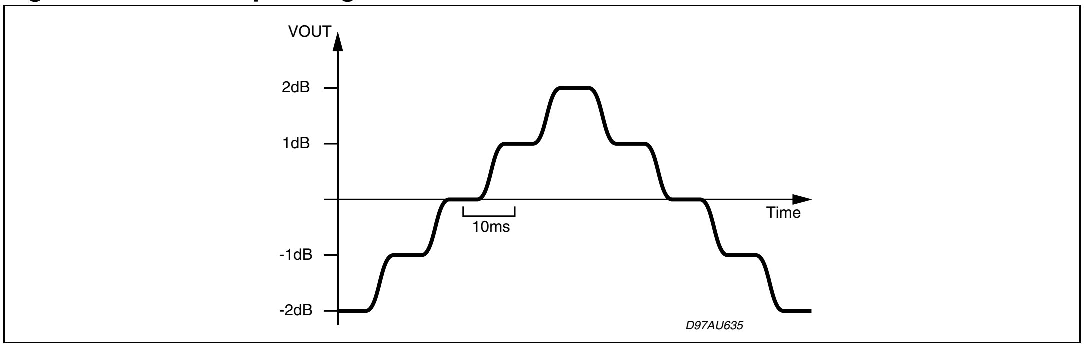


1. Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

3.3.3 Soft step volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Soft step feature both kinds of clicks could be reduced to a minimum and are no more audible (see *Figure 9*).

Figure 9. Soft step timing



1. For steps more than 1dB the soft step mode should be deactivated because it could generate a 1dB error during the blend-time.

3.3.4 Bass

There are three parameters programmable in the bass stage (see *Figure 10*, *11*, *12*, *13*):

- Attenuation
- Center Frequency (60, 70, 80 and 100 Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

3.3.5 DC mode

In this mode the DC gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

3.3.6 Treble

There are two parameters programmable in the treble stage (see *Figure 14*, *15*):

- Attenuation
- Center frequency (10, 12.5, 15 and 17.5 kHz).

3.3.7 Speaker attenuator

Due to practical aspects the steps in the speaker attenuator are not linear over the full range. At attenuations more than 24 dB the steps increase from 1.5 dB to 10 dB (please see data byte specification).

Figure 10. Bass control @ fc = 80 Hz, Q = 1

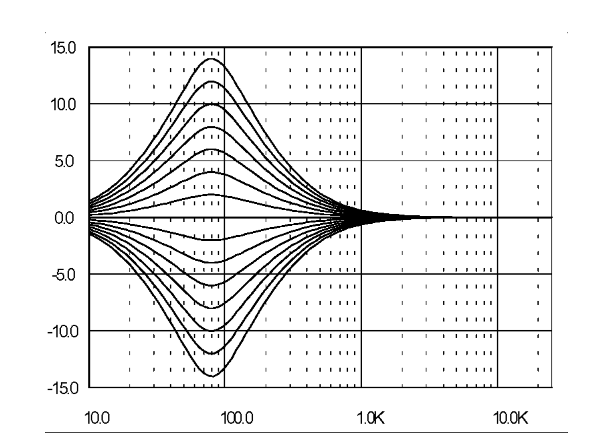


Figure 11. Bass center @ Gain = 14 dB, Q = 1

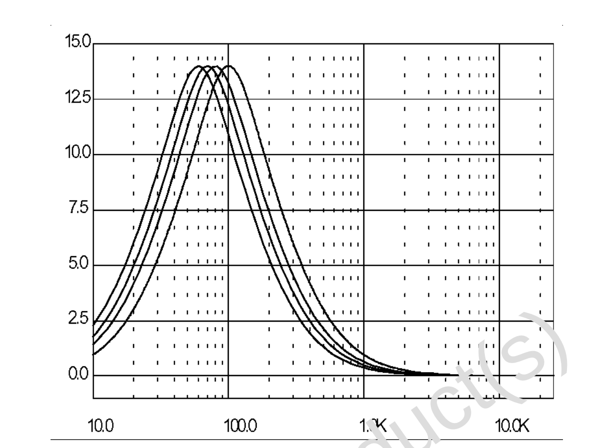


Figure 12. Bass quality factors @ Gain = 14 dB, fc = 80 Hz

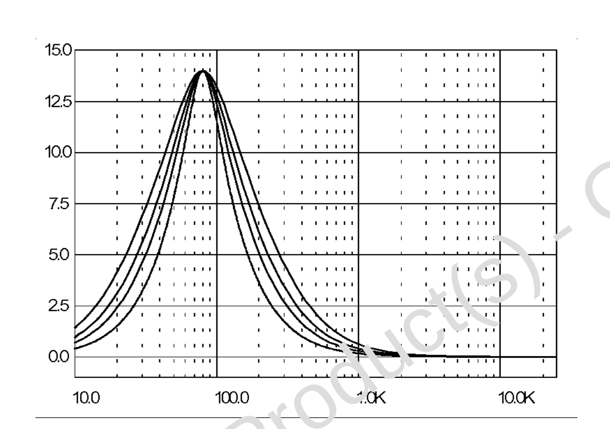


Figure 13. Bass normal and DC mode @ Gain = 14 dB, fc = 80 Hz (1)

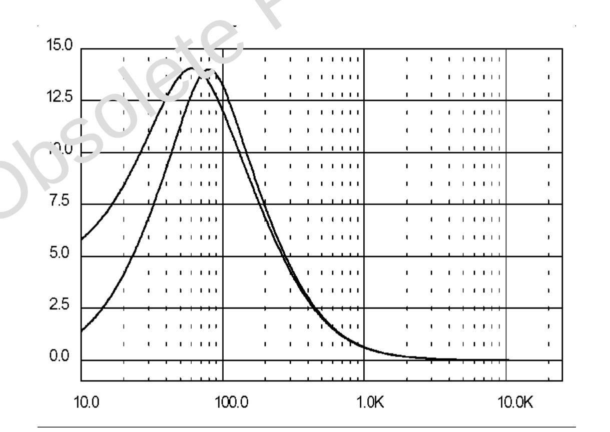


Figure 14. Treble control @ fc = 17.5 kHz)

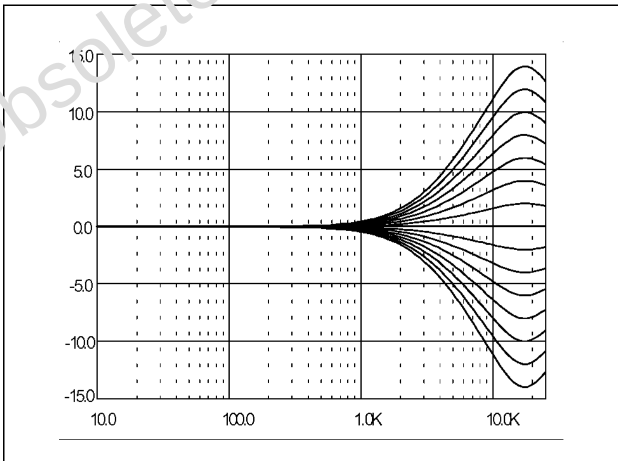
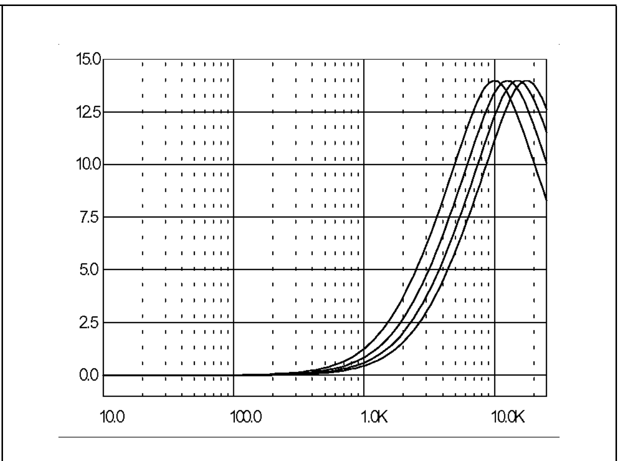


Figure 15. Treble center frequencies @ Gain = 14 dB



1. In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100 Hz.

4 Stereo decoder part

4.1 Stereo decoder feature

- No external components necessary
- PLL with adjustment free fully integrated VCO
- Automatic pilot dependent mono/stereo switching
- Very high suppression of intermodulation and interference
- Programmable roll-off compensation
- Dedicated RDS Softmute
- High cut and stereo blend characteristics programmable in a wide range
- Internal Noise blanker with threshold controls
- Multipath detector with programmable internal/external influence
- I^2C bus control of all necessary functions

4.2 Stereo decoder electrical characteristics

Table 8. Stereo decoder electrical characteristics
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX input level	Input gain = 3.5 dB		0.5	1.25	VRMS
R_{in}	Input resistance		70	100	130	KΩ
G_{min}	Minimum input gain		1.5	3.5	4.5	dB
G_{max}	Max input gain		8.5	11	12.5	dB
G_{STEP}	Step resolution		1.75	2.5	3.25	dB
SVRR	Supply voltage ripple rejection	V_{ripple} = 100 mV, f = 1 kHz		55		dB
a	Max channel separation		30	50		dB
THD	Total harmonic distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus noise to noise ratio	S = 2 V_{rms}	80	91		dB
Mono/stereo switch						
V_{PTHST1}	Pilot threshold voltage	for Stereo, PTH = 1	10	15	25	mV
V_{PTHST0}	Pilot threshold voltage	for Stereo, PTH = 0	15	25	35	mV
V_{PTHMO1}	Pilot threshold voltage	for Mono, PTH = 1	7	12	17	mV
V_{PTHMO0}	Pilot threshold voltage	for Stereo, PTH = 0	10	19	25	mV
PLL						
Δf/f	Capture range		0.5			%

Table 8. Stereo decoder electrical characteristics (continued)
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
De-emphasis and high cut (1)						
τ_{HC50}	De-emphasis time constant	Bit = 7, Subadr. 10 = 0 V_{LEVEL} >> V_{HCH}	25	50	75	µs
τ_{HC75}	De-emphasis time constant	Bit = 7, Subadr. 10 = 1 V_{LEVEL} >> V_{HCH}	50	75	100	µs
τ_{HC50}	High cut time constant	Bit = 7, Subadr. 10 = 0 V_{LEVEL} >> V_{HCL}	100	150	200	µs
τ_{HC75}	High cut time constant	Bit = 7, Subadr. 10 = 1 V_{LEVEL} >> V_{HCL}	150	225	300	µs
Stereo blend and high cut-control						
REF5V	Internal reference voltage		4.7	5	5.3	V
TC_{REF5V}	Temperature coefficient			3300		ppm
L_{Gmin}	Min. level gain		-1	0	+1	dB
L_{Gmax}	Max. level gain		8	10	12	dB
L_{Gstep}	Level gain step resolution		0.3	0.67	1.0	dB
V_{SBLmin}	Min. voltage for mono		29	33	37	%REF5V
V_{SBLmax}	Max. voltage for mono		54	58	62	%REF5V
$V_{SBLstep}$	Step resolution		5.0	8.4	12	%REF5V
$VHCH_{min}$	Min.voltage for no high cut		36	42	46	%REF5V
$VHCH_{max}$	Max. voltage for no high cut		62	66	70	%REF5V
$VHCH_{step}$	Step resolution		5	8.4	12	%REF5V
$VHCL_{min}$	Min. voltage for full high cut		13	17	21	%VHCH
$VHCL_{max}$	Max. voltage for full high cut		29	33	37	%VHCH
Carrier and harmonic suppression at the output						
α19	Pilot signal	f = 19 kHz	40	50		dB
α38	Sub carrier	f = 38 kHz		75		dB
α57	Sub carrier	f = 57 kHz		62		dB
α76	Sub carrier	f = 76 kHz		90		dB
Intermodulation (2))						
α2	Pilot signal	f_{mod} = 10 kHz f_{spur} = 1 kHz;		65		dB
α3		f_{mod} = 13 kHz; f_{spur} = 1 kHz;		75		dB

Table 8. Stereo decoder electrical characteristics (continued)
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Traffic radio [3]						
α57	Signal	f = 57 kHz		70		dB
SCA - Subsidiary communications authorization [4]						
α67	Signal	f = 67 kHz		75		dB
ACI - Adjacent channel interference [5]						
α114	Signal	f = 114 kHz		95		dB
α190	Signal	f = 190 kHz		84		dB

1. By design/characterization but functionally guaranteed through dedicated test mode structure
2. Intermodulation Suppression: measured with: 91% pilot signal; fm = 10kHz or 13kHz.
3. Traffic radio (V.F.) suppression: measured with: 91 % stereo signal; 9 % pilot signal; fm= 1 kHz, 5% sub carrier (f = 57 kHz, fm = 23 Hz AM, m = 60 %)
4. SCA (subsidiary communications authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1 kHz; 1 0% SCA sub carrier (fs = 6 7 kHz, unmodulated).
5. ACI (adjacent channel interference) measured with: 90% mono signal; 9% pilot signal; fm = 1 kHz; 1% spurious signal (fs = 110 kHz or 186 kHz, unmodulated).

4.3 Noise blanker part

- internal 2nd order 140 kHz high pass filter
- programmable trigger threshold
- additional circuits for trigger adjustment (deviation, field-strength)
- very low offset current during hold time
- four selectable pulse suppression times

Table 9. Noise blanker electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger threshold (1), (2)	meas. with V_{PEAK} = 0.9V	NBT = 111		30		mV_{OP}
			NBT = 110		35		mV_{OP}
			NBT = 101		40		mV_{OP}
			NBT = 100		45		mV_{OP}
			NBT = 011		50		mV_{OP}
			NBT = 010		55		mV_{OP}
			NBT = 001		60		mV_{OP}
			NBT = 000		65		mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger Threshold(3)	meas. with V_{PEAK} = 1.5V	NCT = 00		260		mV_{OP}
			NCT = 01		220		mV_{OP}
			NCT = 10		180		mV_{OP}
			NCT = 11		140		mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV		0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 100mV; f = 150KHz		2.2	2.5	2.9	V
$V_{RECT DEV}$	Deviation dependent(4) rectifier voltage	means. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	mV_{OP}
			OVD = 10	0.9	1.2	1.5	mV_{OP}
			OVD = 01	1.7	2.0	2.3	mV_{OP}
			OVD = 00	2.5	2.8	3.1	mV_{OP}
$V_{RECT FS}$	Fieldstrength controlled (5) rectifier voltage	means. with V_{MPX} = 0mV $V_{LEVEL} << V_{SBL}$ (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	1.0	1.3	1.6	V
			FSC = 01	1.5	1.8	2.1	V
			FSC = 00	2.0	2.3	2.6	V

1. All thresholds are measured using a pulse with T_R = 2 µs, T_{HIGH} = 2 µs and T_F = 10 µs.
2. NBT represents the Noise blanker-Byte bits D2; D0 for the noise blanker trigger threshold
3. NAT represents the Noise blanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment
4. OVD represents the Noise blanker-Byte bit pair D7,D6 for the over deviation detector
5. FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control

Figure 16. Noise blanker diagram

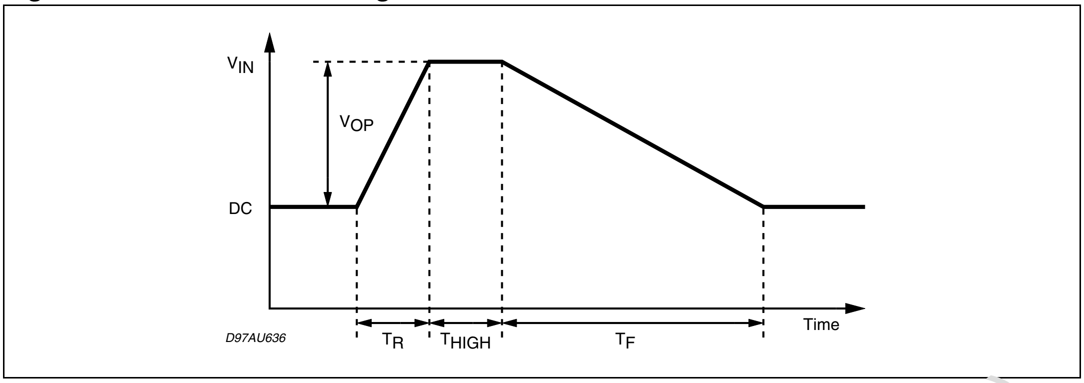


Figure 17. Trigger threshold vs. V_{PEAK}

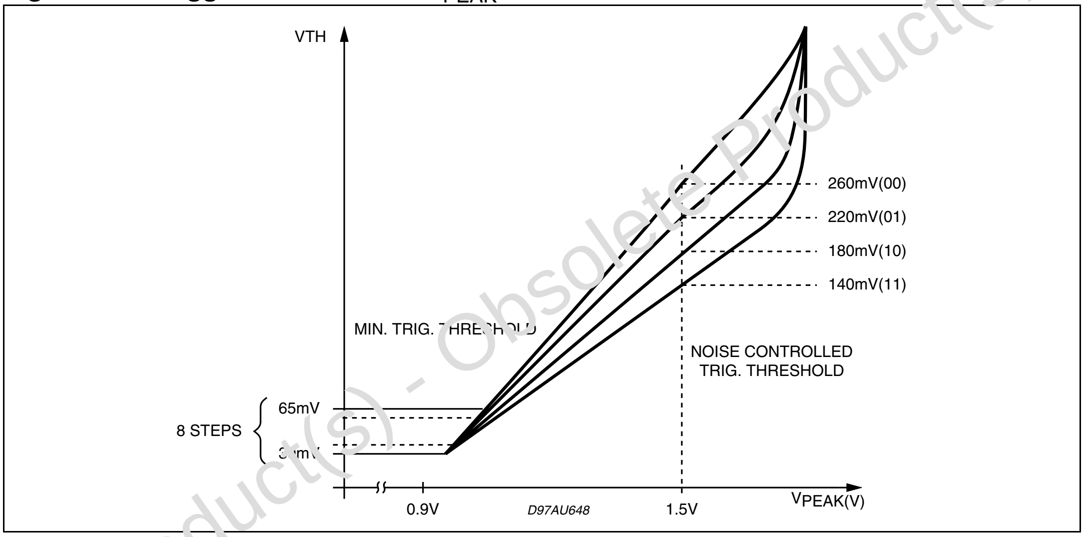


Figure 18. Deviation controlled trigger adjustment

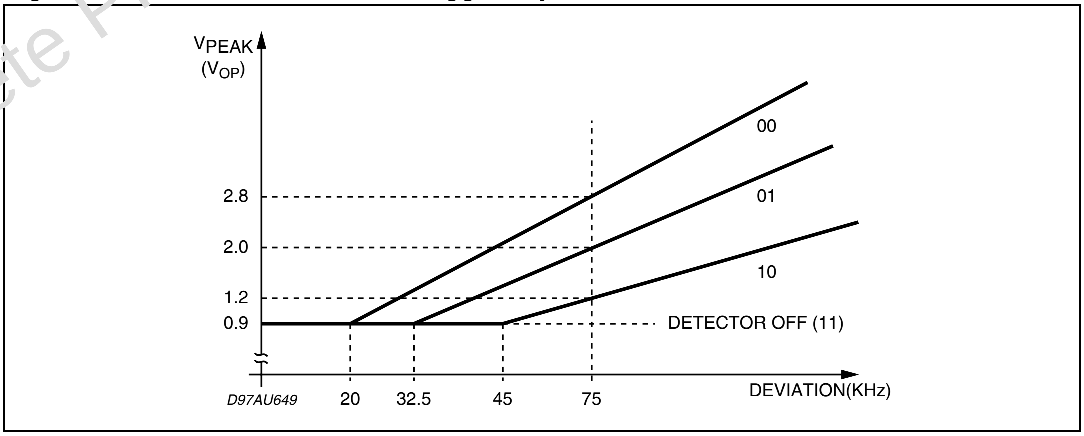
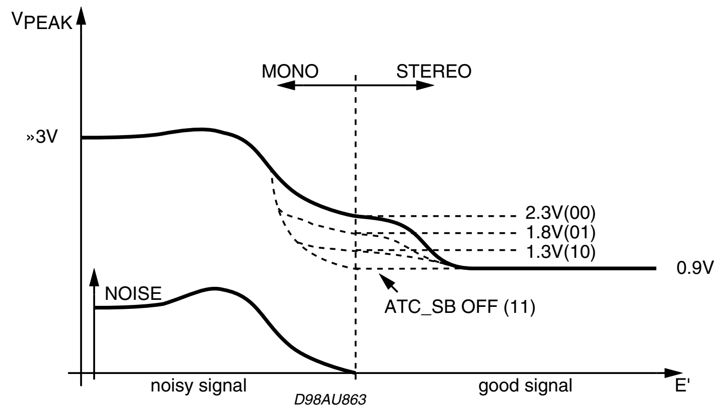


Figure 19. Fieldstrength controlled trigger adjustment



4.4 Multipath detector

- Internal 19 kHz bandpass filter
- Programmable bandpass and rectifier gain
- Two pin solution fully independent usable for external programming
- Selectable internal influence on Stereo blend

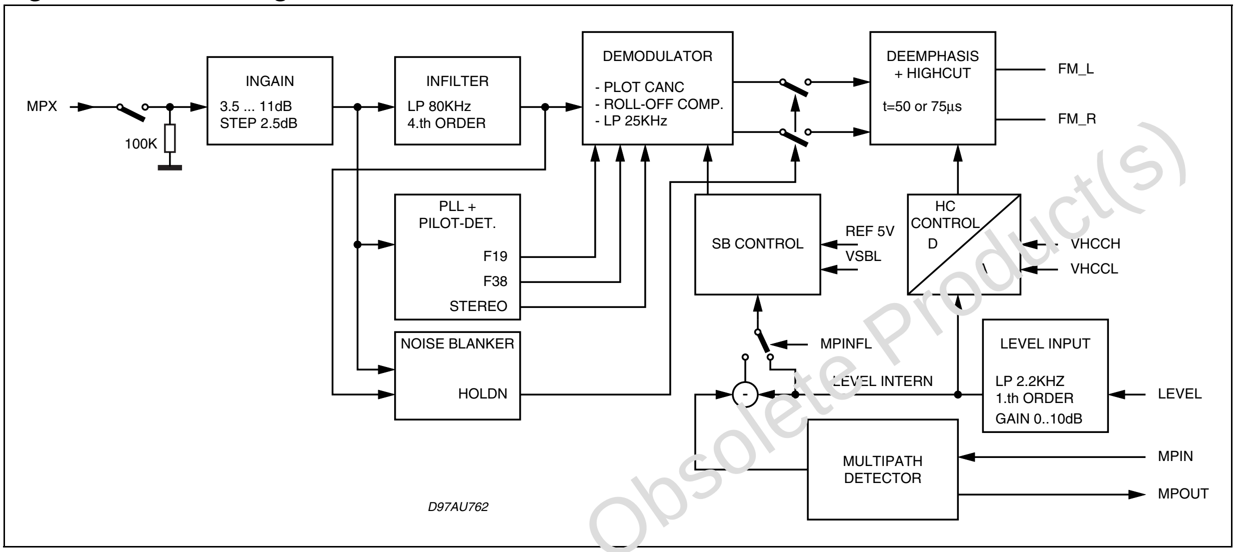
Table 10. Multipath detector electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CMP}	Center frequency of multipath- bandpass	stereo decoder locked on pilot tone		19		KHz
G_{BPMP}	Bandpass gain	bits D_2, D_1 configuration byte = 00		6		dB
		bits D_2, D_1 configuration byte = 01		16		dB
		bits D_2, D_1 configuration byte = 10		12		dB
		bits D_2, D_1 configuration byte = 11		18		dB
G_{RECTMP}	Rectifier gain	bits D_7, D_6 configuration byte = 00		7.6		dB
		bits D_7, D_6 configuration byte = 01		4.6		dB
		bits D_7, D_6 configuration byte = 10		0		dB
I_{CHMP}	Rectifier charge current			1		µA
I_{DISMP}	Rectifier discharge current			1.5		mA

4.5 Description of stereo decoder

The stereo decoder part of the TDA7461 (see *Figure 20*) contains all functions necessary to demodulate the MPX signal like pilot tone dependent mono/stereo switching as well as “stereo blend” and “high cut” functions. Adaptations like programmable input gain, roll-off compensation, selectable de-emphasis time constant and a programmable fieldstrength input allow to use different IF devices.

Figure 20. Block diagram of the stereo decoder



4.5.1 Stereo decoder mute

The TDA7461 has a fast and easy to control RDS mute function which is a combination of the audioprocessor softmute and the high-ohmic mute of the stereo decoder. If the stereo decoder is selected and a softmute command is sent (or activated through the SM pin) the stereo decoder will be set automatically to the high-ohmic mute condition after the audio signal has been soft muted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereo decoder is unmuted immediately and the audioprocessor is softly unmuted. *Figure 21* shows the output signal V_O as well as the internal stereo decoder mute signal. This influence of Softmute on the stereo decoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereo decoder mute command (bit 0, stereo decoder byte set to "1") will set the stereo decoder in any case independently to the high-ohmic mute state.

If any other source than the stereo decoder is selected the decoder remains muted and the MPX pin is connected to Vref to avoid any discharge of the coupling capacitor through leakage currents.

4.5.2 Input stages

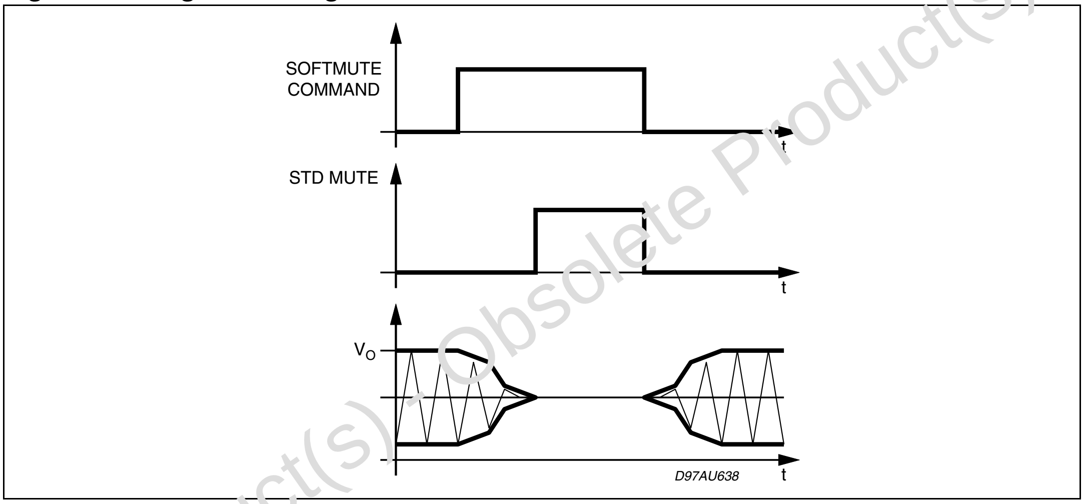
The In gain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80 kHz and is used to attenuate spikes and noise and acts as an anti aliasing filter for the following switch capacitor filters.

4.5.3 Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7461 offers an I^2C bus programmable roll off adjustment which is able to compensate the lowpass behavior of the tuner section.

If the tuner attenuation at 38 kHz is in a range from 20.2 % to 31 % the TDA7461 needs no external network before the MPX pin. Within this range an adjustment to obtain at least 40 dB channel separation is possible. The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation and the fieldstrength control are trimmed.

Figure 21. Signals during stereo decoder's soft mute



4.5.4 De-emphasis and high cut

The lowpass filter for the de-emphasis allows to choose between a time constant of 50 µs and 75 µs (bit D7, Stereo decoder byte).

The high cut control range will be in both cases $t_{HC} = 2 * t_{Deemp}$. Inside the high cut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between t_{Deemp}...$3 \times t_{Deemp}$.

There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values. The high cut function can be switched off by I^2C bus (bit D7, Fieldstrength byte set to "0").

4.5.5 PLL and pilot tone detector

The PLL has the task to lock on the 19 kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilottone threshold VPTHST. Two different thresholds are available. The detector output (signal stereo, see block diagram) can be checked by reading the status byte of the TDA7461 via I^2C bus.

4.5.6 Fieldstrength control

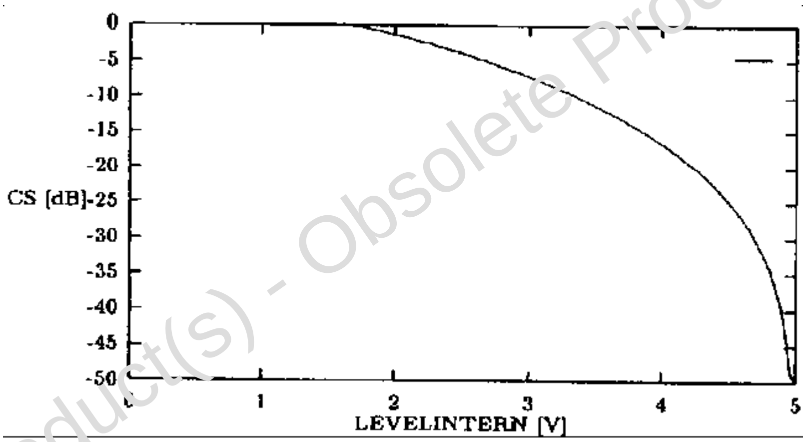
The fieldstrength input is used to control the high cut and the stereo blend function. In addition the signal can be also used to control the noise blanker thresholds.

4.5.7 Level input and gain

To suppress undesired high frequency modulation on the high cut and stereo blend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1st order RC lowpass at 53 kHz (working as anti-aliasing filter) and a 1storder switched capacitor lowpass at 2.2 kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF.

The gain is widely programmable in 16 steps from 0 dB to 10 dB (step = 0.67 dB). These 4 bits are located together with the Roll-Off bits in the "Stereo decoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.

Figure 22. Internal stereo blend characteristics



4.5.8 Stereo blend control

The stereo blend control block converts the internal LEVEL voltage (LEVEL INTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see *Figure 23*).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain L_G and VSBL. To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain LG has to be defined. The following equation can be used to estimate the gain:

$$L_G = \frac{\text{REF5V}}{\text{Field strength voltage[STEREO]}}$$

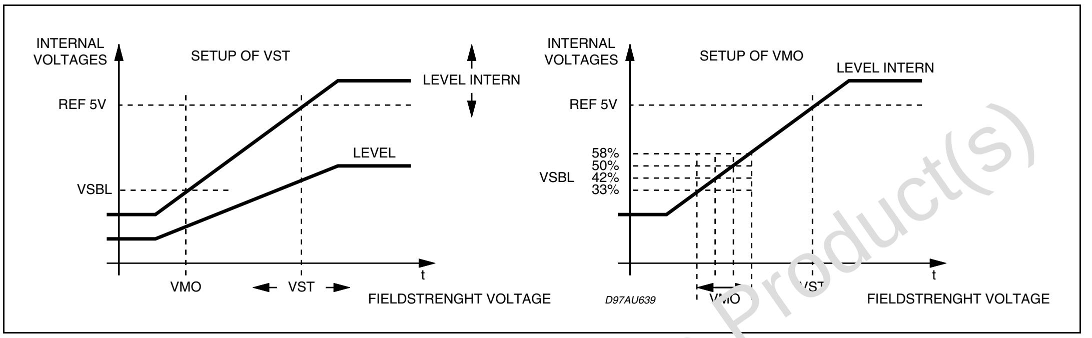
The gain can be programmed through 4 bits in the "Stereo decoder-Adjustment" byte.

The MONO voltage VMO (0 dB channel separation) can be chosen selecting 33, 42, 50 or 58 % of REF5V.

All necessary internal reference voltages like REF5V are derived from a band gap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most IF devices apply a LEVEL voltage with a TC of 3300 ppm. The TDA7461 offers this TC for the reference voltages, too. The TC is selectable with bit D7 of the “stereo decoder adjustment" byte.

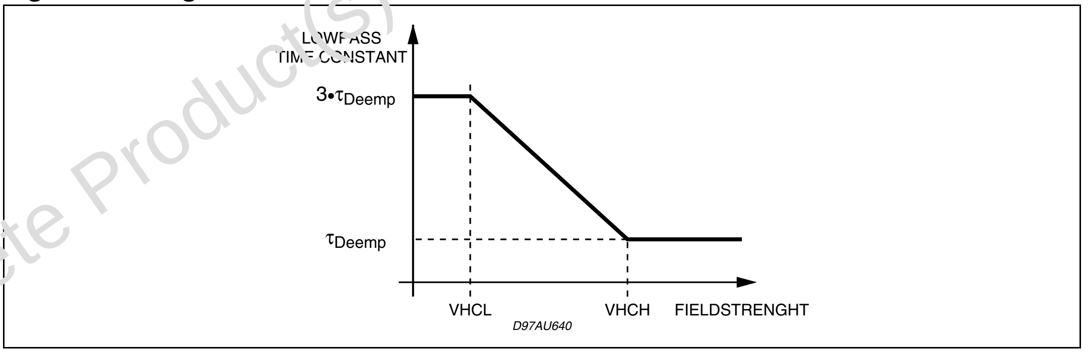
Figure 23. Relation between internal and external LEVEL voltage and setup of Stereo blend



4.5.9 High cut control

The high cut control setup is similar to the stereo blend control setup: the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17 or 33% of VHCH (see *Figure 24*).

Figure 24. High cut characteristics



4.6 FUnctional description of the noise blanker

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noise blanker part is to cancel the audible influence of the spikes. Therefore the output of the stereo decoder is held at the actual voltage for 40 µs.

In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the trigger stage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signal path the noise blanker is supplied by his own biasing circuit.

4.6.1 Trigger path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order highpass-filter has a corner frequency of 140 kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140 kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signalpath for 40 µs.

The block diagram of the noiseblanker is given in *Figure 25*.

4.6.2 Automatic noise controlled threshold adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold:

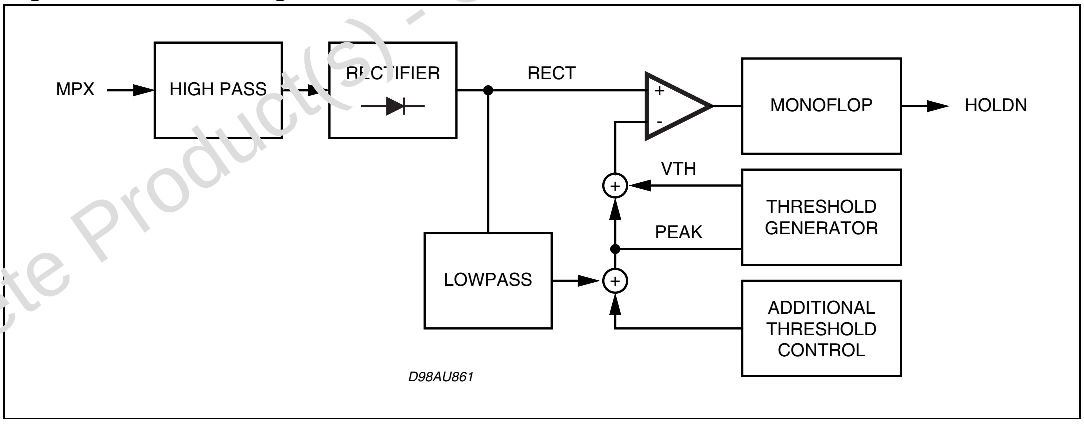
the low threshold in 8 steps (bits D0 to D2 of the noiseblanker byte)

the noise adjusted threshold in 4 steps (bits D3 and D4 of the noiseblanker byte, see fig. 18).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see *Figure 17*).

Figure 25. Block diagram of the noiseblankert



4.6.3 Automatic threshold control

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereo blend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (*Figure 19*). In some cases the behavior of the noise blanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occurs for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.

Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereo blend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the fieldstrength control byte.

4.6.4 Over deviation detector

If the system is tuned to stations with a high deviation the noise blanker can trigger on the higher frequencies of the modulation. To avoid this wrong behavior, which causes noise in the output signal, the noise blanker offers a deviation dependent threshold adjustment. By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereo decoder byte (the first step turns off the detector, see *Figure 18*).

4.7 Functional description of the multipath detector

Using the internal detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19 kHz spectrum in the fieldstrength signal.

Selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the MPOUT pin.

To obtain a optimal performance an adaptation is necessary. Therefore the gain of the 19 kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by the external capacitor value.

4.8 Test mode

During the test mode which can be activated by setting bit D0 of the testing byte and bit D5 of the subaddress byte to "1" several internal signals are available at the CASSR pin. During this mode the input resistance of 100 kΩ is disconnected from the pin. The internal signals available are shown in the software specification.

Figure 26. Block diagram of the multipath detector

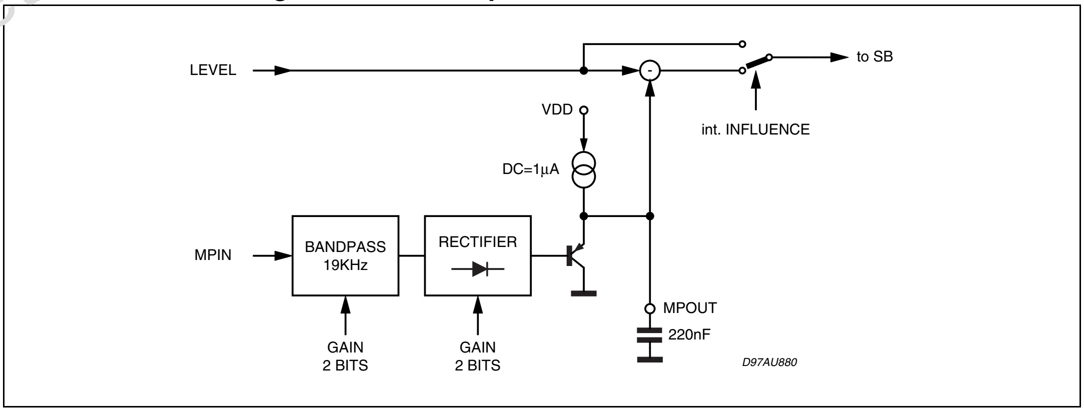
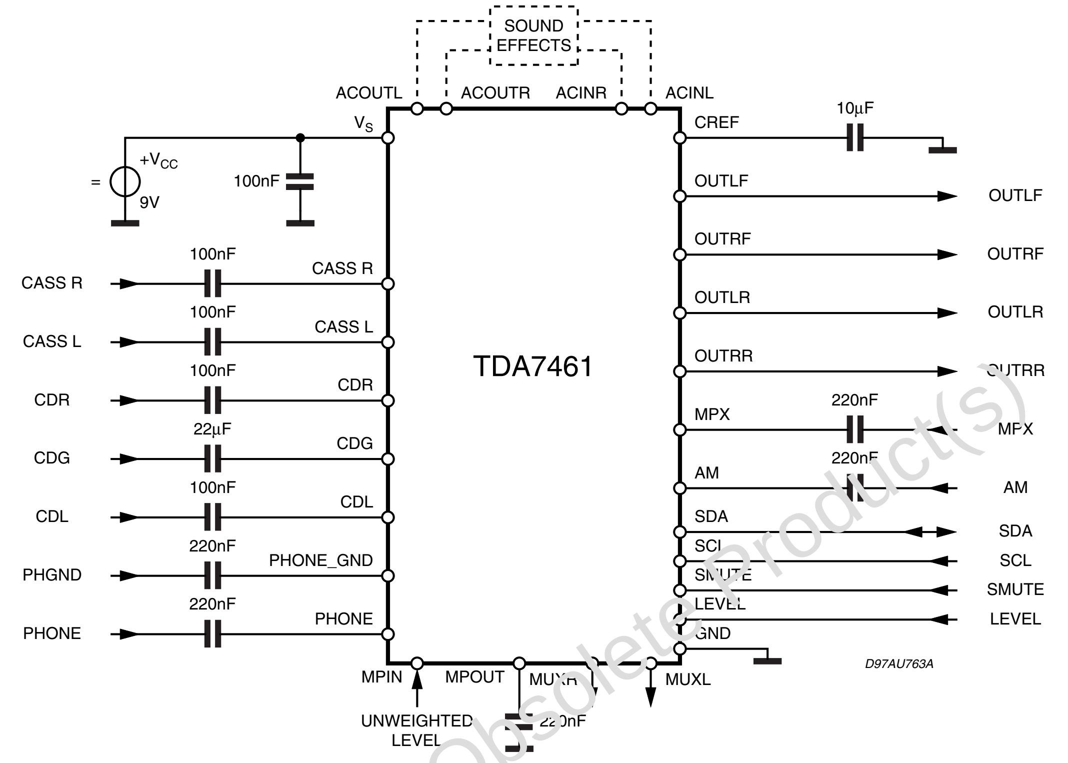
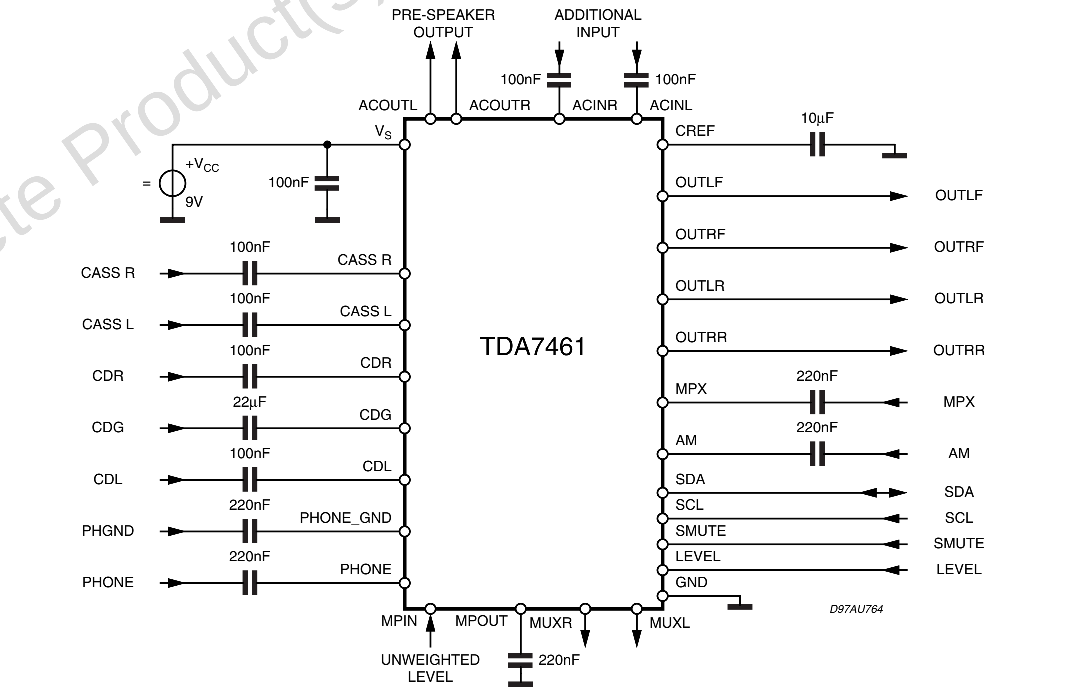


Figure 27. Application example 1



Note: Bit D7 of "Bass and Treble Filter characteristics" set to 1

Figure 28. Application example 2



Note: Bit D7 of "Bass and Treble Filter characteristics" set to 0

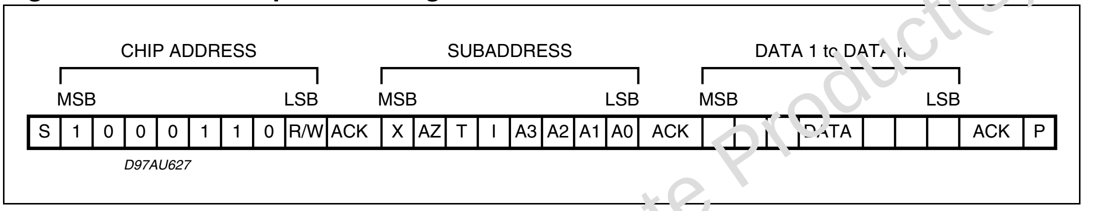
5 I²C bus interface description

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read/ write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 29. Interface protocol diagram



S = Start
ACK = Acknowledge
AZ = AutoZero-Remain
T = Testing
I = Auto increment
P = Stop
Max. clock speed: 500 kbits/s

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

5.2 Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled.

Table 11. Transmitted data (send mode)

MSB							LSB
X	X	X	X	ST	SM	X	X

SM = Soft mute activated
ST = Stereo
X = Not used

Table 12. **Subaddress (receive mode)**

MSB							LSB	FUNCTION
X	AZ	T	I	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness / Auto-Zero
				0	0	1	0	Volume
				0	0	1	1	Softmute / Beep
				0	1	0	0	Bass / Treble Attenuator
				0	1	0	1	Bass / Treble Configuration
				0	1	1	0	Speaker attenuator LF
				0	1	1	1	Speaker attenuator LR
				1	0	0	0	Speaker attenuator RF
				1	0	0	1	Speaker attenuator RR / Blank time adjust
				1	0	1	0	Stereo decoder
				1	0	1	1	Noise blanker
				1	1	0	0	Fieldstrength Control
				1	1	0	1	Configuration
				1	1	1	0	Stereo decoder Adjustment
				1	1	1	1	Testing

T = Testmode

I = Auto increment

AZ = Auto Zero Remain

X = not used

6 Data byte specification

Table 13. Input selector

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Source selector
					0	0	0	CD
					0	0	1	Cassette
					0	1	0	Phone
					0	1	1	AM
					1	0	0	Stereo Decoder
					1	0	1	Input FM
					1	1	0	Mute
					1	1	1	AC inputs
								CD mode
				0				CD Full-differential
				1				CD Quasi-diff
								AM/FM mode
			1		0	1	1	AM mono
			0		0	1	1	AM stereo
			0		1	0	0	AM through Stereo decoder
			1		1	0	0	FM- Stereo decoder
								In-gain
0	0	0						14 dB
0	0	1						12 dB
:	:	:						:
1	1	0						2 dB
1	1	1						0 dB

For example to select the CD input in quasi-differential mode with gain of 8 dB the Data Byte is: 0/01111000

Table 14. Loudness

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Attenuation
				0	0	0	0	0 dB
				0	0	0	1	-1 dB
				:	:	:	:	:
				1	1	1	0	-14 dB
				1	1	1	1	-15 dB
								Filter
			0					on
			1					off (flat)
								Center frequency
		0						200 Hz
		1						400 Hz
								Loudness Q
	0							low (1st order)
	1							normal (2nd order)
1								must be "1"

Note: The attenuation is specified at high frequencies. Around the center frequency the value is different depending on the programmed attenuation (see Loudness frequency response).

Table 15. Mute, Beep and Mixing

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Mute
							0	Enable Softmute
							1	Disable Softmute
					0	0		Mute time =0.48 ms
					0	1		Mute time =0.96 ms
					1	0		Mute time =40.4 ms
					1	1		Mute time =324 ms
				0				Stereo decoder softmute influence = off
				1				Stereo decoder softmute influence = on
								Beep
			0					Beep Frequency = 600 Hz
			1					Beep Frequency = 1.2 kHz
								Mixing
		0						Mix-Source = Beep
		1						Mix-Source = Phone
0	0							Full Mix Signal
0	1							Source -12 dB + Mix-Signal -2.5 dB
1	0							Source -6 dB + Mix-Signal -6 dB
1	1							Full Source

Note: for more information to the Stereo decoder-Softmute-Influence please refer to the stereo decoder description.

Table 16. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	+32 dB
	0	0	0	0	0	0	1	+31 dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	0	0	+20 dB
	0	0	0	1	1	0	1	+19 dB
	0	0	0	1	1	1	0	+18 dB
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	+1 dB
	0	1	0	0	0	0	0	0 dB
	0	1	0	0	0	0	1	- 1 dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	0	-78 dB
	1	1	0	1	1	1	1	-79 dB
								Soft step
0								Soft step volume = off
1								Soft step volume = on

Note: It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

Table 17. Bass and treble attenuation

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Treble steps
				0	0	0	0	-14 dB
				0	0	0	1	-12 dB
				:	:	:	:	:
				0	1	1	0	-2 dB
				0	1	1	1	0 dB
				1	1	1	1	0 dB
				1	1	1	0	+2 dB
				:	:	:	:	:
				1	0	0	1	+12 dB
				1	0	0	0	+14 dB
								Bass steps
0	0	0	0					-14 dB
0	0	0	1					-12 dB
:	:	:	:					:
0	1	1	0					-2 dB
0	1	1	1					0 dB
1	1	1	1					0 dB
1	1	1	0					+2 dB
:	:	:	:					:
1	0	0	1					+12 dB
1	0	0	0					+14 dB

For example 12dB Treble and -8dB Bass give the following data byte: 0 0 1 1 1 0 0 1.

Table 18. Bass and treble filter characteristics

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble
						0	0	Center Frequency = 10 kHz
						0	1	Center Frequency = 12.5 kHz
						1	0	Center Frequency = 15 kHz
						1	1	Center Frequency = 17.5 kHz
								Bass
				0	0			Center Frequency = 60 Hz
				0	1			Center Frequency = 70 Hz
				1	0			Center Frequency = 80 Hz
				1	1			Center Frequency = 100 Hz
		1	1	1	1			Center Frequency = 150 Hz
		0	0					Quality factor = 1
		0	1					Quality factor = 1.25
		1	0					Quality factor = 1.5
		1	1					Quality factor = 2
	0							DC-Gain = 0 dB
	1							DC-Gain = ±4.4 dB
								AC Coupling(1)
0								For External Connection
1								Internally Connection

1. For deeper information see application examples *Figure 27* and *28*.

For example Treble center frequency = 15kHz, Bass center frequency = 100Hz, Bass Q = 1 and DC = 0dB give the following DATA BYTE: 1 0 0 0 1 1 1 0

Table 19. Speaker attenuation (LF, LR, RF, RR)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Attenuation
		0	0	0	0	0	0	0 dB
		0	0	0	0	0	1	-1 dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	-23 dB
		0	1	1	0	0	0	-24.5 dB
		0	1	1	0	0	1	-26 dB
		0	1	1	0	1	0	-28 dB
		0	1	1	0	1	1	-30 dB
		0	1	1	1	0	0	-32 dB
		0	1	1	1	0	1	-35 dB
		0	1	1	1	1	0	-40 dB
		0	1	1	1	1	1	-50 dB
		1						Speaker Mute
1	1							Must be "1" (except RF, RR speaker; see below)
								Blank Time adj. (subaddress speaker RR)
0	0							38 µs
0	1							25.5 µs
1	0							32 µs
1	1							22 µs
								Output selector for pins 15 and 16. subaddress speaker RF)
	0							Stereo decoder output selected
	1							Input multiplexer output selected

Table 20. Stereo decoder

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
							0 1	STD unmuted STD muted
					0 0 1 1	0 1 0 1		IN-Gain 11 dB IN-Gain 8.5 dB IN-Gain 6 dB IN-Gain 3.5 dB
				1 0				Stereo decoder Unmuted with Stdec Input selected and automatically Muted at the selection of any other source. Stereo decoder Unmuted whichever is the selected source.
		1 0	 1					Forced mono Mono/stereo switch automatically
	0 1							Pilot threshold high Pilot threshold low
0 1								De-emphasis 50 µs De-emphasis 75 µs

Table 21. Noise blanker

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Low threshold 65 mV Low threshold 60 mV Low threshold 55 mV Low threshold 50 mV Low threshold 45 mV Low threshold 40 mV Low threshold 35 mV Low threshold 30 mV
			0 0 1 1	0 1 0 1				Noise controlled threshold 320 mV Noise controlled threshold 260 mV Noise controlled threshold 200 mV Noise controlled threshold 140 mV
		0 1						Noise blanker off Noise blanker on
0 0 1 1	0 1 0 1							Over deviation adjust 2.8 V Over deviation adjust 2.0 V Over deviation adjust 1.2 V Over deviation detector off

Table 22. **Field strength control**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	Noise blanker Field strength Adj 2.3 V
						0	1	Noise blanker Field strength Adj 1.8 V
						1	0	Noise blanker Field strength Adj 1.3 V
						1	1	Noise blanker Field strength Adj Off
				0	0			VSBL at 33 % REF 5 V
				0	1			VSBL at 42 % REF 5 V
				1	0			VSBL at 50 % REF 5 V
				1	1			VSBL at 58 % REF 5 V
		0	0					VHCH at 42 % REF 5 V
		0	1					VHCH at 50 % REF 5 V
		1	0					VHCH at 58 % REF 5 V
		1	1					VHCH at 66 % REF 5 V
	1							VHCL at 17 % VHCH
	0							VHCL at 33 % VHCH
0								High cut OFF
1								High cut ON

Table 23. **Configuration**

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Noise rectifier discharge resistor
						0	0	R = infinite
						0	1	R = 56 kΩ
						1	0	R = 33 kΩ
						1	1	R =18 kΩ
								Multipath detector bandpass gain
				0	0			6 dB
				0	1			16 dB
				1	0			12 dB
				1	1			18 dB
								Multipath detector internal influence
			0					On
			1					Off
		1						Mute be “1”
								Multipath detector reflection gain
0	0							Gain = 7.6 dB
0	1							Gain = 4.6 dB
1	0							Gain = 0 dB
1	1							Off

Table 24. Stereo decoder adjustment

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Roll-off compensation
					0	0	0	not allowed
					0	0	1	20.2%
					0	1	0	21.9%
					:	:	:	:
					1	0	0	25.5%
					:	:	:	:
					1	1	1	31.0%
								Level gain
	0	0	0	0				0dB
	0	0	0	1				0.66 dB
	0	0	1	0				1.33 dB
	:	:	:	:				:
	1	1	1	1				10 dB
								Temperature compensation at level input
0								TC = 0
1								TC = 16.7 mV/K (3300 ppm)

Table 25. Testing

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Stereo decoder test signals
							0	OFF
							1	Test signals enabled if bit D5 of the subaddress (test mode bit) is set to "1", too
						0		External Clock
						1		Internal Clock
								Test signals at CASS_R
		0	0	0	0			VHCCH
		0	0	0	1			Level intern
		0	0	1	0			Pilot magnitude
		0	0	1	1			VCOCON: VCO Control Voltage
		0	1	0	0			Pilot threshold
		0	1	0	1			HOLDN
		0	1	1	0			NB threshold
		0	1	1	1			F228
		1	0	0	0			VHCCL
		1	0	0	1			VSBL
		1	0	1	0			not used
		1	0	1	1			not used
		1	1	0	0			PEAK
		1	1	0	1			not used
		1	1	1	0			REF5V
		1	1	1	1			not used
								VCO
	0							Off
	1							On
								Audio processor test mode
0								Only if bit D5 of the subaddress (test mode bit) is set to "1"
1								Off

Note: This byte is used for testing or evaluation purposes only and must not be set to other values than the default "11111110" in the application!

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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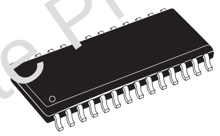
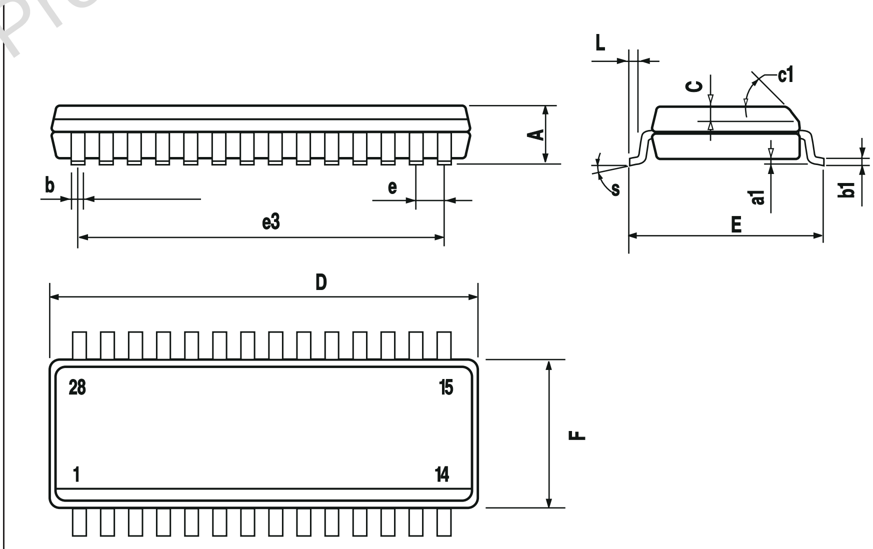
Figure 30. SO-28 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



8 Revision history

Table 26. Document revision history

Date	Revision	Changes
20-Oct-2003	6	Initial release.
13-Jan-2009	7	Document reformatted. Document status changed from datasheet to “not for new design”. Removed all refences to DIP28 package. Added *Table 1: Device summary on page 1*. Updated *Section 7: Package information on page 46*.