NB7NPQ7021M

3.3 V USB 3.1 Dual Channel Linear Redriver

ON Semiconductor®

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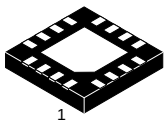


UQFN16
CASE 523AF

MARKING DIAGRAM

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

Description

The NB7NPQ7021M is a 3.3 V dual channel redriver for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7NPQ7021M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter. The Flat Gain and Equalization are controlled by four level control pins. Each channel has a set of independent control pins to make signal optimization possible.

After power up, the NB7NPQ7021M periodically checks both of the TX output pairs for a receiver connection. When the receiver is detected on both channels the RX termination becomes enabled and the NB7NPQ7021M is set to perform the redriver function.

The NB7NPQ7021M comes in a small 3 x 3 mm UQFN16 package and is specified to operate across the entire industrial temperature range of –40°C to 85°C.

Features

- 3.3 V ± 5% Power Supply
- Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic Receiver Termination Detection
- Integrated Input and Output Termination
- Independent, Selectable Equalization and Flat Gain
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range: –40°C to 85°C
- Small 3 x 3 x 0.5 mm UQFN16 Package, Flow Through Design that ease PCB layout
- This is a Pb−Free Device

Typical Applications

- USB3.1 Type−C and Type−A Signal Routing
- Mobile Phone and Tablet
- Computer and Laptop
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

ORDERING INFORMATION

Device	Package	Shipping†
NB7NPQ7021MMUTXG	UQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

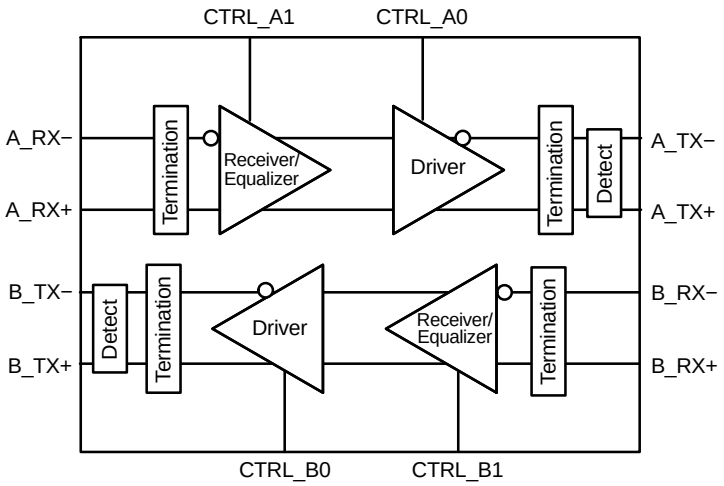


Figure 1. Logic Diagram of NB7NPQ7021M

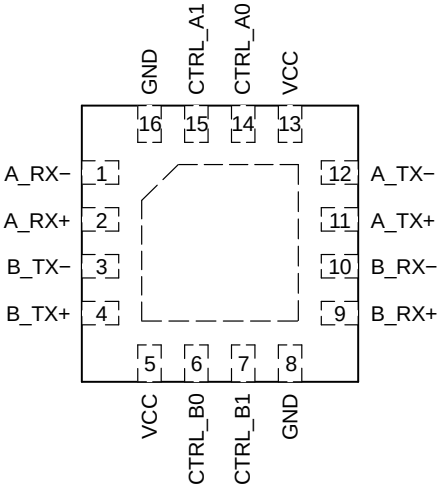


Figure 2. UQFN16 Package Pinout
(Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	A_RX-	DIFF IN	Channel A Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
2	A_RX+		
3	B_TX−	DIFF OUT	Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
4	B_TX+		
5	VCC	Power	3.3 V power supply. VCC pins must be externally connected to power supply to guarantee proper operation.
6	CTRL_B0	LVCMOS IN	Control pin “B0” for equalization and flat gain on Channel B. 4−state input with integrated pull−up and pull−down resistors. See Table 2.
7	CTRL_B1	LVCMOS IN	Control pin “B1” for equalization and flat gain on Channel B. 4−state input with integrated pull−up and pull−down resistors. See Table 2.
8	GND	GND	Reference Ground. GND pins must be externally connected to power supply to guarantee proper operation.
9	B_RX+	DIFF IN	Channel B Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
10	B_RX−		
11	A_TX+	DIFF OUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
12	A_TX-		
13	VCC	Power	3.3 V power supply. VCC pins must be externally connected to power supply to guarantee proper operation.
14	CTRL_A0	LVCMOS IN	Control pin “A0” for equalization and flat gain on Channel A. 4−state input with integrated pull−up and pull−down resistors. See Table 2.
15	CTRL_A1	LVCMOS IN	Control pin “A1” for equalization and flat gain on Channel A. 4−state input with integrated pull−up and pull−down resistors. See Table 2.
16	GND	GND	Reference Ground. GND pins must be externally connected to power supply to guarantee proper operation.
EP	GND	GND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is not electrically connected to the die, but is recommended to be soldered to GND on the PC Board.

DEVICE CONFIGURATION

Table 2. CONTROL PIN EFFECTS (Typical Values)

Setting #	Channel A		Channel B		Equalization	Flat Gain
	CTRL_A1	CTRL_A0	CTRL_B1	CTRL_B0	(dB)	(dB)
1	L	L	L	L	5	0
2	L	R	L	R	7	0
3	L	F	L	F	8	0
4	L	H	L	H	9	0
5	R	L	R	L	10	0
6	R	R	R	R	3	2
7	R	F	R	F	4	2
8	R	H	R	H	5	2
9	F	L	F	L	7	2
10	F	R	F	R	8	2
11 (Default)	F	F	F	F	8	−1
12	F	H	F	H	5	−1
13	H	L	H	L	7	−1
14	H	R	H	R	9	−1
15	H	F	H	F	11	−1
16	H	H	H	H	7	−1

NOTE: Equalization and DC flat Gain may be set by adjusting the voltage to the control pins. There are 4 specific levels, High “H”, Low “L”, Rexternal “R”, and Float “F”. Please see Table 7 for voltage levels.

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	≤ 4 kV ≤ 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		20330
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{CC}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	1.89	V
	LVCMOS inputs	−0.5	V_{CC} + 0.5	V
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Operating Ambient Temperature Range, T_A		−40	85	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 3)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. RECOMMENDED OPERATING CONDITIONS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Nom	Max	Unit
V_{CC}	Main power supply	3.135	3.3	3.465	V
T_A	Operating free−air temperature	−40		+85	°C
C_{AC}	AC coupling capacitor	75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. POWER SUPPLY CHARACTERISTICS

Parameter		Test Conditions	Min	Typ (Note 4)	Max	Unit
I_{CC}	Active	Link in U0 with Super Speed Plus data transmission		130		mA
	U2/U3	Link in U2 or U3 power saving state		2		mA
	No USB Connection	No connection state, termination disabled		560		μA

4. TYP values use V_{CC} = 3.3 V, T_A = 25°C.

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS 4−State LVCMOS Inputs (CTRL_A0, CTRL_A1, CTRL_B0, CTRL_B1)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IL}	DC Input Setting “L”	Input pin connected to GND		GND	0.1*V_{CC}	V
V_{IR}	DC Input Setting “R”	A specified resistor must be applied between pin and GND	0.23*V_{CC}	0.33*V_{CC}	0.43*V_{CC}	V
V_{IF}	DC Input Setting “F”	Input pin is left floating	0.56*V_{CC}	0.66*V_{CC}	0.76*V_{CC}	V
V_{IH}	DC Input Setting “H”	Input pin connected to V_{CC}		V_{CC}		V
R_{PU}	Internal pull−up resistance			100		kΩ
R_{PD}	Internal pull−down resistance			200		kΩ
I_{IH}	High−level input current	V_{IN} = 3.465 V			25	μA
I_{IL}	Low−level input current	V_{IN} = GND, VCC = 3.465 V	−45			μA
R_{ext}	External Resistor for input setting “R”			68		kΩ

5. Floating refers to a pin left in an open state, with no external connections.

Table 8. RECEIVER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{RX-DIFF-pp}$	Input differential voltage swing	AC−coupled, peak−to−peak differential	100		1200	mV_{PP}
V_{RX-CM}	Common−mode voltage bias in the receiver (DC)			V_{CC}		V
$Z_{RX-DIFF}$	Differential input Resistance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{RX-CM}	Common−mode input Resistance (DC)	Present after an USB device is detected on TX+/TX−	20	25	30	Ω
$Z_{RX-HIGH-IMP}$	Common−mode input Resistance with termination disabled (DC)	Present when no USB device is detected on TX+	25	190		kΩ
$V_{TH-LFPS-pp}$	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Output voltage is considered squelched below 25 mV.	100	200	300	mV_{PP}

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 9. TRANSMITTER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{sw_100M}	−1 dB compression point Output swing at 100 MHz	100 MHz Sine Wave		1200		mV_{PPd}
V_{sw_5G}	−1 dB compression point Output swing at 5 GHz	5 GHz Sine Wave		900		mV_{PPd}
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX-DIFF}$	Differential output impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{TX-CM}	Common−mode output impedance (DC)	Present after an USB device is detected on TX+/TX−	20	25	30	Ω
I_{TX-SC}	TX short circuit current	TX+ or TX− shorted to GND		40		mA
V_{TX-CM}	Common−mode voltage bias in the transmitter (DC)	100 mV, 50 MHz, 5 Gbps and 10 Gbps, prbs 2^7		V_{CC}− 0.8	V_{CC}	V
$V_{TX-CM-ACpp}$	AC common−mode peak−to−peak Voltage swing in active mode	Within U0 and at 50 MHz (LFPS)			100	mV_{PP}
$V_{TX-IDLE-DIFF-ACpp}$	Differential voltage swing during electrical idle	Tested with a high−pass filter	0		10	mV_{PP}
$V_{TX-RXDET}$	Voltage change to allow receiver detect	The change in voltage that triggers detection of a receiver.		325	600	mV
t_R, t_F	Output rise, fall time	20% − 80% of differential voltage measured 1 inch from the output pin, 1 GHz clock, 800 mV differential amplitude		35		ps
t_{RF-MM}	Output rise, Fall time mismatch	20% − 80% of differential voltage measured 1 inch from the output pin			10	ps
$t_{diff-LH}$, $t_{diff-HL}$	Differential propagation delay	Propagation delay between 50% level at input and output		110		ps
$t_{idleExit}$	Idle exit time	50 MHz clock signal, EQ an FG setting “11 (Default)”		10		ns
$t_{idleEntry}$	Idle entry time	50 MHz clock signal, EQ an FG setting “11 (Default)”		60		ps

Table 10. TIMING AND JITTER CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
TIMING						
t_{READY}	Time from power applied until RX termination is enabled	Apply 0 V to V_{CC}, connect USB termination to TX±, apply 3.3 V to V_{CC}, and measure when $Z_{RX-DIFF}$ is enabled		100		ms
JITTER FOR 5 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 6, 7)	EQ = 5 dB, FG = 0 dB, EQ and FG Setting “LL”		0.20		UI
D_{JTX}	Deterministic jitter (Note 7)			0.10		UI
R_{JTX}	Random jitter (Note 7)			0.07		UI
JITTER FOR 10 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 6, 7)	EQ = 5 dB, FG = 0 dB, EQ and FG Setting “LL”		0.22		UI
D_{JTX}	Deterministic jitter (Note 7)			0.08		UI
R_{JTX}	Random jitter (Note 7)			0.06		UI

6. Includes RJ at 10^{-12}.
7. Measured at the ends of reference channel with a K28.5 pattern, VID = 1000 mVpp, −3.5 dB de−emphasis from source.
8. 5 Gbps, UI = 200 ps for 10 Gbps, UI = 100 ps

PARAMETER MEASUREMENT DIAGRAMS

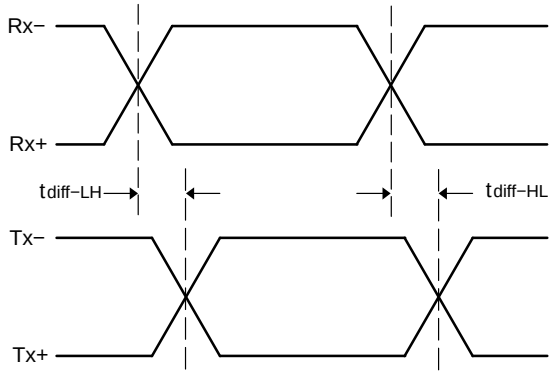


Figure 3. Propagation Delay

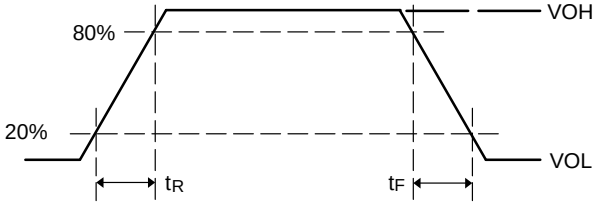


Figure 4. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. The NB7NPQ7021M is tested as a part of a USB compliant system to ensure that it maintains compliance while increasing system performance.

LFPS Functionality

USB 3.1, Gen1 and Gen2 use Low Frequency Periodic Signaling (LFPS) to implement functions like exiting low−power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB−IF. In order to toggle through these patterns for various tests, the receiver must receive a ping. LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100 ns at 20 MHz.

Control Pin Settings

Control pins A1, A0, B1, and B0 control the flat gain and the equalization of channels A and B of the NB7NPQ7021M Device.

The Float (Default) Setting “F” can be set by leaving the control pins in a floating state. The Redriver will internally bias the control pins to the correct voltage to achieve this if the pin is not connected to a voltage source. The low setting “L” can be set by pulling the control pin to ground. Likewise the high setting “H” can be set by pulling the pin high to VCC. The $R_{external}$ setting can be set by adding a 68 K resistor from the control pin to ground. This will bias the Redriver internal voltage to 33% of VCC.

Linear Equalization

The linear equalization that the NB7NPQ7021M provides compensates for losses that occur naturally along board traces and cable lines. Linear Equalization boosts high frequencies and lower frequencies linearly so when transmitting at varying frequencies, the voltage amplitude will remain consistent. This compensation electrically counters losses and allows for longer traces to be possible when routing.

DC Flat Gain

DC flat gain equally boosts high and low frequency signals, and is essential for countering low frequency losses. DC flat gain can also be used to simulate a higher input signal from a USB Controller. If a USB controller can only provide 800 mV differential to a receiver, it can be boosted to 1128 mV using 3 dB of flat gain.

Total Gain

When using Flat Gain with Equalization in a USB application it is important to make sure that the total voltage does not exceed 1200 mV. Total gain can be calculated by adding the EQ gain to the Flat Gain.

TYPICAL APPLICATION

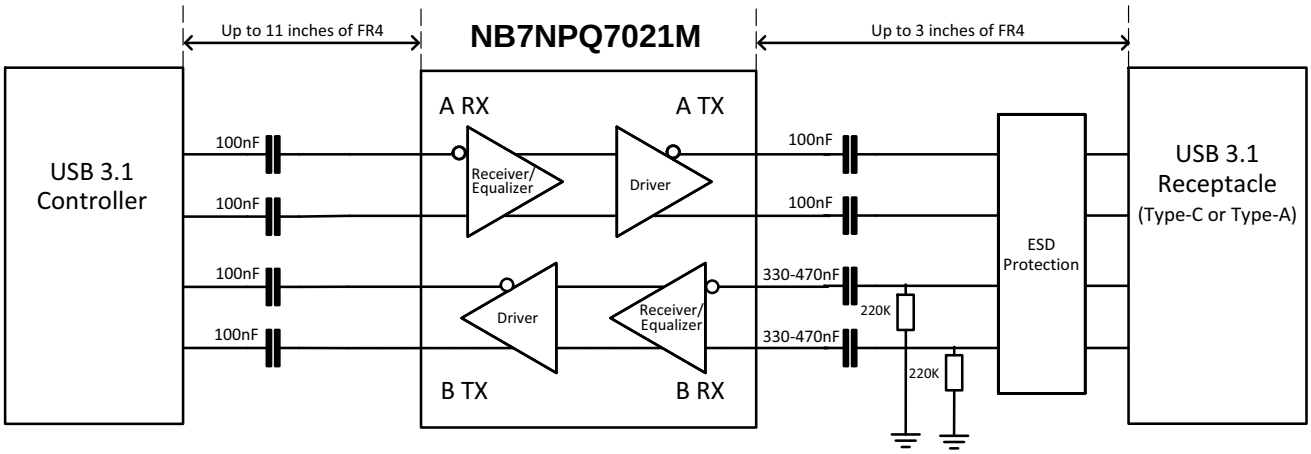


Figure 5. USB 3.1 Host Side NB7NPQ7021M Application

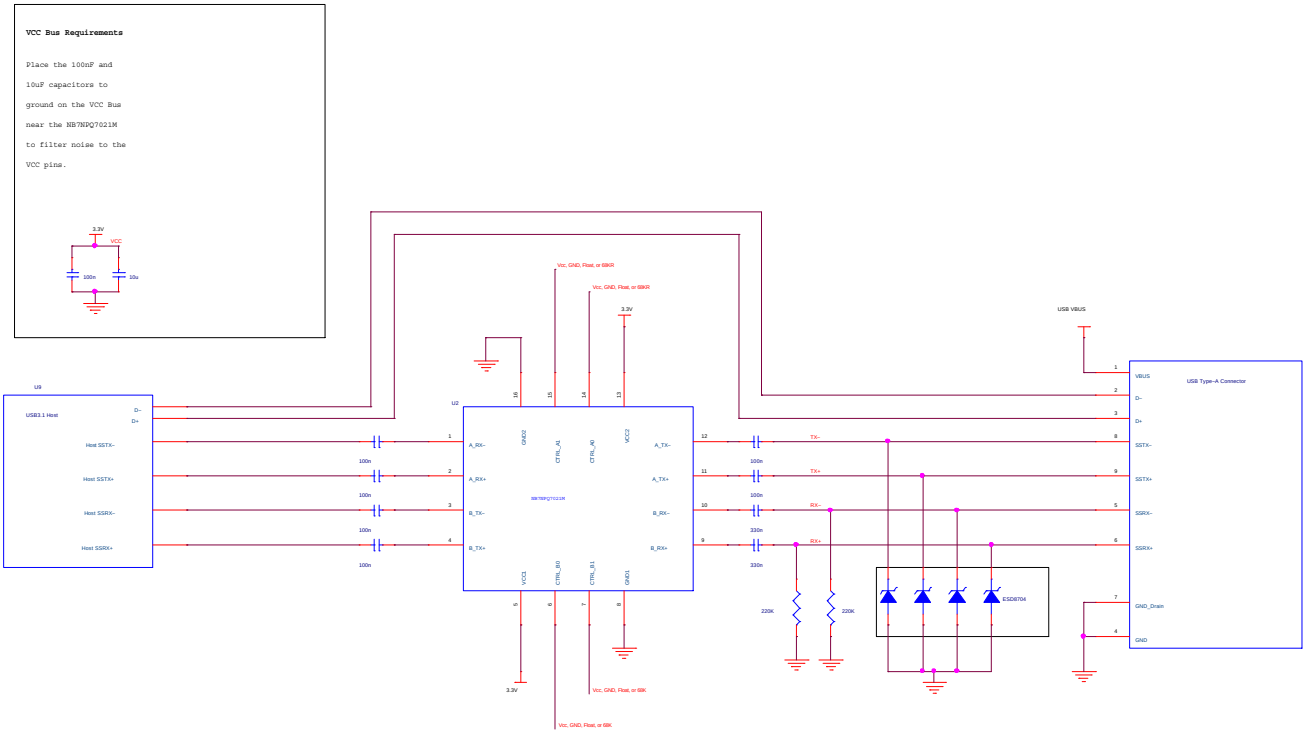
Table 11. DESIGN REQUIREMENTS

Design Parameter	Value
Supply Voltage	3.3 V nominal, (3.135 V to 3.465 V)
Operation Mode (Control Pin Selection)	Floating by Default, adjust for application losses See Table 2
AC Coupling Capacitors	100 nF nominal, 75 nF to 265 nF, see Figure 5
$R_{external}$	68 kΩ, ±10%
RX Pull Down Resistors at Receptacle	200 KΩ to 220 KΩ
Power Supply Capacitors	100 nF to GND close to each Vcc pin, and 10 μF to GND on the Vcc plane
Trace loss of FR4 before NB7NPQ7021M	Up to 11 inches
Trace loss of FR4 after NB7NPQ7021M	Up To 3 inches. Keep as short as possible for best performance.
Linear Range at 5GHz	900 mV differential
DC Flat Gain Options	−1 dB, 0 dB, 2 dB
Equalization Options	3 to 11 dB
Differential Trace Impedance	90 Ω ±10%

9. Trace loss of FR4 was estimated to have 1 dB of loss per 1 inch of FR4 length with matched impedance and no VIAS.

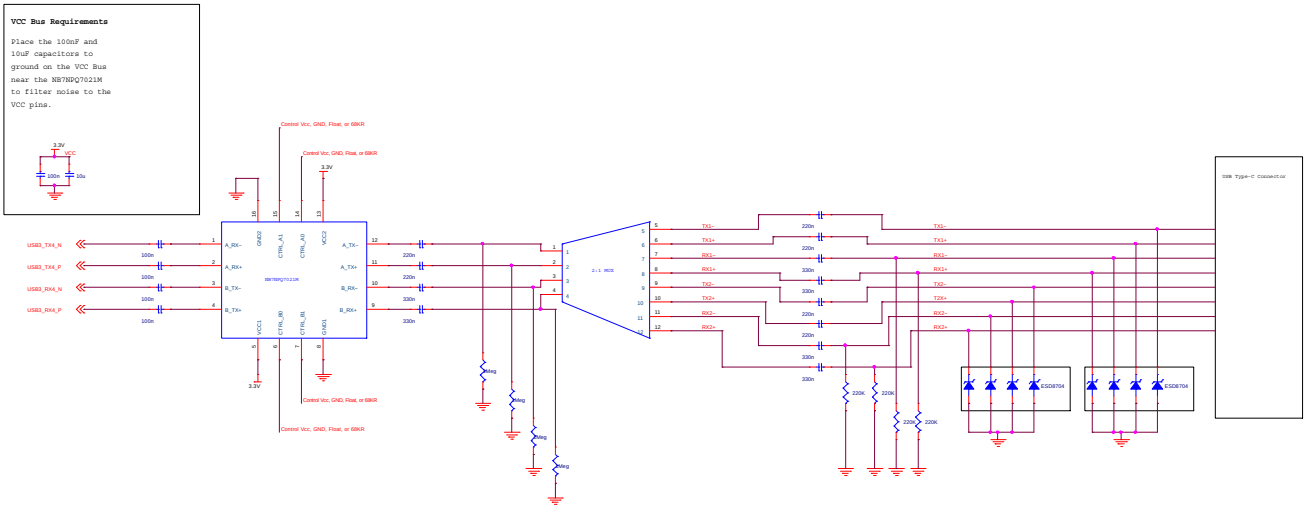
Typical Layout Practices

- RX and TX pairs should maintain as close to a 90 Ω differential impedance as possible.
- Limit the number of vias used on each data line. It is suggested that 2 or fewer are used.
- Traces should be routed as straight and symmetric as possible.
- RX and TX differential pairs should always be placed and routed on the same layer directly above a ground plane. This will help reduce EMI and noise on the data lines.
- Routing angles should be obtuse angles and kept to 135 degrees or larger.
- To minimize crosstalk, TX and RX data lines should be kept away from other high speed signals.



RX coupling capacitors are suggested to remain 330 nF or higher. In some cases; such as when the NB7NPQ7021M is utilized with a multiplexer, a higher capacitor value may be necessary.

Figure 6. Typical Application Diagram for Implementing a USB 3.1 Type−A Port



Note: For the best performance it is recommended to place two redrivers after the multiplexer. Only the most commonly used implementation can be seen in Figure 7.

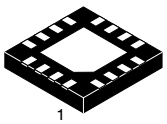
Figure 7. Typical Application Diagram for Implementing a USB 3.1 Type−C Port

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

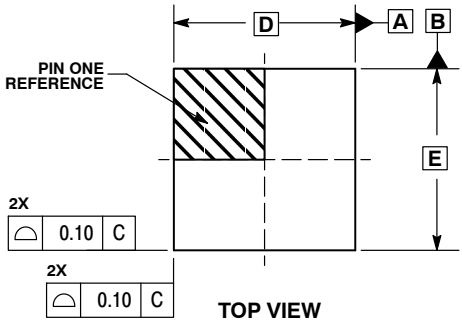
ON Semiconductor®

UQFN16 3x3, 0.5P
CASE 523AF
ISSUE B

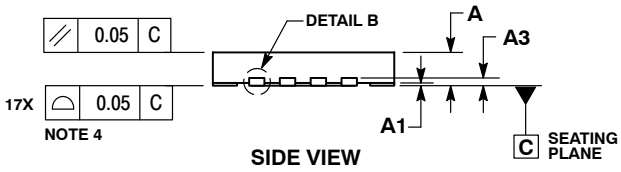
DATE 04 NOV 2015



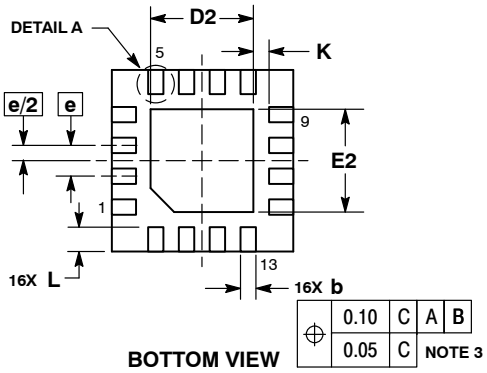
SCALE 4:1



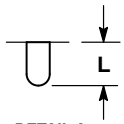
TOP VIEW



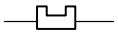
SIDE VIEW



BOTTOM VIEW



DETAIL A
OPTIONAL CONSTRUCTION
2X SCALE



DETAIL B
OPTIONAL CONSTRUCTION
4X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

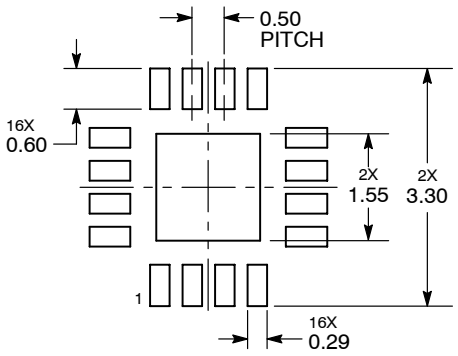
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UQFN16, 3X3, 0.5P	PAGE 1 OF 1

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