# L9758

## Automotive multiple supply for engine control

**PowerSO-36**

*GADG1808161316PS*

## Features

- AEC-Q100 qualified

- Buck converter pre-regulated supply rated for a minimum of 2 A (RMS)

- Optional Boost converter for low battery conditions

- 5 V, 2% @ 1 A, $V_{DD5}$ low dropout (LDO) regulator

- Programmable 3.3 V or 2.6 V, 2% @ 1 A, $V_{DDL}$ LDO regulator with external pass transistor

- Programmable microcontroller core voltage LDO regulator, $V_{CORE}$ 2% @ 1 A with external voltage divider and pass transistor
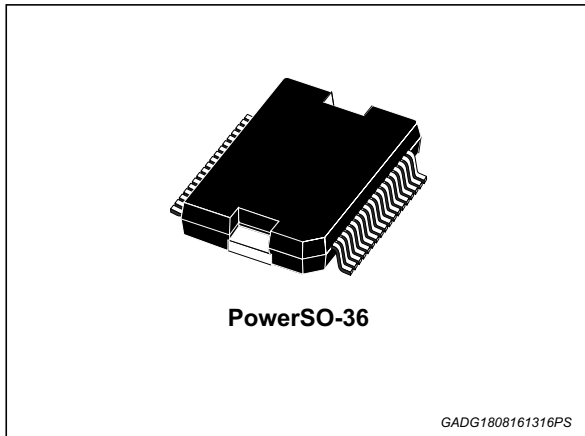
- Programmable 1 V or 1.5 V, 10% @ 10 mA, standby memory regulator ($V_{KAM}$)

- Programmable 3.3 V or 2.6 V, 10% @ 10 mA alternate standby regulator (VSTBY)

- Four 5 V ± 7 mV @ 50 mA protected tracking regulators, one of them with selectable external voltage reference.

- Independent reset signals, RST5 and RSTL for the $V_{DD5}$, $V_{DDL}$ supplies.

- Independent standby voltage monitor STANDBY_OK

- Two power supply enable signals for different voltage level signals

- Battery voltage thresholding - IGN

- Logic level thresholding - PSU_EN

## Description

The L9758 is a multiple output voltage regulator utilizing linear, switchmode (buck and boost) and tracking regulators to support high end automotive microcontrollers used in powertrain applications.

The L9758 provides two standby power regulators as well as controllable LDO regulators.

The L9758 has power on reset functionality and controlled slew rate of the $V_{DD5}$, $V_{DDL}$ and $V_{CORE}$.

**Table 1. Device summary**

| Order code | Temperature range | Package | Packing |
|------------|-------------------|---------|---------|
| L9758 | -40 °C to +125 °C | PowerSO-36 | Tube |
| E-L9758BBTR | | | Tape & Reel |

This is information on a product in full production.     *www.st.com*

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# 1 Pins configuration

**Figure 1. Pins connection (top view)**



*GADG1808161450PS*
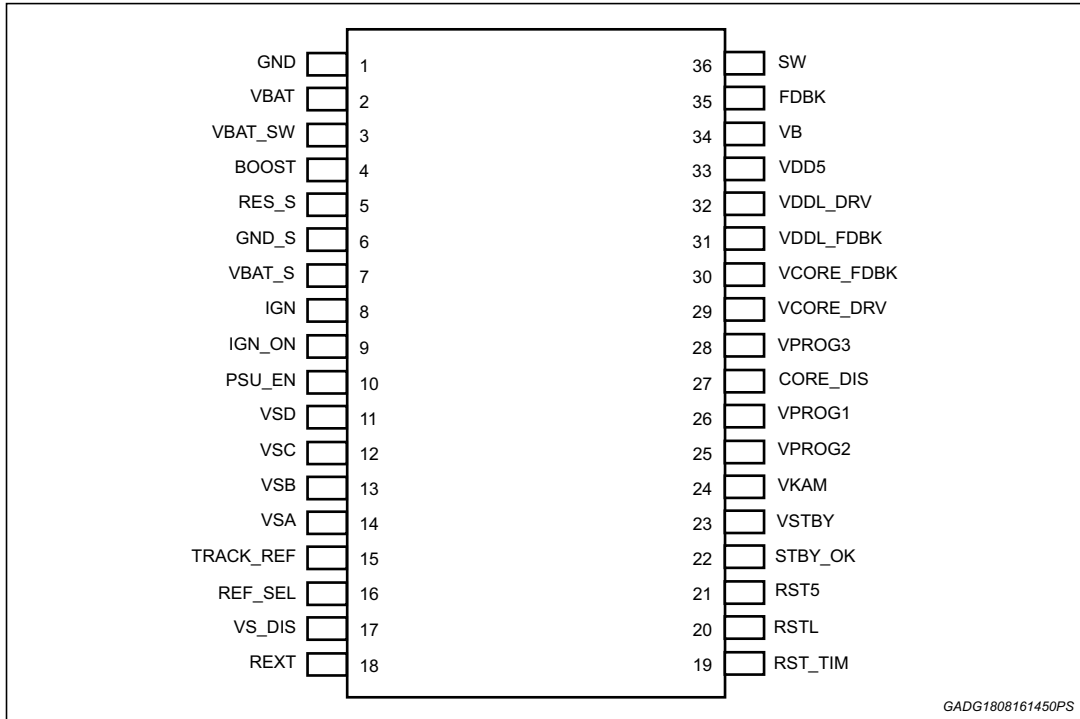
**Table 2. Pins description**

| Pin # | Name | Description |
|-------|------|-------------|
| 1 | GND | Power ground |
| 2 | VBAT | Battery power source |
| 3 | VBAT_SW | Switched battery power source |
| 4 | BOOST | External boost transistor predriver output |
| 5 | RES_S | Boost (+) current comparator input |
| 6 | GND_S | Boost (-) current comparator input |
| 7 | VBAT_S | Battery feedback for boost controller |
| 8 | IGN | Ignition switch |
| 9 | IGN_ON | Ignition state |
| 10 | PSU_EN | Power supply enable |
| 11 | VSD | Tracking regulator D |
| 12 | VSC | Tracking regulator C |
| 13 | VSB | Tracking regulator B |
| 14 | VSA | Tracking regulator A |
| 15 | TRACK_REF | Tracking A voltage reference |

**Table 2. Pins description (continued)**

| Pin # | Name | Description |
|-------|------|-------------|
| 16 | REF_SEL | Tracking A voltage reference selection |
| 17 | VS_DIS | Sensor supply disable |
| 18 | REXT | External current reference resistance |
| 19 | RST_TIM | Reset timer adjustment |
| 20 | RSTL | VDDL regulator reset output |
| 21 | RST5 | VDD5 regulator reset output |
| 22 | STBY_OK | Standby regulator monitor |
| 23 | VSTBY | Standby regulator output |
| 24 | VKAM | Standby memory regulator output |
| 25 | VPROG2 | Standby regulator voltage selection (VSTBY) |
| 26 | VPROG1 | Standby memory regulator voltage selection (VKAM) |
| 27 | CORE_DIS | VDDL and VCORE disable |
| 28 | VPROG3 | VDDL voltage selection |
| 29 | VCORE_DRV | VCORE external pass transistor predriver output |
| 30 | VCORE_FDBK | VCORE feedback |
| 31 | VDDL_FDBK | VDDL feedback |
| 32 | VDDL_DRV | VDDL external pass transistor predriver output |
| 33 | VDD5 | VDD5 linear regulator output |
| 34 | VB | Switching preregulator output |
| 35 | FDBK | Switching voltage feedback |
| 36 | SW | Buck regulator switch output |

**Table 3. Control pins description**

| Pin name | Logic level | Description | Type of I/O |
|----------|-------------|-------------|-------------|
| IGN | Low | Enter in Stand-by Mode if also PSU_EN is low | Pull down |
|     | High | Enter in Run Mode | |
| IGN_ON | Low | IGN is high | Open drain |
|        | High | IGN is low | |
| PSU_EN | Low | Enter in Stand-by Mode if also IGN is low | Pull down |
|        | High | Enter in Run Mode | |
| VS_DIS | Low | Enable VSB, VSC, VSD tracking regulators | Pull down |
|        | High | Disable VSB, VSC, VSD tracking regulators | |

**Table 3. Control pins description (continued)**

| Pin name | Logic level | Description | Type of I/O |
|---|---|---|---|
| Ref_Sel | Low | Voltage reference for VSA tracking regulator is VDD5 | Pull down |
| | High | Voltage reference for VSA tracking regulator is VTRACK_REF | |
| RSTL | Low | VDDL output regulator out of range (under voltage) | Open collector |
| | High | VDDL output regulator fully operational | |
| RST5 | Low | VDD5 output regulator out of range (under voltage) | Open collector |
| | High | VDD5 output regulator fully operational | |
| VPROG1 | Low | VKAM regulator output programmed to 1V | Pull up |
| | High | VKAM regulator output programmed to 1.5V | |
| VPROG2 | Low | VSTBY regulator output programmed to 2.6V | Pull up |
| | High | VSTBY regulator output programmed to 3.3V | |
| VPROG3 | Low | VDLL regulator output programmed to 2.6V | Pull up |
| | High | VDLL regulator output programmed to 3.3V | |
| CORE_DIS | Low | Enable VDLL and VCORE linear regulators | Pull down |
| | High | Disable VDLL and VCORE linear regulators | |
| STBY_OK | Low | VSTBY output regulator out of range (under voltage) | Open drain |
| | High | VSTBY output regulator fully operational | |

# 2 Functional block diagram

**Figure 2. Functional block diagram**



*GADG1808161452PS*
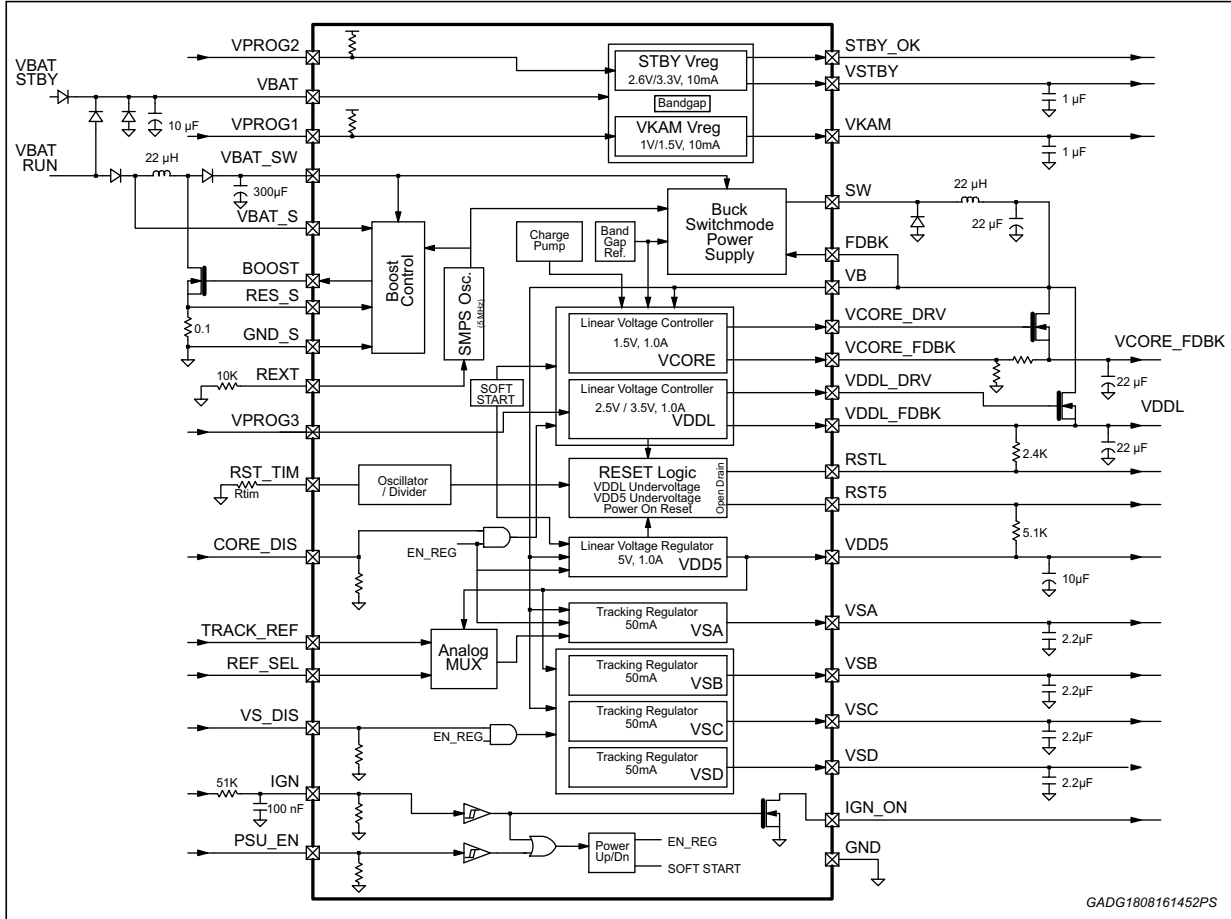
# 3 Operating conditions

## 3.1 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{BAT}$, $V_{BAT\_SW}$, $V_{BAT\_S}$ | Battery supply voltage | -0.3 to 40 | V |
| $V_{IGN}$ | Ignition input voltage (with at least 10K external resistance) | -2.0 to 40 | V |
| $V_{I\text{-}digital}$ | Digital input voltages (PSU_EN, VS_EN, VPROG1, VPROG2, VPROG3, VDDL/VCORE_EN, REF_SEL) | -0.3 to 7 | V |
| $V_{I\text{-}analog}$ | Analog input voltages (REXT, TRACK_REF, RST_TIM VDDL_FDBK, VCORE_FDBK) | -0.3 to 7 | V |
| $V_B$ | Linear regulator supply (VB) | -0.3 to 40 | V |
| $V_{FDBK}$ | Switching feedback (FDBK) | -0.3 to 40 | V |
| $V_{SW}$ | Buck regulator switch output (SW) | -2 to 40 | V |
| $V_{O\text{-}digital}$ | Digital output voltages (IGN_ON, RSTL, RST5, BOOST, STBY_OK) | -0.3 to 7 | V |
| $V_{OR}$ | Regulator output voltages (VDD5, VSTBY, VKAM) | -0.3 to 7 | V |
| $V_{VSx}$ | Regulator output voltages (VSA, VSB, VSC, VSD) | -3 to 40 | V |
| $V_{CORE\_DRV}$, $V_{DDL\_DRV}$ | External regulator predriver output (VCORE_DRV, VDDL_DRV) | -0.3 to 15 | V |
| $I_{SMPS}$ | Switching preregulator current | 0 to 4.2 | A |
| $T_{op}$ | Operating temperature | -40 to 125 | °C |
| $T_{stg}$ | Storage temperature | -50 to 150 | °C |
| $T_j$ | Max junction temperature | 150 | °C |
| $V_{ESD}$ | Max ESD (human body model) | ±2 | KV |

**Warning:**     **Exceeding these values might destroy this part. This part is not guaranteed to function properly at these ratings. The CMOS inputs and outputs should never go above 5 V + 0.3 V or below GND - 0.3 V without protection (series resistance). If this occurs, the device might be destroyed by latch-up and/or the output levels might not be controlled by the inputs. Unused inputs must be connected to GND and unused outputs should be left open and programmed to a low state. Unused I/O pins should be programmed as outputs, left open, and programmed to a low state.**

## 3.2 Operating ranges

Full specification parameters cannot be guaranteed outside the operating ranges. Once the condition has returned within the specified operating ranges, the part will recover with no damage or degradation.

**Table 5. Operating ranges**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{BAT}$, $V_{BAT\_SW}$, $V_{BAT\_S}$ | Battery supply voltage | 4 to 26.5 | V |
| | | 4 to 40 (t < 400 ms) | |
| $V_{IGN}$ | Ignition input voltage (with at least 10K external resistance) | 4 to 26.5 | V |
| $V_{I-digital}$ | Digital input voltages (PSU_EN,VS_EN,VPROG1, VPROG2, VPROG3, VDDL/VCORE_EN, REF_SEL) | -0.3 to 5.3 | V |
| $V_{I-analog}$ | Analog input voltages (REXT, TRACK_REF, RST_TIM VDDL_FDBK, VCORE_FDBK) | -0.3 to 5.3 | V |
| $I_{AVE}$ | Switching preregulator average current | 0 to 2.5 | A |
| $T_{op}$ | Operating temperature | -40 to 125 | °C |
| $T_j$ | Junction temperature | -40 to 150 | °C |

## 3.3 Thermal data

**Table 6. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(j-case)}$ | Thermal resistance junction-to-case | 2 | °C/W |

# 4 Electrical characteristics

All voltage values are, if not otherwise stated, relative to ground.Current flow into a pin is positive. If not otherwise stated, all rise times are between 10% and 90%, fall times between 90% and 10% and delay times at 50% of the relevant steps.

## 4.1 General DC characteristics

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 7. General DC characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{BAT\_SW\_SB}$ | Quiescent current at pin BAT_SW | $V_{BAT}$ = 0 V; $V_{BAT\_SW}$ = 12 V | - | - | 150 | µA |
| $I_{Q\_OFF}$ | Supply current in OFF state | $I_{VBAT\_SW}$ + $I_{VBAT}$ | - | - | 120 | µA |
| $V_{LVI\_LOW}$ | Low voltage inhibit Low threshold | - | 3.5 | - | 3.9 | V |
| $V_{LVI\_HIGH}$ | Low voltage inhibit High threshold | - | 4.0 | - | 4.5 | V |
| $V_{LVI\_HYS}$ | Low voltage inhibit hysteresis | - | 0.3 | - | 1 | V |
| $V_{ST}$ | Linear Start-up voltage | - | 3.8 | - | 4.8 | V |
| $V_{REXT}$ | Rext Voltage | - | 1.18 | - | 1.24 | V |
| $V_{TH\_VSEN}$ | VS_EN input threshold | - | 0.8 | - | 2 | V |
| $V_{VDDL/VCORE\_EN}$ | VDDL/VCORE_EN input threshold | - | 0.8 | - | 2 | V |
| $V_{PROG1\_LOW}$ | PROG1 input Low Voltage | - | - | - | 0.8 | V |
| $V_{PROG2\_LOW}$ | PROG2 input Low Voltage | - | - | - | 0.8 | V |
| $V_{PROG3\_LOW}$ | PROG3 input Low Voltage | - | - | - | 0.8 | V |
| $V_{DDL\_ENUP}$ | Vddl Power-up enable | - | 1 | - | 2 | V |

## 4.2 BUCK pre-regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V; unless otherwise specified.

**Table 8. BUCK pre-regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $F_{SW}$ | Operating frequency | $R_{ext}$ = 10.0 kΩ ±1% <br> $V_{BAT\_SW}$ = 13.5 V | 300 | - | 450 | kHz |
| $R_{dsON}$ | High side switch ON resistance | $V_{BAT\_SW}$ = 6.0 V | - | - | 0.25 | Ω |
| $I_{ST\_MAX}$ | Average current during start-up | $V_B$ = 3.0V | 0.3 | - | 0.7 | A |
| $V_{BREG}$ | Output voltage | 7.0 V < $V_{BAT\_SW}$ < 18 V <br> 0.25 A < $I_{VBAT}$ <2.0 A | 5.5 | - | 6.1 | V |
| Vb100 | 100% Duty Cycle operation threshold | Voltage sensed at VBAT_SW pin | 6.2 | - | 7.8 | V |
| Vb100h | 100% Duty Cycle operation threshold hysteresis | | 0.05 | - | 0.8 | V |
| ΔVpre | Load regulation | $\Delta I_{VB}$ = 0.1 A –2 A $V_{BAT\_SW}$ = 13.5 V | - | - | 400 | mV |
| Vrpre | Voltage ripple, p-p | L = 22 µH, C = 22 µF X7R <br> $V_{BAT\_SW}$ = 13.5 V | - | - | 300 | mV |
| Ts | Start time | L = 22 µH, C = 22 µF X7R | - | - | 1.4 | ms |
| DCmin | Minimum duty cycle | - | 10 | - | 18 | % |
| EFF | Efficiency | $V_{BAT\_SW}$ = 13.5 V $I_{VB}$ = 0.5 A <br> $V_{BAT\_SW}$ = 13.5 V $I_{VB}$ = 2 A | 70 <br> 70 | - | - | % |
| L <br> Rs | Output Inductance | - | 15 | 22 | 30 <br> 75 | µH <br> mΩ |
| C <br> ESR | Output capacitance | - | 10 <br> 0 | - | 100 <br> 160 | µF <br> mΩ |
| Ov | Power-up overvoltage | $V_{BAT\_SW}$ < 26.5 V <br> 0.25 A < $I_{VBAT}$ <2.0 A | 15 | - | 200 | mV |
| Tr_sw <br> Tf_sw | SW rising and falling time | 7.0 V < $V_{BAT\_SW}$ < 18 V <br> $I_{VBAT}$ <2.0 A (20%, 80%) | 10 | - | 150 | µs |

## 4.3      Boost pre-regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 9. Boost pre-regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| FSW | Operating frequency | $R_{ext}$ = 10.0 kΩ ±1%<br>$V_{BAT\_SW}$ = 13.5 V | 300 | - | 450 | kHz |
| $V_{B\_REG}$ | Output voltage | 4.0 V < $V_{BAT\_S}$ < 7 V, 0.25 A < $I_{VB}$ < 2.0 A | 8.5 | - | 10 | V |
| BoostONth | Boost enable threshold | Voltage sensed at VBAT_S pin | 7.0 | - | 8.3 | V |
| BoostOFFth | Boost disable threshold | | 7.0 | - | 8.3 | V |
| $V_{BOOST\_HY}$ | Boost operation threshold hysteresis | Voltage sensed at VBAT_S pin | 0.05 | - | 0.9 | V |
| $\Delta V_{BOOST}$ | Load regulation | $\Delta I_{VB}$ = 0.1 A–2 A $V_{BAT\_S}$ = 4 V | - | - | 600 | mV |
| $V_{R\_VBOOST}$ | Voltage ripple, p-p | L = 22 µH, C = 300 µF X7RX7R<br>$V_{BAT\_S}$ = 4 V | - | - | 600 | mV |
| $V_{OLB}$ | Boost predriver low level voltage | $I_{sink}$ = 1 mA | - | - | 0.2 | V |
| $V_{OHB}$ | Boost predriver low level voltage | $I_{source}$ = 200 µA | 4.8 | - | - | V |
| $T_{RB}$ | Boost predriver rise time | CI = 1 nF | 50 | - | 180 | ns |
| $T_{FB}$ | Boost predriver fall time | CI = 1 nF | 20 | - | 100 | ns |
| L<br>Rs | Output inductance | - | 15 | 22 | 30<br>75 | µH<br>mΩ |
| C<br>ESR | Output capacitance | - | 100<br>10 | 300 | 900<br>200 | µF<br>mΩ |
| $R_{SENSE}$ | Sensing resistor | - | 40 | 50 | - | mΩ |

## 4.4 VDD5 linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 10. VDD5 linear regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD5}$ | Output voltage | 5 mA < $I_{DD5}$ < 1 A $V_{BAT\_SW}$ => 5.7 V 5 mA < $I_{DD5}$ < 800 mA $V_{BAT\_SW}$ = 5.5 V | 4.9 | - | 5.1 | V |
| | | 5 mA < $I_{DD5}$ < 1 A $V_{BAT\_SW}$ ≥ 4 V | 3.3 | | 4.0 | |
| $I_{DD5\_LIM}$ | Current limit | $V_{DD5}$ = 4.75 V | 1200 | - | 2500 | mA |
| $C_{DD5}$ ESR | Output capacitor | Ceramic or Tantalum C = 4.7 µF | 4.70 | - | 100 160 | µF mΩ |
| $R_{RDD5}$ | Ripple rejection | F = 375 kHz | 26 | - | - | dB |
| $V_{DD5\_MAX}$ | Maximum overshoot | ΔVB/Δt < 70 V/ms $V_{BAT\_SW}$ = 4V → 8 V | - | - | 5.5 | V |
| $\Delta V_{DD5}/\Delta t$ | Output voltage slew rate at power-up | 5 mA < $I_{DD5}$ < 1 A $V_{BAT\_SW}$ = 13.5 V | 10 | - | 20 | V/ms |
| $I_{DD5}$ | Load current | - | 5 | - | 1000 | mA |
| $V_{DD5}$lineR | Line regulation | 6.0 V < $V_B$ < 7 V | -25 | - | +25 | mV |
| $V_{DD5}$loadR | Load regulation | 5 mA < $I_{DD5}$ < 1 A | -25 | - | +25 | mV |
| $V_{DD5}$-$V_{ddl}$ | Start up | $V_{DD5}$-$V_{ddl}$ during start up | 0.5 | - | 3.1 | mV |

## 4.5 VDDL linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$= $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 11. VDDL linear regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDL}$ | Output voltage | 5 mA < $I_{DDL}$ < 1 A, $V_{PROG3}$ = Open 4.0 V < $V_{BAT\_SW}$ < 18 V | 3.23 | - | 3.37 | V |
| | | 5 mA <$I_{DDL}$ < 1 A, $V_{PROG3}$ = Low 4.0 V < $V_{BAT\_SW}$ < 18 V | 2.55 | | 2.65 | |
| $C_{DDL}$ ESR | Output capacitor | Ceramic or Tantalum | 4.70 | - | 100 160 | µF mΩ |
| $RR_{DDL}$ | Ripple rejection | F = 375 kHz | 26 | - | - | dB |

**Table 11. VDDL linear regulator  (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $V_{DDL\_MAX}$ | Maximum overshoot | 5 mA $<I_{DDL}$ < 1 A, $V_{PROG3}$ = Open<br>4.0 V < $V_{BAT\_SW}$ < 18 V<br>$\Delta VB/\Delta t$ < 70 V/ms<br><br>5 mA < $I_{DDL}$ < 1 A, $V_{PROG3}$ = Low<br>4.0 V < $V_{BAT\_SW}$ < 18 V<br>$\Delta VB/\Delta t$ < 70 V/ms | - | - | 3.75<br><br>3.6 | V |
| $\Delta V_{DDL}/\Delta t$ | Output voltage slew rate at power-up | 5 mA $<I_{DDL}$ < 1 A $V_{BAT\_SW}$ =13.5 V | 5 | - | 25 | V/ms |
| $I_{DDL}$ | Load current | - | 5 | - | 1000 | mA |
| $V_{DDL}$lineR | Line regulation | 5.5 V < $V_{BAT\_SW}$ < 7 V | -8 | - | +8 | mV |
| $V_{DDL}$loadR | Load regulation | 5 mA < $I_{DDL}$< 1 A | -8 | - | +8 | mV |

## 4.6      VCORE linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$= $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 12. VCORE linear regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $V_{CORE}$ | Output voltage | 5 mA < $I_{CORE}$ < 1 A;<br>4.0 V < $V_{BAT\_SW}$ < 18 V | 1.47 | - | 1.53 | V |
| CddL<br>ESR | Output capacitor | Ceramic or Tantalum | 4.700 | - | 100<br>160 | µF<br>mΩ |
| RRddL | Ripple rejection | F= 375 kHz | 26 | - | - | dB |
| $V_{CORE\_M}$ | Maximum overshoot | 5 mA < $I_{CORE}$ < 1 A<br>4.0 V < $V_{BAT\_SW}$ < 18 V | - | - | 1.7 | V |
| $\Delta V_{CORE}/\Delta t$ | Output voltage slew rate at power-up | 5 mA < $I_{CORE}$ < 1 A $V_{BAT\_SW}$=13.5 V | 5 | - | 25 | V/ms |
| $I_{CORE}$ | Load current | - | 5 | - | 1000 | mA |
| $V_{CORE\_PROG}$ | Range of programmability | Using external resistor divider | 1.05 | 1.5 | 2.8 | V |
| $V_{CORE\_FBK}$ | Feedback voltage | - | 0.98 | - | 1.02 | V |
| $V_{CORE}$lineR | Line regulation | 5.5 V < $V_{BAT\_SW}$ < 7 V | -25 | - | +25 | mV |
| $V_{CORE}$loadR | Load regulation | 5 mA < $I_{CORE}$ < 1 A | -25 | - | +25 | mV |

## 4.7 VKAM linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 13. VKAM linear regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{KAM}$ | Output voltage | 0.1mA < $I_{VKAM}$ < 10mA, $V_{PROG1}$ = Low 4.0V < $V_{BAT}$ < 18V | 0.9 | - | 1.1 | V |
| | | 0.1mA < $I_{VKAM}$ < 10mA, $V_{PROG1}$ =Open 4.0V < $V_{BAT}$< 18V | 1.37 | | 1.65 | |
| $C_{VKAM}$ ESR | Output capacitor | Ceramic | 0.10 | - | 4.7 20 | µF mΩ |
| $RR_{VKAM}$ | Ripple rejection | F=375 kHz | 26 | - | | dB |
| $V_{KAM\_M}$ | Maximum overshoot (absolute value relative to GND) | 0.1 mA < $I_{VKAM}$ < 10 mA, $V_{PROG1}$ = Low 4 V < $V_{BAT}$ < 18 V | - | - | 1.2 | V |
| | | 0.1 mA < $I_{VKAM}$ < 10 mA, $V_{PROG1}$ = Open 4 V < $V_{BAT}$< 18 V | | | 1.7 | |
| Iddkamsh | Current limit | $V_{KAM}$ = 0.5 V | 11 | - | 50 | mA |
| $I_{KAM}$ | Load current | - | 0.1 | - | 10 | mA |
| $V_{KAM}$lineR | Line regulation | 6 V < $V_{BAT}$ < 18 V | -25 | - | +25 | mV |
| $V_{KAM}$loadR | Load regulation | 0.1 mA < $I_{KAM}$ < 10 mA | -25 | - | +25 | mV |

## 4.8 VSTBY linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 14. VSTBY linear regulator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{STBY}$ | Output voltage | 0.1 mA < $I_{STBY}$ < 10 mA, $V_{PROG2}$ = Low 4 V < $V_{BAT}$< 18 V | 2.47 | - | 2.73 | V |
| | | 0.1 mA < $I_{STBY}$ < 10 mA, $V_{PROG2}$ = Open 4 V < $V_{BAT}$< 18 V | 3.13 | | 3.47 | |
| $C_{STBY}$ ESR | Output capacitor | Ceramic | 0.10 | - | 10 20 | µF mΩ |
| $RR_{STBY}$ | Ripple rejection | F = 350 kHz | 26 | - | - | dB |
| $V_{STBY\_M}$ | Maximum overshoot (absolute value relative to GND) | 0.1 mA < $I_{STBY}$ < 10 mA, $V_{PROG2}$ = Low 4 V < $V_{BAT}$< 18 V | - | - | 3.05 | V |
| | | 0.1 mA < $I_{STBY}$ < 10 mA, $V_{PROG2}$ = Open 4 V < $V_{BAT}$< 18 V | | | 3.75 | |
| $I_{STBY}$sh | Current limit | $V_{STBY}$ = 0.5 V | 11 | - | 50 | mA |
| $I_{STBY}$ | Load current | - | 0.1 | - | 10 | mA |
| $V_{STBY}$lineR | Line regulation | 6 V < $V_{BAT}$ <18 V | -25 | - | +25 | mV |
| $V_{STBY}$loadR | Load regulation | 0.1 mA < $I_{STBY}$ < 10 mA | -25 | - | +25 | mV |

## 4.9 VSA, VSB, VSC, VSD tracking linear regulator

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$= $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

### Table 15. VSA, VSB, VSC, VSD tracking linear regulator

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{TRK}$ | Output voltage tracking accuracy | 1 mA < $I_{t1}$ < 50 mA, 6 V < $V_{BAT\_SW}$ < 18 V<br>1 mA < $I_{t1}$ < 5 0mA, 4 V < $V_{BAT\_SW}$ < 6 V | -7<br>-50 | - | 10<br>50 | mV |
| $I_{TRK}$sh | Current limit | $V_{tck}$ = 4.75 V | 51 | - | 100 | mA |
| $C_{TRK}$<br>ESR | Output load capacitor | Ceramic or Tantalum | 1<br>0 | - | 16<br>3 | µF<br>mΩ |
| Ctckmin<br>ESRmin | Minimum output capacitor for stability | Ceramic or Tantalum | 1<br>0 | - | <br>3 | µF<br>Ω |
| $RR_{TRK}$ | Ripple rejection | F= 375 kHz | 26 | - | - | dB |
| Vdrop | Dropout voltage | $I_{load}$ = 50 mA | - | - | 300 | mV |
| $T_{TSD}$ | Thermal shutdown | Vtck = 4.75 V (current limitation) | 165 | - | 185 | °C |
| $T_{HYST}$ | Thermal hysteresis | Vtck = 4.75 V (current limitation) | 5 | - | 15 | °C |
| $I_{TRK}$ | Load current | - | 1 | - | 50 | mA |

## 4.10 RST5 and RSTL reset signals

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

### Table 16. RST5 reset signals

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{RST5\_H}$ | Reset "high" leakage current | $V_{RST5}$ = 5.15 V | -3.0 | - | - | µA |
| $V_{RST5\_L}$ | Reset "low" output voltage | $V_{DD5}$ = 4.5 V Ire = 5 mA<br>$V_{DD5}$ = 1.0 V Ire = 1 mA | -<br> | -<br> | 0.4<br>0.4 | V |
| $V_{FTH\_RST5}$ | Reset threshold decreasing | $\Delta V_{DD5}/\Delta t$ < 0 | 4.5 | - | $V_{DD5}$–0.2 | V |
| $V_{RTH\_RST5}$ | Reset threshold increasing | $\Delta V_{DD5}/\Delta t$ > 0 | 4.5 | - | $V_{DD5}$–0.07 | V |
| $V_{HY\_RST5}$ | Reset threshold hysteresis | - | 50 | - | - | mV |
| $t_{ACT\_RST5}$ | Reset activation out of tolerance duration | - | 15 | - | 25 | µs |
| $t_{DEL\_RST5}$ | Reset delay | 4.7 kΩ < $R_{ext}$ < 47 kΩ | 1 | - | 10 | ms |
| $t_{ERR\_RST5}$ | Reset delay accuracy | $R_{ext}$ ±1% | -15 | - | +15 | % |

**Table 17. RSTL reset signals**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $I_{RSTL\_H}$ | Reset "high" leakage current | $V_{DDL}$= 5.15 V | -3.0 | - | - | µA |
| $V_{RSTL\_L}$ | Reset "low" output voltage | $V_{DDL}$=5.0V Ire=5mA<br>$V_{DDL}$=1.0V Ire=1mA | -<br> | -<br> | 0.4<br>0.4 | V |
| $V_{FTH\_RSTL}$ | Reset threshold decreasing | $\Delta V_{DDL}/\Delta t < 0$, $V_{PROG3}$=Low | 2.375 | - | $V_{DDL}$−0.05 | V |
| $V_{RTH\_RSTL}$ | Reset threshold increasing | $\Delta V_{DDL}/\Delta t < 0$, $V_{PROG3}$=Low | 2.375 | - | $V_{DDL}$−0.02 | V |
| $V_{FTH\_RSTL\_O}$ | Reset threshold decreasing | $\Delta V_{DDL}/\Delta t < 0$, $V_{PROG3}$=Open | 3.13 | - | $V_{DDL}$−0.05 | V |
| $V_{RTH\_RSTL\_O}$ | Reset threshold increasing | $\Delta V_{DDL}/\Delta t < 0$, $V_{PROG3}$=Open | 3.13 | - | $V_{DDL}$−0.02 | V |
| $V_{HY\_RSTL}$ | Reset threshold hysteresis | - | 40 | - | - | mV |
| $t_{ACT\_RSTL}$ | Reset activation out of tolerance duration | - | 15 | - | 25 | µs |
| $t_{DEL\_RSTL}$ | Reset delay | 1nF < $C_{EXT}$< 10nF; 4.7kΩ < $R_{ext}$ < 47kΩ | 1 | - | 10 | ms |
| $t_{ERR\_RSTL}$ | Reset delay accuracy | $R_{ext}$ ±1% | -15 | - | +15 | % |

## 4.11   IGN and PSU_EN inputs

$T_{amb}$ = -40 °C to 125 °C, $V_{BAT}$ = $V_{BAT\_SW}$ = 5.5 to 26.5 V, unless otherwise specified.

**Table 18. IGN and PSU_EN inputs**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $V_{TH\_IGN}$ | IGN input threshold | threshold @ IGN pin | 2 | - | 3.6 | V |
| $V_{HYS\_IGN}$ | IGN input threshold hysteresis | - | 0.2 | - | 1.4 | V |
| $R_{PD\_IGN}$ | IGN pull-down resistor | - | 300 | - | 1100 | kΩ |
| $V_{TH\_PSUEN}$ | PSU_EN input threshold | - | 0.9 | - | 0.55*$V_{STBY}$ | V |
| $V_{HYS\_PSUEN}$ | PSU_EN input threshold hysteresis | - | 0.2 | - | 0.8 | V |
| $R_{PD\_PSUEN}$ | PSU pull-down resistor | - | 50 | - | 230 | kΩ |
| $V_{OL\_IGNON}$ | IGN_ON "low" output voltage | Iol=1mA | | | 0.4 | V |
| $R_{IGN\_EXT}$ | IGN external input resistance | | 10 | | 50 | kΩ |

## 4.12 STBY_OK signal

$T_{amb}$ = -40°C to 125°C, $V_{BAT}$= $V_{BAT\_SW}$ = 5.5 to 26.5V, unless otherwise specified.

**Table 19. STBY_OK signal**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{h\_stbyok}$ | VstanbyOK threshold | $\Delta V_{STBY}/\Delta t$ <0 | -8,5 | - | -3,5 | % |
| $T_{stbydly}$ | STBY_OK filter time | - | 15 | - | 25 | µs |
| $T_{stbyok}$ | STBY_OK delay accuracy | - | 10 | - | 60 | µs |
| $V_{ol\_stbyok}$ | STBY_OK low output voltage | $V_{STBY}$ = 1 V $I_{stbyok}$ =1 mA | - | - | 0.4 | V |

# 5 Functional description

## 5.1 General function

The L9758 is equipped with 9 linear voltage regulators. A buck boost switch mode power supply as pre regulator for the 7 main regulators is used to reduce the power consumption in the system.

Two standby regulators can be used to bias the system on off-mode. These two regulators are equipped with an independent bandgap voltage reference. The current consumption of these two linear regulators is specified to be less than 120 µA in OFF state. If these standby functions are not used the current consumption on the battery can be reduced by not connecting the VBAT. Under this condition the device enters immediately in the run mode, the pin PSU_REN looses his function. The quiescent current on the VBAT_SW can be reduced to maximum 10 µA with 12 V battery voltage in off mode. The main regulators can be activated with the IGN input. With an external resistor higher than 10 kΩ in series to the IGN pin a battery compliant signal can be used. In the functional block diagram (see *Figure 2*) a resistor value of 51 kΩ is used together with a 100 nF capacitor for noise robustness on IGN.

## 5.2 Switching pre-regulator

The switching pre-regulator is a buck or a buck-boost current control mode regulator. The optional boost operation for low battery conditions can be selected connecting external logic level low side NCH FET and an external diode in series to the inductor.

The external parts required to complete the switching regulator are an inductor, recirculation diode and input and output filtering capacitor. The compensation network is inside the device.

With a constant switching frequency of 350 kHz, the pre-regulator controls the output voltage (the voltage at the VB and FDBK pins) to the limits stated in the electrical characteristics table varying the duty cycle. The 350 kHz are related to $R_{EXT}$ = 10 kΩ (see *Section 5.8*).

At low battery voltages, in buck configuration, the pre-regulator runs with the duty cycle up to 100%. In buck-boost configuration normally it runs at 350 kHz but for a limited range of input voltage it could enter in pulse skipping mode to control the output voltage.

A soft start function is implemented reducing the current limitation during the power-up phase.

## 5.3 VDD5, VDDL and VCORE linear regulators

The VDD5 output is a fully integrated low drop out regulator. The $V_{DDL}$ and $V_{CORE}$ supplies will be implemented via an external N-channel pass MOS, with the control being internal to the IC. If the pass MOS is not used, two low current (max 30 mA) regulators are available connecting directly VDDL_FDBK to VDDL_DRV and VCORE_FDBK to VCORE_DRV with a resistor divider.The output of the pre-regulator is used as the source of these supplies.

$V_{DD5}$ is a fixed 5 V nominal output, while $V_{DDL}$ and $V_{CORE}$ are programmable.

The $V_{DDL}$ voltage is selectable with the VPROG3 pin: 2.5 V if connected to GND and 3.3 V if left open (an internal pull-up is present). $V_{CORE}$ voltage is programmable connecting an external resistor divider at the feedback pin (VCORE_FDBK).

Once programmed to a value at power-up, this value cannot change during the power cycle. Purposely the system runs at a single fixed value for $V_{DDL}$ and $V_{CORE}$ for the life of the product.

All the linear regulators start with a controlled slew rate when the pre-regulated voltage reaches $V_{DDL\_ENUP}$ threshold as indicated in the electrical characteristics table. All the linear regulators are short circuit protected with a limited current.

## 5.4 Tracking regulators

Four low drop-out tracking regulators (VSA, VSB, VSC and VSD) are supplied by the output of the switching pre-regulator. They track the output voltage of the VDD5 linear regulator with the accuracy as specified in the electrical characteristic table.

The VSA regulator also tracks an external voltage reference (TRACK_REF pin) and the tracking voltage is selected by the REF_SEL pin.

If REF_SEL is tied High (5 V) then $V_{TRK\_REF}$ is tracked. If REF_SEL is left open then $V_{DD5}$ is tracked. There is an internal pull-down on REF_SEL.

The tracking supplies are intended to drive loads that are external to the ECU so they are short circuit protected with the current limited. The outputs of the tracking regulators also withstand short circuit to the battery.

A short circuit to GND, continuous or intermittent on one tracking supply will not affect any other supply, including the preregulator output voltage $V_B$. In addition to these requirements, all sensor supplies shall be capable of operating with up to a 15 µF load on the supply line. This load may be present during initial startup, or be applied after the supply has been powered up. In either case, the application of this load shall not cause the tracking regulators to be permanently disabled.

VSB, VSC and VSD regulators can be disabled with VS_EN pin.

## 5.5 VKAM and VSTBY linear regulators

These two outputs are fully integrated low quiescent current low drop out regulators. The input VBAT is used as the source of these supplies. These outputs are operational during both standby and run mode; these are the only outputs operational during standby ($V_{BAT}$ not present).

The VKAM regulator has two programmable levels: 1.0 V (VPROG1 pin connected to GND) or 1.5 V (if this pin is left open, an internal pull-up is present).

The $V_{STBY}$ regulator has two programmable levels: 2.6 V (VPROG2 pin connected to GND) or 3.3 V (if this pin is left open, an internal pull-up is present).

The STBY_OK pin indicates when the $V_{STBY}$ is out of range (voltage below the threshold indicated in the electrical characteristic table). Once driven low it should stay low for a minimal amount of time allowing external circuitry to latch.

## 5.6 RESET monitors

RST5 is the reset signal tied to the $V_{DD5}$ supply. This is an open collector active low signal that pulls low when $V_{DD5}$ is out of range.

RSTL is the reset signal for the $V_{DDL}$ supply. This is an open collector active low signal that pulls low when $V_{DDL}$ is out of range. RST5 and RSTL are also driven low when STBY_OK pin is driven low, regardless of the status of $V_{DD5}$ and $V_{DDL}$.

Reset Delay is the time duration from when the output ($V_{DD5}$ or $V_{DDL}$) is within range to when the reset pin (RST5 or RSTL) is released. RST5 and RSTL use separate timers. This delay is programmable via an external resistor connected to RST_TIM pin. A value of 4.7 kΩ corresponds to 1 ms and 47 kΩ to 10 ms. All values in between are linear approximated. The timer delay is common however the attack and release times are only dependant on the condition of the respective supplies ($V_{DD5}$ or $V_{DDL}$).

## 5.7 Thermal protection

The tracking regulators incorporate thermal limit with shutdown. When the junction temperature reaches the shutdown threshold, if there is a tracking regulator in current limitation, it switches off and all the other regulators stay on. When the temperature decreases the regulator restarts. The over temperature shutdown has a hysteresis to avoid thermal pumping.

## 5.8 Reference current

The L9758 provides a DC voltage at the REXT pin. An external resistor to ground creates a reference current which is mirrored internally for use in the device.

The reference current is used to supply all the analog blocks and to charge and discharge an integrated capacitor to generate a 5 MHz clock for the switching functionality.

**Figure 3. Current reference generator**
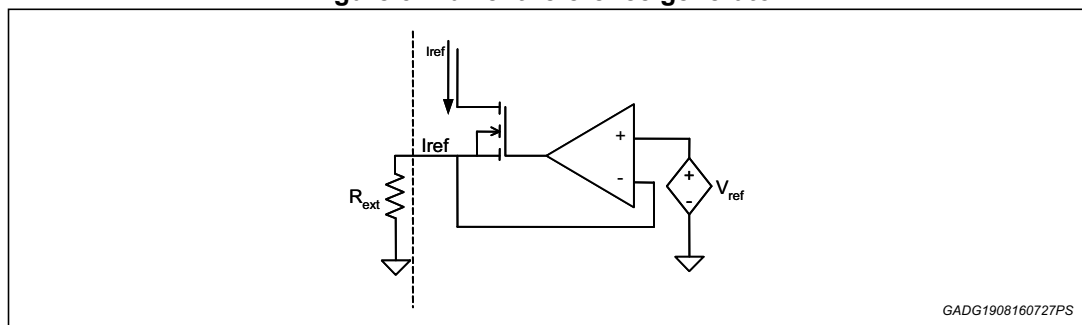


The circuit is designed for a 10 kΩ resistor. For all affected parameters, this resistor value is mentioned in the electrical characteristics section.

# 6 Operating modes

There are two modes of operation of the power supply: standby and run mode. However during RUN mode, there are three input voltage regions: low voltage, normal voltage and high voltage. A brief definition and description of each of these operating regions is described below.

## 6.1 Standby mode

STANDBY mode is defined by the following conditions:
- VBAT is within the required voltage range
- VBAT_SW may or may not be present
- IGN is in the OFF state
- PSU_EN is not asserted by the microprocessor

During standby mode, all functions are shutdown except the two standby supplies, VKAM and VSTBY, and the circuitry monitoring IGN and PSU_EN. During standby mode, current consumption is minimized. The standby functions are powered from VBAT.

There is no currents drawn from VBAT_SW or any other input except those required to perform the standby functions. Outputs, other than IGN_ON are disabled, sourcing nor sinking current.

## 6.2 Run mode

RUN mode is defined by the following conditions:
- VBAT is within the required range
- VBAT_SW is within the required range
- Either IGN is in the Run state and/or PSU_EN is in the active state

During RUN mode, all functions can be enabled. All functions listed above, with the exception of the standby functions, are powered by VBAT_SW.

If VBAT is not present, the circuit is fully running with the exception of PSU_EN and the standby functions (VKAM and VSTBY). In this condition the entry into the RUN MODE can only be performed by the IGN pin and the circuit is kept running until IGN pin is pulled low.

### 6.2.1 Entry into RUN mode

RUN mode is entered when at least one of the two signals IGN_SW or PSU_EN goes in the active state. These two signals may be applied in any order or simultaneously.

When the IGN input is valid, the active low IGN_ON signal is asserted.

The design of VDD5, VDDL and VCORE regulators limits the slew rate of the output voltages during the start-up as indicated in the electrical characteristic table and ensures that $V_{DD5}$ is always greater than $V_{DDL}$ and $V_{CORE}$.

As indicated in *Figure 4*, the switching regulator starts first with soft start control or reduced current limitation. When the VB voltage reaches the VDDL_ENUP threshold all the linear regulators start with controlled slew-rate. The slew-rate control is done controlling the slew

rate of the common voltage reference so the slew is different for each regulator because all start together and reach the steady-state at the same time but with different voltage levels.

## 6.3 Power down

The power down sequence starts when both IGN and PSU_EN signal are low. In this phase there is no control of the linear regulator output voltages. The falling slew-rate is defined from load currents and load capacitors. A voltage comparator controls VDDL voltage and ensures that the VDDL supply voltage will drop below 2V before initiating a new power-up sequence.

**Figure 4. Power up/down sequence**
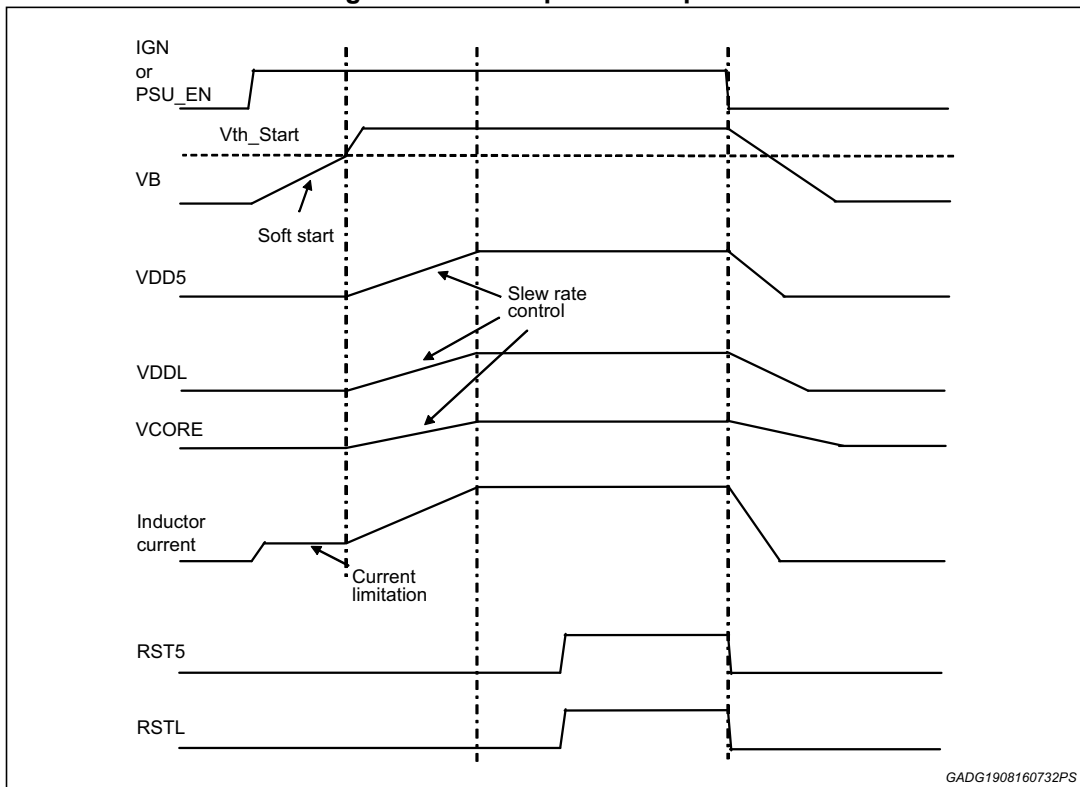
## 6.4 Low voltage operation

When L9758 is up and running it is fully operational with the VBAT and VBAT_SW pin voltages down to $V_{LVI\_LOW}$. When L9758 is up and running and the supply voltages are less than 5.5 V and are grater than or equal to $V_{LVI\_LOW}$ if the boost option is used the device is fully operational. If only the buck regulator is used the L9758 operates as follows:

- Switching regulator runs at 100% duty cycle;
- VKAM and VSTBY regulators are fully operational;
- VDDL fully operational;
- VCORE fully operational;
- VDD5 out of range with output voltage no less than 3.2 V;
- Tracking regulators out of range with output voltages no less than 3.2 V;
- Reset monitor RST5 and RSTL fully operational, with reset at RST5 pin is allowed.

## 6.5 High voltage operation

The L9758 is fully operational during jump start when the battery is temporarily replaced with a higher voltage source to aid starting the engine (26.5 V for 1 minute). The L9758 is fully operational during positive battery transient such as load dump (40 V maximum voltage with durations of up to 400 ms).

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 PowerSO-36 package information

### Figure 5. PowerSO-36 package outline



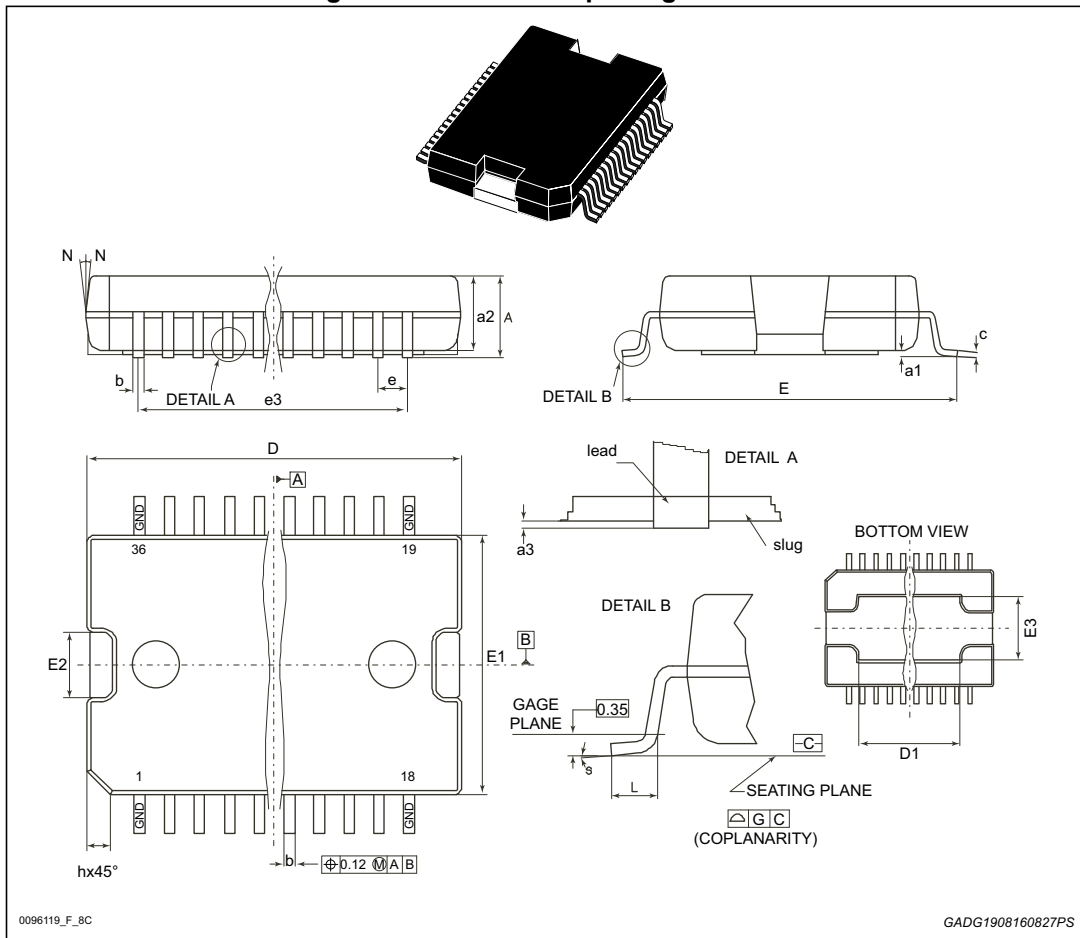0096119_F_8C                                                                           GADG1908160827PS

**Table 20. PowerSO-36 package mechanical data**

| Ref | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches[1] | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 3.60 | - | - | 0.1417 |
| a1 | 0.10 | - | 0.30 | 0.0039 | | 0.0118 |
| a2 | | - | 3.30 | - | - | 0.1299 |
| a3 | 0 | - | 0.10 | - | - | 0.0039 |
| b | 0.22 | - | 0.38 | 0.0087 | - | 0.0150 |
| c | 0.23 | - | 0.32 | 0.0091 | - | 0.0126 |
| D[2] | 15.80 | - | 16.00 | 0.6220 | - | 0.6299 |
| D1 | 9.40 | - | 9.80 | 0.3701 | - | 0.3858 |
| E | 13.90 | - | 14.5 | 0.5472 | - | 0.5709 |
| E1[2] | 10.90 | - | 11.10 | 0.4291 | - | 0.4370 |
| E2 | - | - | 2.90 | - | - | 0.1142 |
| E3 | 5.80 | - | 6.20 | 0.2283 | - | 0.2441 |
| e | - | 0.65 | - | - | 0.0256 | - |
| e3 | - | 11.05 | - | - | 0.4350 | - |
| G | 0 | - | 0.10 | 0 | - | 0.0039 |
| H | 15.50 | - | 15.90 | 0.6102 | - | 0.6260 |
| h | - | - | 1.10 | - | - | 0.0433 |
| L | 0.8 | - | 1.10 | 0.0315 | - | 0.0433 |
| N | 10° (max) | | | | | |
| s | 8° (max) | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. "D and E1" do not include mold flash or protusions. Mold flash or protusions shall not exceed 0.15 mm (0.006"). Critical dimensions are "a3", "E" and "G"..

# 8 Revision history

**Table 21. Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 12-Dec-2007 | 1 | Initial release. |
| 17-Nov-2010 | 2 | Updated *Section 1: Pins configuration*.<br>Updated *Figure 2: Functional block diagram*.<br>Updated *Section 3: Operating conditions*.<br>Updated *Table 7: General DC characteristics* and *Table 12: VCORE linear regulator*.<br>Added *Section 5.1: General function*.<br>Updated *Section 5.2: Switching pre-regulator*, *Section 5.6: RESET monitors* and *Section 5.8: Reference current*.<br>Updated *Section 5.3: VDD5, VDDL and VCORE linear regulators on page 21*. |
| 23-Nov-2010 | 3 | Update *Table 10*, *Table 11*, *Table 12*, *Table 13* and *Table 14*. |
| 20-Sep-2013 | 4 | Updated disclaimer. |
| 06-Sep-2016 | 5 | Updated:<br>– Title in cover page (added 'Automotive');<br>– *Features on page 1* (added 'AEC-Q100 qualified' and car icon);<br>– *Table 1: Device summary on page 1*.<br>– *Table 7: General DC characteristics on page 12*<br>– *Package information on page 27*. |

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