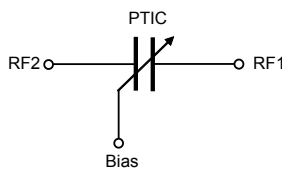


## Parascan™ tunable integrated capacitor



WLCSP 3 solder bars



### Features

- High power capability
- 5:1 tuning range
- High linearity
- High quality factor (Q)
- Low leakage current
- Compatible with high voltage control IC (STHV DAC series)
- RF tunable passive implementation in mobile phones to optimize antenna radiated performance
- Available in wafer level chip scale package:
  - WLCSP package 0.75 x 0.72 x 0.32 mm
- WLCSP package is not sensitive to moisture (MSL = 1)
- ECOPACK2 compliant component

### Applications

- Cellular antenna open loop tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- Open loop tunable RF filters

### Description

The ST integrated tunable capacitor offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan™, which is a version of barium strontium titanate (BST) developed by Paratek microwave.

BST capacitors are tunable capacitors intended for use in mobile phone application and dedicated to RF tunable applications. These tunable capacitors are controlled through an extended bias voltage ranging from 1 to 24 V. The implementation of BST tunable capacitor in mobile phones enables significant improvement in terms of radiated performance making the performance almost insensitive to the external environment.

Parascan is a trademark of Paratek Microwave Inc.

Product status link

[STPTIC-82C4](#)

# 1 Electrical characteristics

**Table 1. Absolute maximum ratings (limiting values)**

Symbol	Parameter	Rating	Unit
$P_{IN}$	Input power $RF_{IN}$ (CW model) / all RF ports	+40	dBm
$V_{ESD(HBM)}$	Human body model, JESD22-A114-B, all I/O	Class 1B <sup>(1)</sup>	V
$V_{ESD(MM)}$	Machine model, JESD22-A115-A, all I/O	+100	V
$V_{ESD(CDM)}$	Charge device model, JESD22-C101, all I/O	$> \pm 125$	V
$T_{device}$	Device temperature	+125	°C
$T_{stg}$	Storage temperature	-55 to +150	
$V_x$	Bias voltage	25	V

1. Class 1B defined as passing 500 V, but fails after exposure to 1000V ESD pulse.

**Table 2. Recommended operating conditions**

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
$P_{IN}$	RF input power		+33	+39	dBm
$F_{OP}$	Operating frequency	700		2700	MHz
$T_{device}$	Device temperature			+100	°C
$T_{OP}$	Operating temperature	-30		+85	
$V_{BIAS}$	Bias voltage	1		24	V

**Table 3. Representative performance ( $T_{amb} = 25\text{ °C}$  otherwise specified)**

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
$C_{1V}$	Capacitor at 1 V bias	STPTIC-82G2	8.54	9.7	10.86	pF
$C_{2V}$	Capacitor at 2 V bias	STPTIC-82G2	7.38	8.2	9.2	pF
$C_{24V}$	Capacitor at 24 V bias	STPTIC-82G2	1.53	1.66	1.79	pF
C	Capacitance accuracy	$V_{BIAS}$ range = 2 V/ 20 V			10	%
$\Delta C$	Tuning range	Ratio between $C_{1V}/C_{24V}$ <sup>(1)</sup>	5/1			
$I_L$	Leakage current	Measured with $V_{BIAS} = 24\text{ V}$			100	nA
$Q_{LB}$	Quality factor	Measured at 700 MHz at 2 V	55	65		
$Q_{HB}$	Quality factor	Measured at 2700 MHz at 10 V	25			
$Q_{HB}$	Quality factor	Measured at 2700 MHz at 2 V	20			
IP3	Third order intercept point	$V_{BIAS} = 2\text{ V}$ <sup>(2)(3)</sup>	52	60		dBm
		$V_{BIAS} = 20\text{ V}$ <sup>(2)(3)</sup>	70	75		dBm
H2	Second harmonic	$V_{BIAS} = 2\text{ V}$ <sup>(4)(3)</sup>		-65	-45	dBm

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
H2	Second harmonic	$V_{BIAS} = 20\text{ V}^{(4)(3)}$		-70	-60	dBm
H3	Third harmonic	$V_{BIAS} = 2\text{ V}^{(4)(3)}$		-35	-30	dBm
		$V_{BIAS} = 20\text{ V}^{(4)(3)}$		-65	-60	dBm
$t_T$	Transition time	Transition between 20 V to 2 V <sup>(5)</sup>			100	$\mu\text{s}$
		Transition between 2 V to 20 V			60	$\mu\text{s}$
		Transition between 20 V to 4 V or 4 V to 20 V			60	$\mu\text{s}$

1. Measured at low frequency
2.  $F_1 = 894\text{ MHz}$ ,  $F_2 = 849\text{ MHz}$ ,  $P_1 = +25\text{ dBm}$ ,  $P_2 = +25\text{ dBm}$ ,  $2f_1 - f_2 = 939\text{ MHz}$
3. IP3 and harmonics are measured in the shunt configuration in a 50  $\Omega$  environment
4. 850 MHz,  $P_{IN} = +34\text{ dBm}$
5. One or both of  $RF_{IN}$  and  $RF_{OUT}$  must be connected to DC ground, using the HVDAC turbo mode. Transition time for tuner between Cmin. to 90% of Cmax. or Cmax. to 90% of Cmin. include MIPI order work time (trig with last MIPI CLK).

## 1.1 Electrical characteristic curves

Figure 1. Capacitor variation versus bias voltage

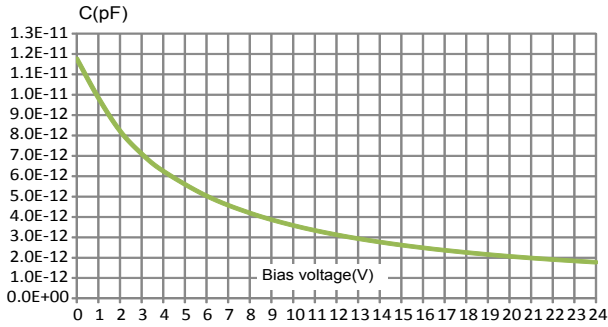


Figure 2. Quality factor versus frequency

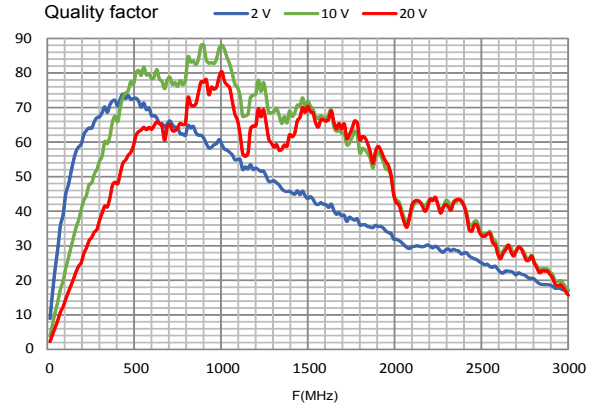


Figure 3. Harmonic power versus bias voltage (series)

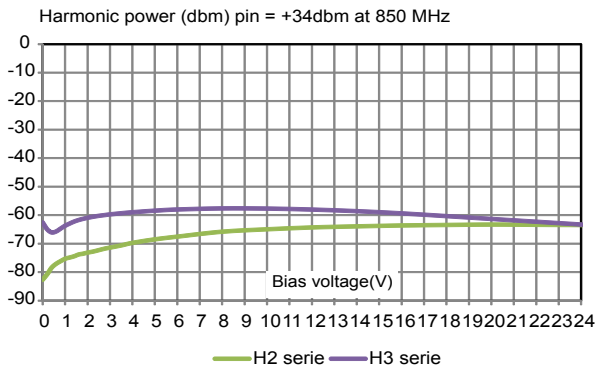


Figure 4. Harmonic power versus bias voltage (shunt)

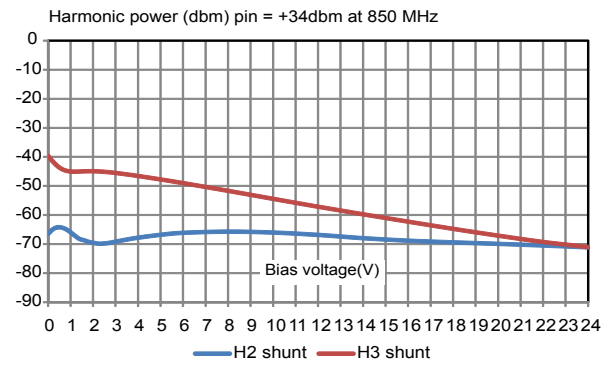
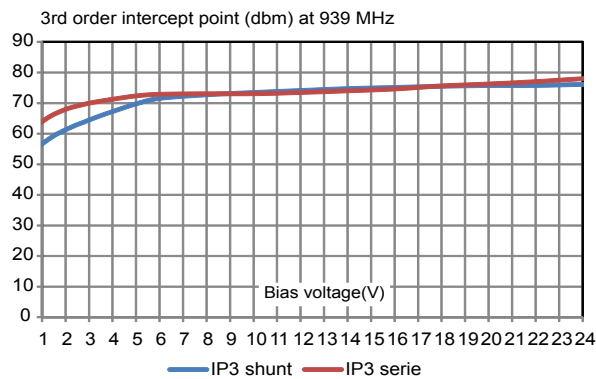
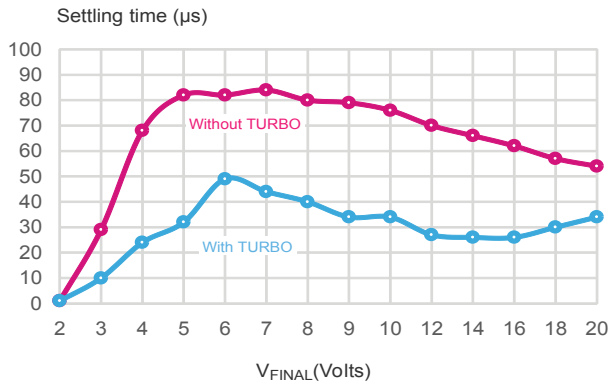


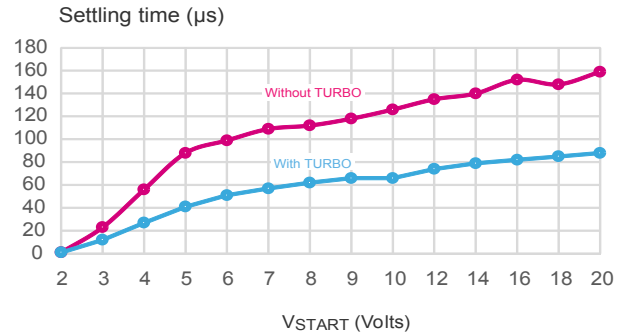
Figure 5. Third order intercept point (IP3)



**Figure 6. Settling time from 2 V to  $V_{FINAL}$**



**Figure 7. Settling time from  $V_{START}$  to 2 V**



**Table 4. Capacitance variation according to  $V_{BIAS}$**

$V_{BIAS}$ (V)	Capacitance (min.)	Capacitance (typ.)	Capacitance (max.)
2	7.38 pF	8.20 pF	9.02 pF
3	6.19 pF	6.87 pF	7.55 pF
4	5.39 pF	5.97 pF	6.56 pF
5	4.69 pF	5.19 pF	5.70 pF
6	4.20 pF	4.65 pF	5.10 pF
7	3.75 pF	4.15 pF	4.55 pF
8	3.43 pF	3.79 pF	4.15 pF
9	3.14 pF	3.46 pF	3.79 pF
10	2.92 pF	3.21 pF	3.51 pF
11	2.70 pF	2.98 pF	3.25 pF
12	2.54 pF	2.80 pF	3.05 pF
13	2.38 pF	2.62 pF	2.86 pF
14	2.26 pF	2.48 pF	2.70 pF
15	2.14 pF	2.34 pF	2.55 pF
16	2.04 pF	2.24 pF	2.43 pF
17	1.95 pF	2.13 pF	2.32 pF
18	1.87 pF	2.05 pF	2.22 pF
19	1.79 pF	1.96 pF	2.13 pF
20	1.73 pF	1.89 pF	2.05 pF

## 2 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 2.1 WLCSP 3 solder bars package information

Figure 8. WLCSP 3 solder bars package outline

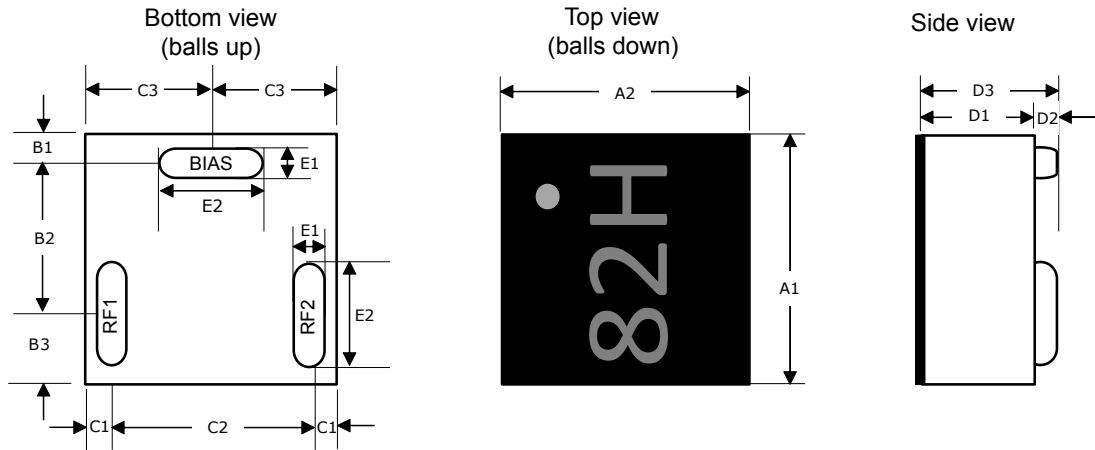


Table 5. WLCSP 3 solder bars package dimensions

Dimensions	A1	A2	B1	B2	B3	C1	C2	C3	D1	D2	D3	E1	E2
STPTIC-82G2C4	720	750	100	420	200	100	550	375	225	90	315	125	300
Tolerance	±30	±30	±15	±10	±15	±15	±10	±15	±20	±25	±40	±25	±25

Figure 9. Recommended PCB land pattern for WLCSP 3 solder bars package

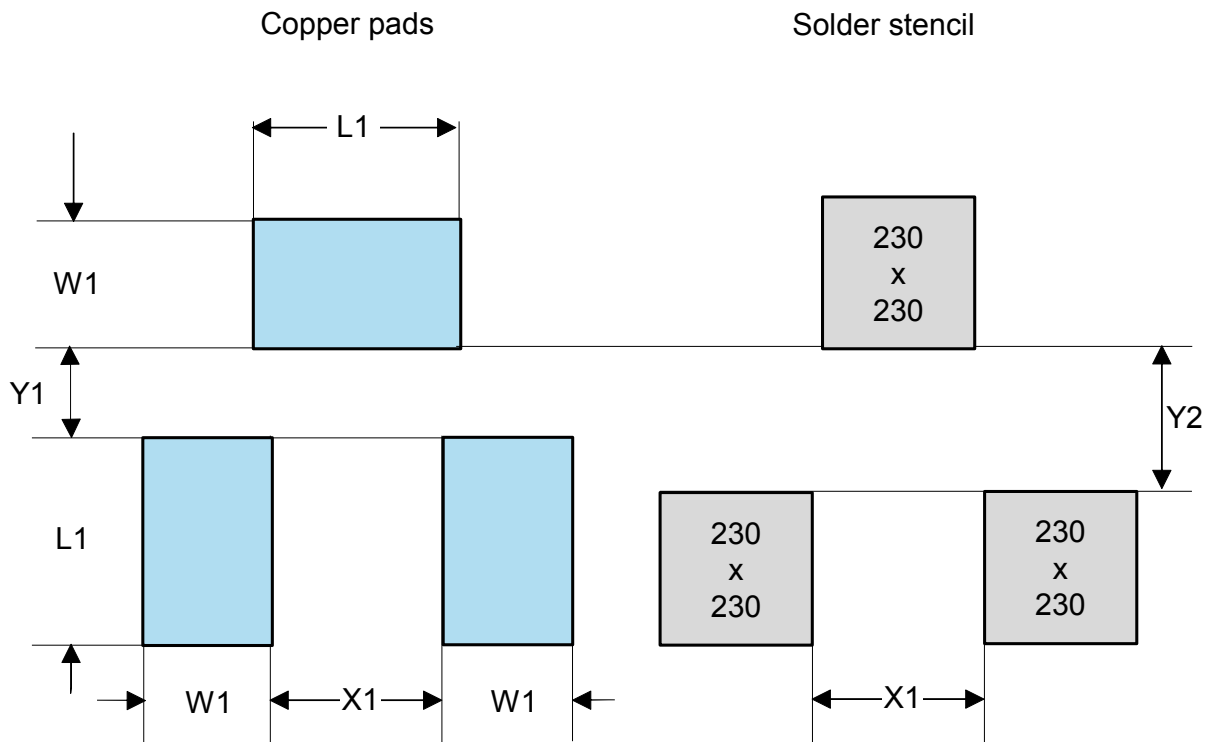


Table 6. Dimensions

Ball	L1	W1	X1	Y1	Y2
Typical values (in microns)	300	200	350	130	200



## 2.2 Packing information

Figure 10. Tape and reel outline

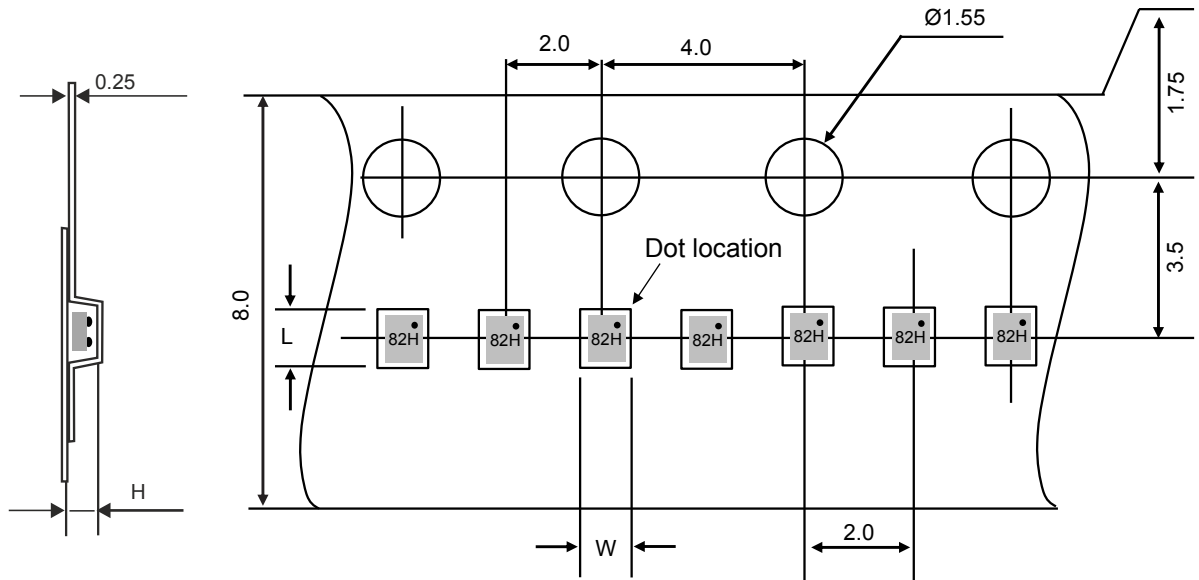
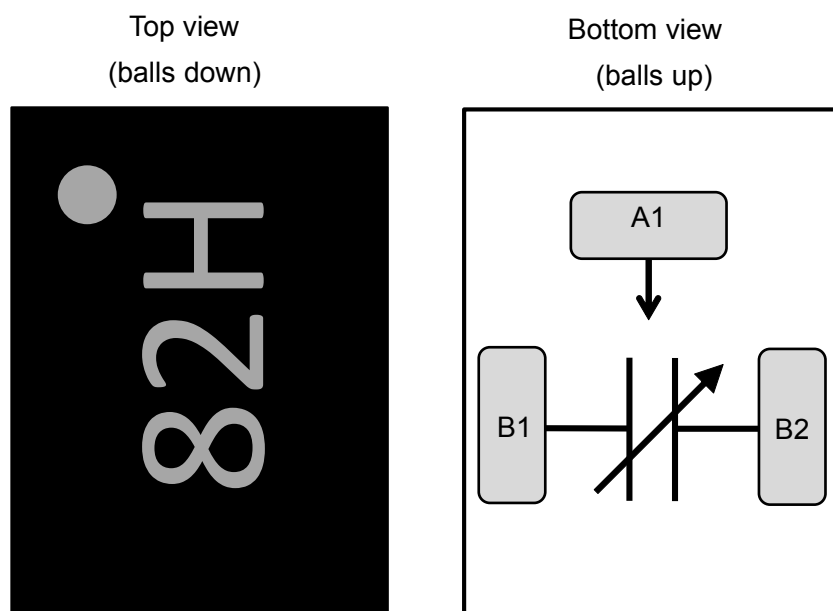


Table 7. Pocket dimensions

Pocket dimensions	L	W	H
STPTIC-82G2C4	820	790	385

**Figure 11. Marking**



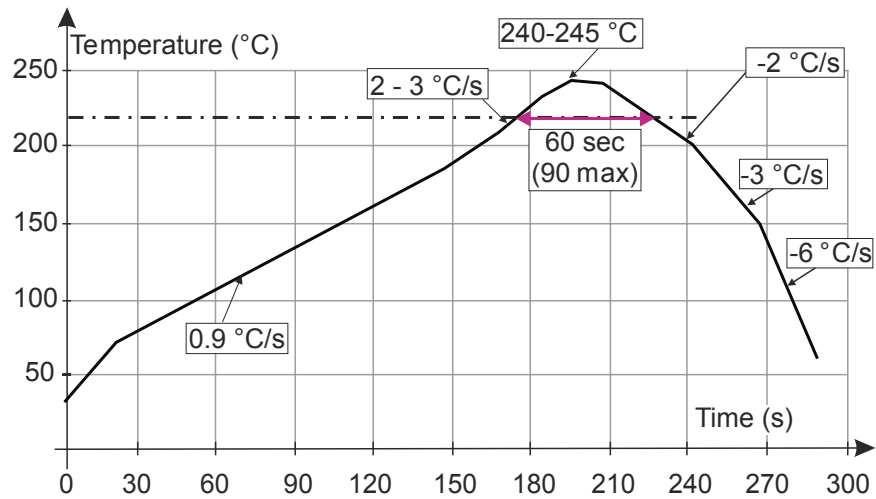
**Table 8. Pinout description**

Pad / ball number	pin name	Description
A1	DC bias	DC bias voltage
B1	RF1	RF input / output
B2	RF2 <sup>(1)</sup>	RF input / output

1. When connected in shunt, please connect RF2 (B2 ball) to GND

## 2.3 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 9. Recommended values for soldering reflow

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

### 3 Evaluation board

Figure 13. Series and shunt connection

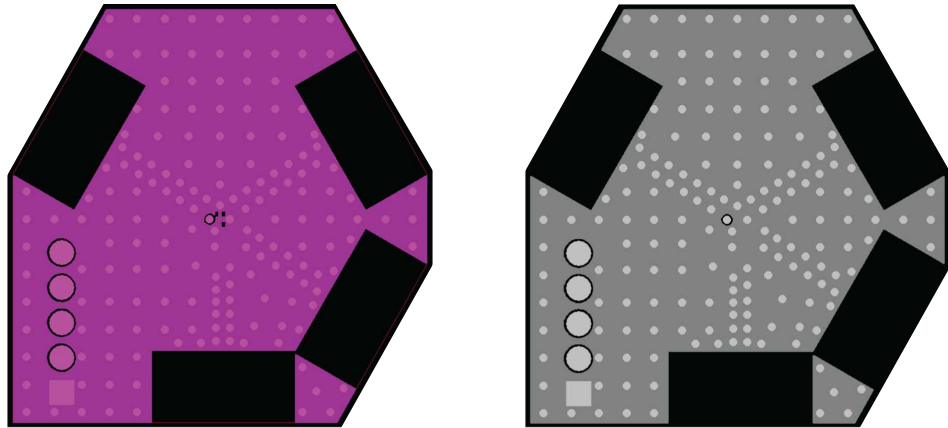


Figure 14. Layer 1 and layer 4

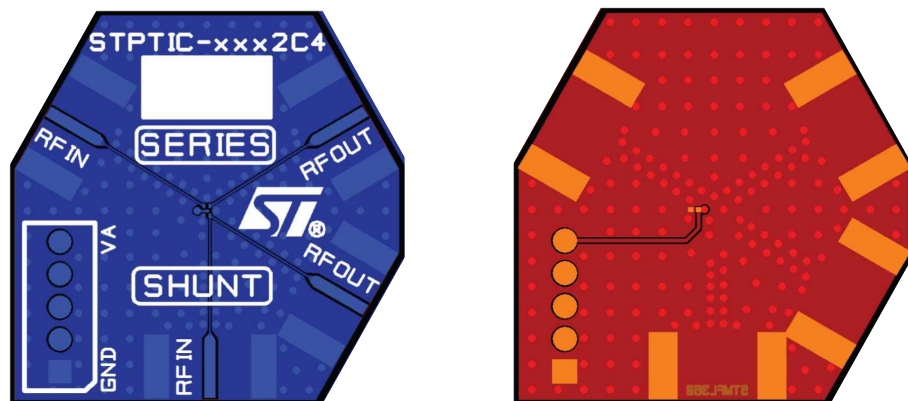
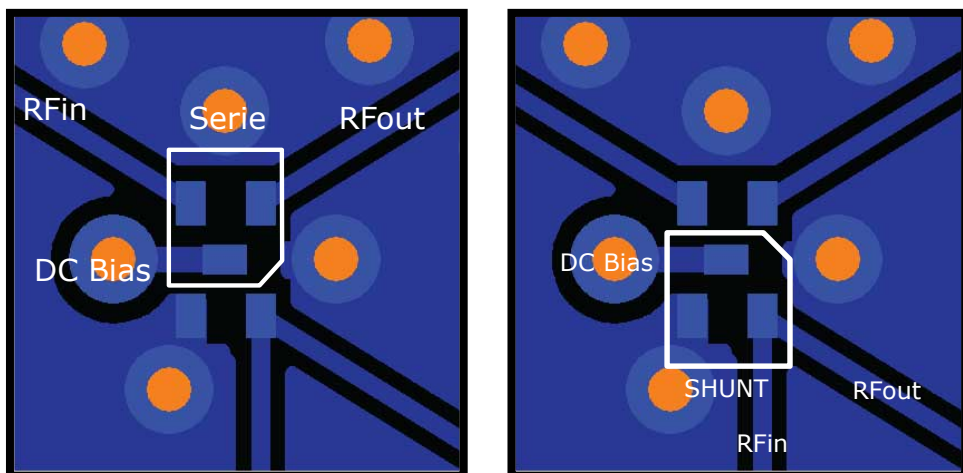


Figure 15. Layer 2 and layer 3



## 4 Ordering information

Figure 16. Ordering information scheme

ST	PTIC	-	82	G	2	C4
<u>Manufacturer</u>	<u>Product family</u>	-	<u>Capacitor value</u>	<u>Linearity</u>	<u>Tuning</u>	<u>Package</u>
ST Microelectronics	PTIC Parascan™ tunable Integrated capacitor		12 = 1.2 pF 27 = 2.7 pF 33 = 3.3 pF 39 = 3.9 pF 47 = 4.7 pF 56 = 5.6 pF 68 = 6.8 pF 82 = 8.2 pF	F: Standard (x24) G: Standard (x24) L: High (x48)	1 = 4/1 tuning 2 = 5/1 tuning	M6 : QFN C5 : WLCSP C4 : WLCSP 3 bars

Table 10. Ordering information

Order code	Marking	Base qty.	Package	Delivery mode
STPTIC82G2C4	82H	15 000	WLCSP 3 solder bars	Tape and reel

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
14-Dec-2016	1	First issue.
01-Mar-2017	2	Updated Table 3.
30-Apr-2018	3	Updated properties restrictions.
15-May-2018	4	Updated Figure 8. WLCSP 3 solder bars package outline.
25-Feb-2020	5	Updated Section Features.
16-Mar-2020	6	Updated Table 1. Absolute maximum ratings (limiting values).

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