M48Z128 M48Z128Y

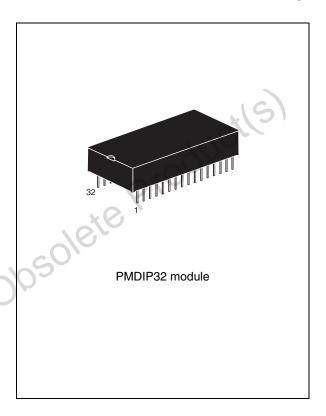
5.0 V, 1 Mbit (128 Kbit x 8) ZEROPOWER® SRAM

Not recommended for new design

Features

- Integrated, ultra low power SRAM, power-fail control circuit, and battery
- Conventional SRAM operation; unlimited WRITE cycles
- 10 years of data retention in the absence of power
- Battery internally isolated until power is first applied
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages: (V_{PFD} = power-fail deselect voltage)
 - $\begin{array}{ll} & \text{M48Z128: V}_{\text{CC}} = 4.75 \text{ to } 5.5 \text{ V}; \\ & 4.5 \text{ V} \leq \text{V}_{\text{PFD}} \leq 4.75 \text{ V} \end{array}$
 - M48Z128Y: V_{CC} = 4.5 to 5.5 V; 4.2 V \leq $V_{PFD} \leq$ 4.5 V
- Pin and function compatible with JEDEC standard 128 K x 8 SRAMs
- RoHS compliant
- Lead-free second level interconnect

This is information on a product still in production but not recommended for new designs.



Contents

1	Description
2	Operating modes
	2.1 READ mode
	2.2 WRITE mode 9
	2.3 Data retention mode
	2.4 V _{CC} noise and negative going transients
3	Maximum ratings
4	DC and AC parameters
5	Package mechanical data
6	Part numbering
7	Environmental information
8	Revision history
	ete Produc
Opso	



List of tables

Table 1. Table 2. Table 3	Signal names
Table 4.	WRITE mode AC characteristics
Table 5. Table 6.	Absolute maximum ratings
Table 7.	Capacitance
Table 8.	DC characteristics
Table 10.	Power down/up trip points DC characteristics
Table 11.	PMDIP32 – 32-pin plastic DIP module, package mechanical data
Table 12.	Revision history
	Signal names Operating modes 7 READ mode AC characteristics 8 WRITE mode AC characteristics 10 Absolute maximum ratings 12 Operating and AC measurement conditions 13 Capacitance 13 DC characteristics 14 Power down/up AC characteristics 15 POwer down/up trip points DC characteristics 15 PMDIP32 – 32-pin plastic DIP module, package mechanical data 16 Ordering information scheme 17 Revision history 19
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	Ops
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	AUC
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103	



List of figures M48Z128, M48Z128Y

List of figures

Figure 1. Figure 2. Figure 3. Figure 4. Figure 5. Figure 6	Logic diagram
Figure 7. Figure 8. Figure 9. Figure 10. Figure 11.	Chip enable controlled, WRITE AC waveforms
Figure 12.	Recycling symbols
	Obsoler
	oroduci(s)
Obsoli	Logic diagram



M48Z128, M48Z128Y Description

1 Description

The M48Z128/Y ZEROPOWER[®] RAM is a 128 Kbit x 8 non-volatile static RAM organized as131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic, 32-pin DIP module to provide a highly integrated battery-backed memory solution.

The M48Z128/Y is a non-volatile pin and function equivalent to any JEDEC standard 128 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed. The 32-pin, 600 mil DIP module houses the M48Z128/Y silicon with a long-life lithium button cell in a single package.

Figure 1. Logic diagram

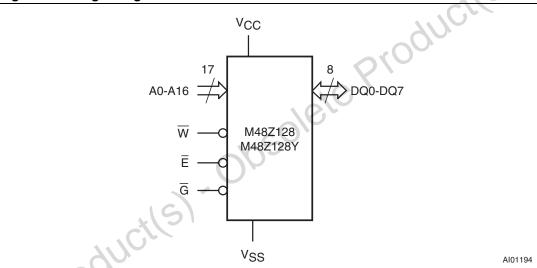


Table 1. Signal names

A0-A16	Address inputs
DQ0-DQ7	Data inputs / outputs
Ē	Chip enable input
G	Output enable input
W	WRITE enable input
V _{CC}	Supply voltage
V _{SS}	Ground
NC	Not connected internally

Description M48Z128, M48Z128Y

Figure 2. DIP connections

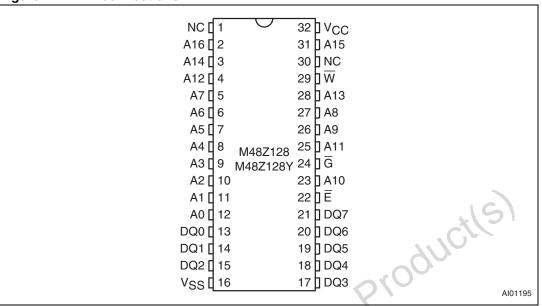
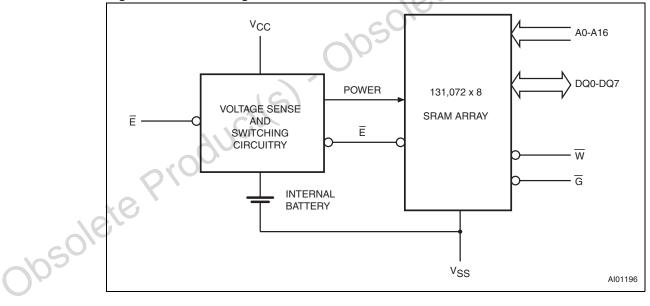


Figure 3. Block diagram



6/20 Doc ID 2426 Rev 6

M48Z128Y Operating modes

2 Operating modes

The M48Z128/Y also has its own power-fail detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC} . As V_{CC} falls below the switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

Mode	v _{cc}	Ē	G	W	DQ0-DQ7	Power
Deselect		V_{IH}	Х	Х	High Z	Standby
WRITE	4.75 to 5.5 V or	V _{IL}	Х	V _{IL}	D _{IN}	Active
READ	4.5 to 5.5 V	V_{IL}	V_{IL}	V _{IH}	D _{OUT}	Active
READ		V _{IL}	V _{IH}	V _{IH}	High Z	Active
Deselect	V _{SO} to V _{PFD} (min) ⁽¹⁾	Х	Х	Х	High Z	CMOS standby
Deselect	≤ V _{SO} ⁽¹⁾	Х	Х	X	High Z	Battery backup mode

^{1.} See Table 10 on page 15 for details.

Note: $X = V_{IH}$ or V_{IL} ; V_{SO} = battery backup switchover voltage.

2.1 READ mode

The M48Z128/Y is in the READ mode whenever \overline{W} (WRITE enable) is high and \overline{E} (chip enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the \overline{E} and \overline{G} (output enable) access times are also satisfied. If the \overline{E} and \overline{G} access times are not met, valid data will be available after the later of chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}). The state of the eight three-state data I/O signals is controlled by \overline{E} and \overline{G} . If the outputs are activated before t_{AVQV} , the data lines will be driven to an indeterminate state until t_{AVQV} . If the address inputs are changed while \overline{E} and \overline{G} remain low, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

7/20

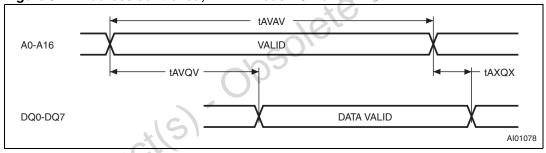
Operating modes M48Z128, M48Z128Y

tAVAV A0-A16 VALID tAVQV tAXQX tEHQZ tELQV Ē tELQX tGLQV tGHQZ $\overline{\mathsf{G}}$ tGLQX · DQ0-DQ7 DATA OUT AI01197

Figure 4. Chip enable or output enable controlled, READ mode AC waveforms

Note: WRITE enable (\overline{W}) = high.

Figure 5. Address controlled, READ mode AC waveforms



Note: Chip enable (\overline{E}) and output enable (\overline{G}) = low, WRITE enable (\overline{W}) = high.

Table 3. READ mode AC characteristics

			M48Z	128/Y	M48Z	128/Y	M48Z	128/Y	
\ 0	Symbol	Parameter ⁽¹⁾	-7	70	-8	85	-1	20	Unit
	,		Min	Max	Min	Max	Min	Max	
2003	t _{AVAV}	READ cycle time	70		85		120		ns
\bigcirc	t _{AVQV}	Address valid to output valid		70		85		120	ns
	t _{ELQV}	Chip enable low to output valid		70		85		120	ns
	t _{GLQV}	Output enable low to output valid		35		45		60	ns
	t _{ELQX} (2)	Chip enable low to output transition	5		5		5		ns
	t _{GLQX} ⁽²⁾	Output enable low to output transition	3		3		3		ns
	t _{EHQZ} (2)	Chip enable high to output Hi-Z		30		35		45	ns
	t _{GHQZ} (2)	Output enable high to output Hi-Z		20		25		35	ns
	t _{AXQX}	Address transition to output transition	5		5		10		ns

^{1.} Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).

8/20 Doc ID 2426 Rev 6



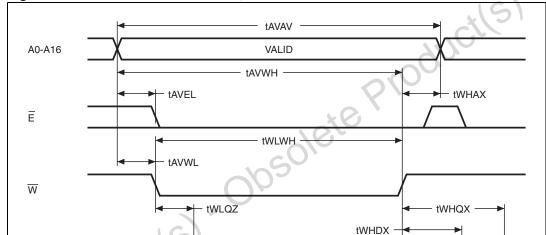
^{2.} $C_L = 5 pF$.

M48Z128, M48Z128Y Operating modes

2.2 WRITE mode

The M48Z128/Y is in the WRITE mode whenever \overline{W} and \overline{E} are active. The start of a WRITE is referenced from the latter occurring falling edge of \overline{W} or \overline{E} . A WRITE is terminated by the earlier rising edge of \overline{W} or \overline{E} .

The addresses must be held valid throughout the cycle. \overline{E} or \overline{W} must return high for minimum of t_{EHAX} from \overline{E} or t_{WHAX} from \overline{W} prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} or t_{EHDX} afterward. \overline{G} should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on \overline{E} and \overline{G} , a low on \overline{W} will disable the outputs t_{WLOZ} after \overline{W} falls.



DATA INPUT

AI01198

tDVWH

Figure 6. WRITE enable controlled, WRITE AC waveforms

Note: Output enable (\overline{G}) = high.

DQ0-DQ7

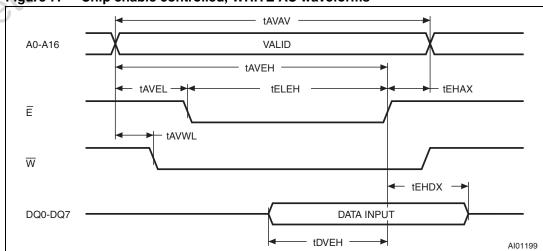


Figure 7. Chip enable controlled, WRITE AC waveforms

Note: Output enable (\overline{G}) = high.

Doc ID 2426 Rev 6 9/20

Operating modes M48Z128, M48Z128Y

Table 4. WRITE mode AC characteristics

		M48Z	128/Y	M48Z	128/Y	M48Z	128/Y	
Symbol	Parameter ⁽¹⁾ –70		-85		-120		Unit	
		Min	Max	Min	Max	Min	Max	
t _{AVAV}	WRITE cycle time	70		85		120		ns
t _{AVWL}	Address valid to WRITE enable Low	0		0		0		ns
t _{AVEL}	Address valid to chip enable low	0		0		0		ns
t _{WLWH}	WRITE enable pulse width	55		65		85		ns
t _{ELEH}	Chip enable low to chip enable high	55		75		100		ns
t _{WHAX}	WRITE enable high to address transition	5		5		5		ns
t _{EHAX}	Chip enable high to address transition	15		15		15	15	ns
t _{DVWH}	Input valid to WRITE enable high	30		35		45		ns
t _{DVEH}	Input valid to chip enable high	30		35		45		ns
t _{WHDX}	WRITE enable high to input transition	0		0	~4O	0		ns
t _{EHDX}	Chip enable high to input transition	10		10		10		ns
t _{WLQZ} (2)(3)	WRITE enable low to output Hi-Z		25	48	30		40	ns
t _{AVWH}	Address valid to WRITE enable high	65	7/6	75		100		ns
t _{AVEH}	Address valid to chip enable high	65	O,	75		100		ns
t _{WHQX} (2)(3)	WRITE enable high to output transition	5		5		5		ns

^{1.} Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).

2.3 Data retention mode

With valid V_{CC} applied, the M48Z128/Y operates as a conventional BYTEWIDETM static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD} . All outputs become high impedance, and all inputs are treated as "Don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP} write protection takes place. When V_{CC} drops below V_{SO} , the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z128/Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO} . As system power returns and V_{CC} rises above V_{SO} , the battery is disconnected, and the power supply is switched to external V_{CC} . Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER} , normal RAM operation can resume.

For more information on battery storage life refer to the application note AN1012.

^{2.} $C_L = 5 pF$.

^{3.} If \overline{E} goes low simultaneously with \overline{W} going low, the outputs remain in the high impedance state.

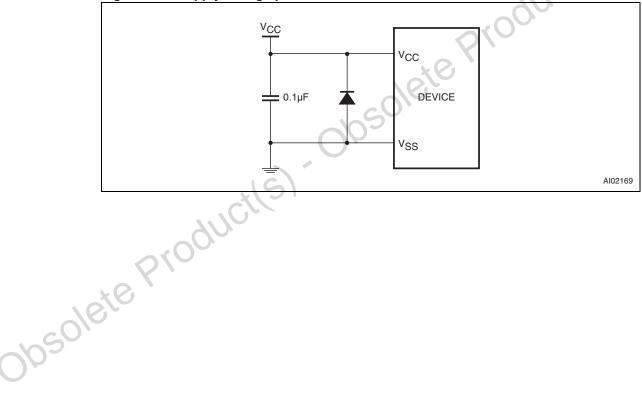
M48Z128, M48Z128Y Operating modes

2.4 V_{CC} noise and negative going transients

 I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 μ F (see *Figure 8*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface-mount).

Figure 8. Supply voltage protection



Maximum ratings M48Z128, M48Z128Y

Maximum ratings 3

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
T _A	Ambient operating temperature	0 to 70	°C
T _{STG}	Storage temperature (V _{CC} off, oscillator off)	-40 to 85	C°C
T _{BIAS}	Temperature under bias	-10 to 70	°C
T _{SLD} ⁽¹⁾	Lead solder temperature for 10 seconds	260	°C
V _{IO}	Input or output voltages	-0.3 to 7	V
V _{CC}	Supply voltage	-0.3 to 7.0	V
Io	Output current	20	mA
P _D	Power dissipation	1	W

Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.

Caution:

Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup Obsolete Product(s)

Doc ID 2426 Rev 6 12/20

4 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter	M48Z128/Y	Unit
Supply voltage (V _{CC})	4.75 to 5.5 V or 4.5 to 5.5	V
Ambient operating temperature (T _A)	0 to 70	C°C
Load capacitance (C _L)	100	pF
Input rise and fall times	≤ 5	ns
Input pulse voltages	0 to 3	V
Input and output timing ref. voltages	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. AC measurement load circuit

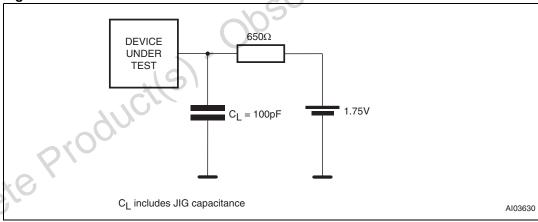


Table 7. Capacitance

Symbol	Parameter ⁽¹⁾⁽²⁾	Min	Max	Unit
C _{IN}	Input capacitance	-	10	pF
C _{IO} (3)	Input / output capacitance	-	10	pF

- 1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
- 2. At 25 °C, f = 1 MHz.
- 3. Outputs deselected.

57

DC characteristics Table 8.

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				M4	8Z128/Y		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Sym	Parameter	Test condition ⁽¹⁾	-70 /			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				Min	Max		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Input leakage current	$0 \text{ V} \leq V_{IN} \leq V_{CC}$		±1	μA	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	I _{LO} ⁽²⁾	Output leakage current	$0 \text{ V} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}$		±1	μΑ	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	I _{CC}	Supply current			105	mA	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	I _{CC1}	Supply current (standby) TTL	$\overline{E} = V_IH$		7	mA	
V_{IH} Input high voltage 2.2 $V_{CC} + 0.3$ V V_{OL} Output low voltage $I_{OL} = 2.1 \text{ mA}$ 0.4 V	I _{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2 \text{ V}$		4	mA	
V _{OL} Output low voltage I _{OL} = 2.1 mA 0.4 V	V _{IL}	Input low voltage		-0.3	0.8	V	
	V _{IH}	Input high voltage		2.2	V _{CC} + 0.3	V	
	V _{OL}	Output low voltage	I _{OL} = 2.1 mA		0.4	V	
. Valid for ambient operating temperature: T _A = 0 to 70 °C; V _{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted). 2. Outputs deselected.		Output high voltage		2.4	O	V	
ci(s)	2. Output	s deselected.	isolete				
	2. Output	s deselected.	Obsolete				
	2. Output	s deselected.	Obsolete				
Plan	2. Output	s deselected.	Obsolete				
i ate Pilo	2. Output	s deselected.	Obsolete				
detePla	2. Output	s deselected.	Obsolete				
asolete Pro	2. Output	s deselected.	Obsolete				
osolete Pro	2. Output	s deselected.	Obsolete				

^{1.} Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).

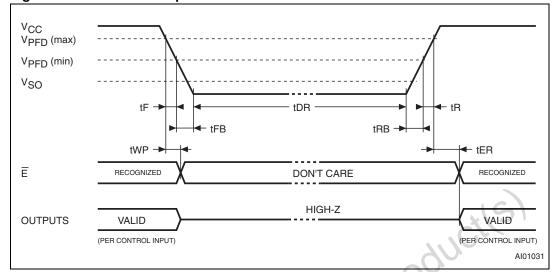


Figure 10. Power down/up mode AC waveforms

Table 9. Power down/up AC characteristics

Symbol	Parameter ⁽¹⁾	Min	Max	Unit
t _F ⁽²⁾	V _{PFD} (max) to V _{PFD} (min) V _{CC} fall time	300		μs
t _{FB} ⁽³⁾	V _{PFD} (min) to V _{SS} V _{CC} fall time	10		μs
t _R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		μs
t _{RB}	V _{SS} to V _{PFD} (min) V _{CC} rise time	1		μs
t _{WP}	Write protect time	40	150	μs
t _{ER}	E recovery time	40	120	ms

Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

Table 10. Power down/up trip points DC characteristics

Symbol	Parameter ⁽¹⁾⁽²⁾	Min	Тур	Max	Unit	
V _{PFD}	Power-fail deselect voltage	M48Z128	4.5	4.6	4.75	V
	Fower-lan deselect voltage	M48Z128Y	4.2	4.3	4.5	V
V _{SO}	Battery backup switchover voltage	M48Z128/Y		3.0		V
t _{DR} ⁽³⁾	Expected data retention time	10			YEARS	

^{1.} All voltages referenced to V_{SS} .

3. At 25 °C; $V_{CC} = 0 \text{ V}$.

577

^{2.} V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 μ s after V_{CC} passes V_{PFD} (min).

^{3.} V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

^{2.} Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).

PMDIP

Package mechanical data 5

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

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Figure 11. PMDIP32 - 32-pin plastic DIP module, package outline

Note:

Drawing is not to scale.

Table 11. PMDIP32 - 32-pin plastic DIP module, package mechanical data

	Table 11.	i mbii oz oz pili plastio bii illodalic, paokage illodialida data					
	Symb	mm		inches			
	Syllib	Тур	Min	Max	Тур	Min	Max
	Α	9	9.27	9.52		0.365	0.375
	A1		0.38	_		0.015	_
	K B		0.43	0.59		0.017	0.023
7/6	С		0.20	0.33		0.008	0.013
-7501	D		42.42	43.18		1.670	1.700
002	Е		18.03	18.80		0.710	0.740
0	e1		2.29	2.79		0.090	0.110
	e3	38.1			1.5		
	eA		14.99	16.00		0.590	0.630
	L		3.05	3.81		0.120	0.150
	S		1.91	2.79		0.075	0.110
	N		32			32	

16/20 Doc ID 2426 Rev 6 M48Z128, M48Z128Y Part numbering

6 Part numbering





Supply voltage and write protect voltage

$$128^{(1)} = V_{CC} = 4.75 \text{ to } 5.5 \text{ V}; V_{PFD} = 4.5 \text{ to } 4.75 \text{ V}$$

 $128Y^{(1)} = V_{CC} = 4.5 \text{ to } 5.5 \text{ V}; V_{PFD} = 4.2 \text{ to } 4.5 \text{ V}$

Speed

-70 = 70 ns

-85 = 85 ns

 $-120^{(2)} = 120 \text{ ns}$

Package

PM = PMDIP32

Temperature range

1 = 0 to 70 °C

Shipping method

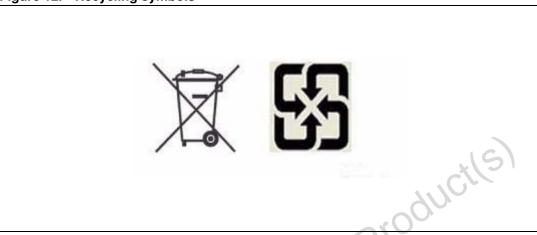
blank = ECOPACK® package, tubes

- 1. Device is not recommended for new design. Contact local ST sales office for availability.
- 2. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Environmental information

Figure 12. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

577

18/20 Doc ID 2426 Rev 6

Josoleite Produci(s)

M48Z128, M48Z128Y Revision history

8 Revision history

Table 13. Revision history

Date	Revision	Changes		
May-1999	1	First issue		
13-Apr-2000	2	Document layout changed; surface-mount chip set solution added		
20-Jun-2000	2.1	t _{GLQX} changed (<i>Table 3</i>)		
19-Jul-2000	2.2	M48Z128V added		
14-Sep-2001	3	Reformatted; added temperature information (Table 7, 8, 3, 4, 9, 10)		
07-Nov-2001	3.1	Remove chipset option from ordering Information (Table 12)		
20-May-2002	3.2	Modify reflow time and temperature footnotes (Table 5)		
18-Nov-2002	3.3	Modifying SMT solution text (Figure 2, 4; Table 2)		
17-Sep-2003	3.4	Remove references to M68ZXXX (obsolete) parts (<i>Figure 4</i> ; <i>Table 2</i>); update disclaimer		
22-Feb-2005	4	Reformatted; IR reflow, SO package updates (Table 5)		
20-Jul-2010	5	Reformatted document; updated <i>Features</i> , <i>Section 3: Maximum ratings</i> , <i>Table 11</i> , <i>12</i> ; added ECOPACK [®] text to <i>Section 5</i> ; added <i>Section 7: Environmental information</i> ; removed SOH28, SNAPHAT [®] housing and all references from datasheet.		
6-Sep-2011	6	Devices are not recommended for new design (updated cover page, Table 12); updated footnote of Table 5: Absolute maximum ratings; updated Section 7: Environmental information; removed M48Z128V.		
osoleite Produci(s)				

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