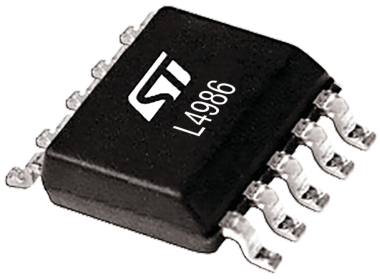
L4986

Datasheet

CCM PFC controller with high voltage startup



Features

- Peak current mode CCM-operated
- 800 V high voltage startup with integrated input voltage sensing
- Active input filter capacitor discharge
- Proprietary multiplier “emulator” with minimum THD of line current in all operating conditions (CCM and DCM)
- Extremely few external components
- Protections: feedback loop failure, OVP, OCP, inductor saturation, brown-in, brownout (compliant to medical SMPS standards)
- Inductor current sense
- Disable and low consumption function
- In-rush current monitoring
- Soft-start for smooth startup
- 1.2% (@ Tj = 25 °C) internal reference voltage
- 65 kHz (A version) and 130 kHz (B version) switching frequency
- PGOOD_OUT and adjustable PGOOD_IN
- SSOP10 package

Application

- PFC pre-regulators for:
  - IEC61000-3-2 and JEIDA-MITI compliant SMPS in excess of 1 kW
  - Desktop PC, server, web server, game console
  - High power LED luminaries
  - Industrial and medical SMPS according to IEC 60601-1-2

Product status link
L4986
L4986A
L4986B
L4986ATR
L4986BTR

Product summary		
Order codes	**Package**	**Packaging**
L4986A	SSOP10	Tube
L4986B		Tube
L4986ATR		Tape and reel
L4986BTR		Tape and reel

Description

The L4986 is a peak current-mode PFC controller for boost converter with a proprietary multiplier “emulator” which in addition to the innovative THD optimizers guarantee very low Total Harmonic Distortion (THD) performance in all operating conditions. The device comes in a pin SO package and offers a high performance/ low-component count solution for CCM-operated boost PFC pre-regulators in EN61000-3-2 and JEIDA-MITI compliant applications, in a power range that spans from few hundred W to some kW.

The device, thanks to a proprietary off-time modulator, operates in quasi-fixed frequency in all operating conditions. Two options are available, 65 kHz for A and 130 kHz for B.

The 800 V high voltage start-up block includes also the circuitry to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulation (such as IEC 61010-1 or IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitors.

Product label

The device features low consumption and disable functions allowing usage in applications supposed to comply even with the latest energy saving requirements issued by Energy Star, the Department of Energy (DoE) in the United States, the European Code of Conduct, the European Union's Ecodesign Directive, and other guidelines.

In addition to an overvoltage protection able to keep the output voltage under control during transient conditions, the IC is provided also with a protection against feedback loop failures or erroneous settings and boost inductor saturation. The brownout protection function allows to design medical equipment according to the latest regulations driven by IEC 60601-1-2 which requires the output regulation in case of mains dips lasting up to 500 msec. Soft-start limits the peak current.

The PG_IN is an adjustable input comparator suitable for monitoring the PFC output voltage and accordingly driving a logic signal exiting from PG_OUT pin. The totem-pole output stage, capable of 0.7 A source and 1.5 A sink current, is suitable for big MOSFET or IGBT drive.

1 Block diagram and typical application

Figure 1. **Block diagram**

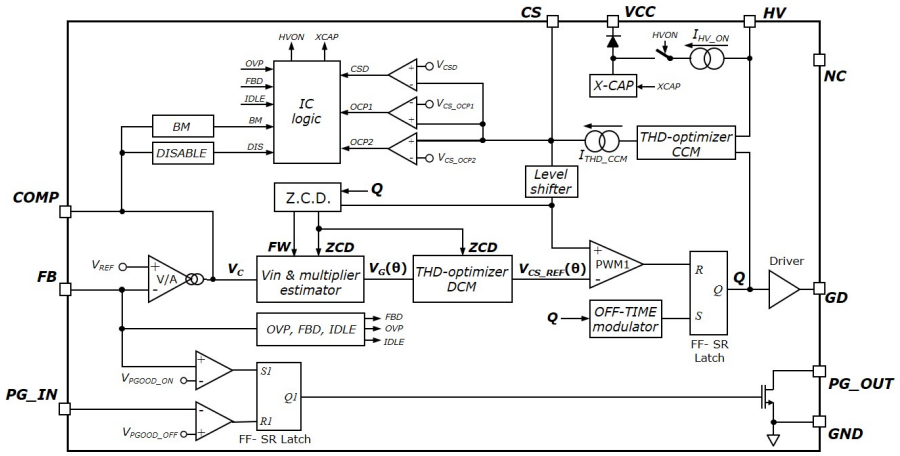
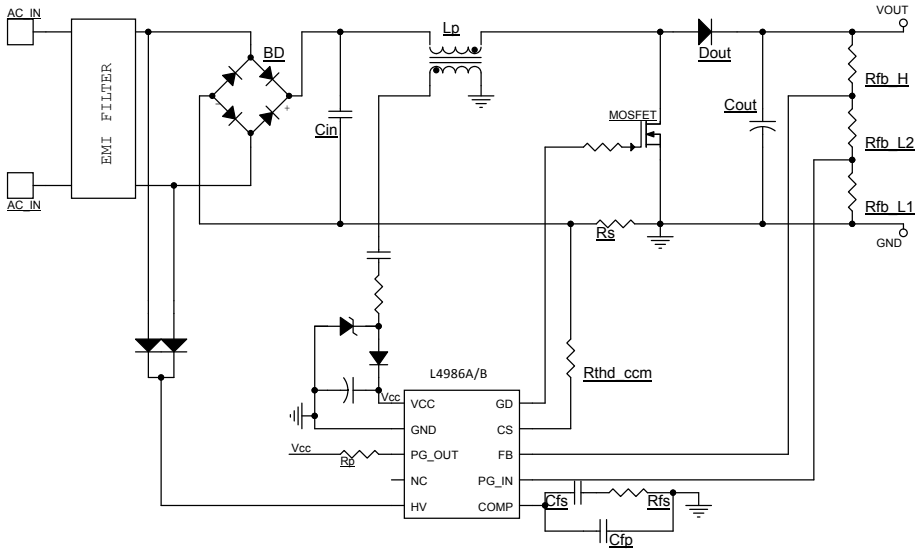


Figure 2. **Typical application**



2 Pin connection and functions

Figure 3. **Pin connection (top view)**

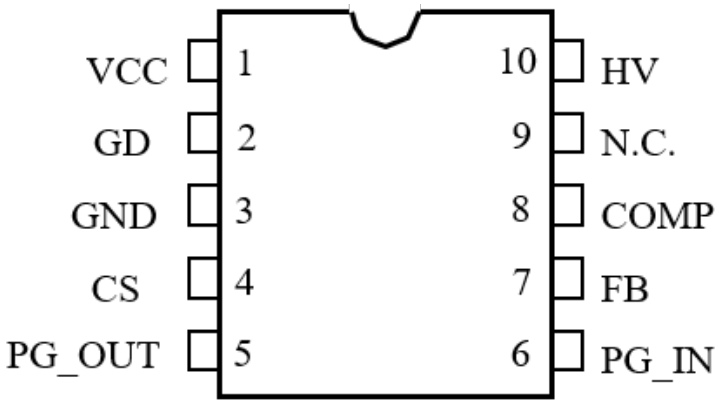


Table 1. **Pin description**

No.	Name	Function
1	VCC	Supply voltage. The internal high voltage start-up generator charges an electrolytic capacitor connected between this pin and GND as long as the voltage on the pin is below the start-up threshold of the IC, after it is disabled and the chip turns on. A bypass capacitor to GND has to be place close to the pins to get a clean bias voltage.
2	GD	Gate driver output. The output stage is able to drive power MOSFETs and IGBTs; it is capable of 0.7 A source current and 1.5 A sink current (typical values).
3	GND	IC ground. Current return for both the signal/bias part of the IC and the gate driver current. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
4	CS	Current sense input. The inductor current is sensed through a resistor R_S on the current return side. The resulting negative voltage is applied to this pin and compared to an internal sinusoidal-shaped reference to determine the turn-off instant of the external power switch. The pin is equipped with an internal current generator (sourced current during power switch on-time); it can be used, by simply adding a series resistor (R_{THD_CCM}) for improved THD in CCM operation. If the voltage on the pin goes below V_{CS_OCP1} (-0.49 V typ.) the internal overcurrent comparator is triggered and terminates the conduction cycle of the external power switch before the normal PWM circuit does. In this way, the peak inductor current is limited at a maximum of $0.49/R_S$. A second overcurrent level set at V_{CS_OCP2} (-0.75 V typ.) detects abnormal current values (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that immediately stops the converter activity until the current level reaches the zero-current threshold V_{CS_ZCD} (-10 mV typical value). It allows safe operations also during current surges occurring at power-up or after a mains dip or missing cycle; in fact it allows switching start/restart only when the overcurrent event is definitively over.
5	PG_OUT	Power good output (open drain). The pin is actively pulled to ground once the IC is turned on and the FB pin voltage exceeds the internal threshold V_{PGOOD_ON} (2.375 V typ.). If the PG_IN input is lower than the internal threshold V_{PGOOD_OFF} (1.25 V typ.), the PG_OUT pin is set to high impedance.
6	PG_IN	Power good input. The pin is used to set the off-threshold of PGOOD comparator and it is connected to the output voltage resistor divider.
7	FB	Inverting input of the trans-conductance Error Amplifier (OTA).

No.	Name	Function
		The information on the output voltage of the PFC regulator is fed into the pin through a resistor divider so that its voltage is proportional to the instantaneous value of the high voltage bus (V_{BULK}). Under steady-state conditions the voltage on pin sits at the internal reference of the error amplifier (V_{REF} = 2.5 V). If the voltage exceeds the steady-state value by 7% ($V_{FB} > V_{FB\_S}$), e.g. due to an output voltage overshoot, the switching activity is stopped until $V_{FB} < V_{FB\_R}$ (2.55 V typ.). If the voltage at FB pin is below $V_{FB\_FF/EBM}$ (0.5 V typ.) either a failure of the output divider is assumed or the device is externally forced in burst-mode operation. In both cases the PFC controller is stopped with low consumption. See Section 5.7 Idle operation (external burst-mode function) and Section 5.10.6 Feedback failure detection for further details.
8	COMP	Output pin of the trans-conductance Error Amplifier (OTA). A compensation network is placed between this pin and GND to allow stability of the control loop and ensure high PF and THD. To avoid uncontrolled rise of the output voltage at light or zero load, when $V_{COMP} < V_{COMP\_S}$ (1 V typ. Burst Mode condition) the gate driver pin (GD) is forced low and the switching activity is stopped. If the Burst Mode condition is triggered when GD is high, the system is allowed to complete the current ON-time and the system stoppage takes place after GD falling edge. The pin can be also used to disable the device by forcing $V_{COMP} < V_{COMP\_DIS}$ (0.7 V typ.) by means of an external pull-down active network.
9	N.C.	High voltage spacer. This pin is not internally connected to isolate the high voltage section and ease compliance with safety regulations (creepage distance) on the PCB.
10	HV	High voltage start-up generator input / AC voltage sensing input. The pin, able to withstand 800 V, has to be connected to the AC side of the input bridge via a pair of diodes (1N400x type) to sense the AC input voltage. If the voltage on the pin is higher than V_{HV_START} (29 V typ.), an internal pull-up circuit charges the capacitor connected between the pin VCC and GND. Initially the current is low for safety in case of a shorted VCC, and then it goes to the normal level as far as the VCC pin reaches the start-up threshold (V_{CC_ON}). The generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold (V_{CC_OFF}). The pin is used also to sense the AC voltage, which is used by the AC brownout, the input voltage feedforward and the THD-CCM optimizer functions. An internal logic circuit detects that the unit has been detached from the power line; if this event occurs then, the HV pin sinks a current to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulations (such as IEC 61010-1 or IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitor, thus saving the associated power losses and enabling ultra-low consumption in stand-by conditions. In case an AC brownout condition is detected the internal generator is alternatively turned on and off and, as a consequence, the voltage at VCC pin cycles between the start-up threshold and the UVLO threshold.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
VCC	1	Supply voltage	-0.3 to 30	V
ICC	1	Maximum supply current	0 to 25	mA
GD	2	Gate driver	-0.3 to VCC	V
CS	4	Current sense	-10 to 3.6	V
PG_OUT	5	PGOOD output	-0.3 to VCC	V
PG_IN	6	PGOOD input (IPG_IN < 1 mA)	-0.3 to self-limited	V
FB	7	Input feedback (IFB < 1mA)	-0.3 to self-limited	V
COMP	8	OTA output	-0.3 to 6	V
HV	10	Line voltage input (referred to GND)	-1 to 800	V

Table 3. Recommended operating conditions.

Symbol	Pin	Parameter	Min.	Max.	Unit	Remarks
VCC	1	IC supply voltage	-0.3	24.5	V	Internal clamp at 24.5 V min.
CS	4	Current sense input	-10	3.3	V	
PG_OUT	5	Power good output	-0.3	VCC	V	
PG_IN	6	Power good input	-0.3	3.0	V	Internal clamp at 3 V min.
FB	7	Feedback input	-0.3	3.0	V	Internal clamp at 3 V min.
COMP	8	OTA output	-0.3	5.3	V	Values referred to an externally forced condition
HV	10	High voltage input	-1	600	V	

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient	120	°C/W
P_{tot}	Power dissipation @Tamb = 50 °C	0.75	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

4 Electrical characteristics

T_j = -25 to 125 °C, V_{CC} = 15 V, C_{GD} = 1 nF unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_{CC}	Operating range	After turn-on	10		24.5	V
V_{CC_ON}	Turn-on threshold	Voltage rising(1)	13	14	15	V
V_{CC_OFF}	Turn-off threshold	Voltage falling (1)	8.5	9.0	9.5	V
$V_{CC\_HVSTUP\_OVP}$	Turn-on threshold of HVSTUP in OVP state	Voltage falling(1)	10.8	11.5	12.2	V
V_Z	V_{CC} clamp voltage	I_{VCC} = 20 mA(2)	24.5	26	27	V
SUPPLY CURRENT						
I_{START_UP}	Start-up current	Before turn-on, V_{CC} = 14 V		400	550	µA
I_Q	Quiescent current	$V_{FB} < V_{FB\_FF/EBM}$		0.6	0.8	mA
		V_{FB} = 2.5 V, $V_{COMP} < V_{COMP\_S}$		0.65	0.85	mA
		$V_{FB} > V_{FB\_S}$		0.65	0.85	mA
I_{CC}	Operating supply current	L4986A, $T_{ON} = T_{ON\_MIN}$(3)		2.2	2.8	mA
		L4986A, HV*T_{ON} = 1.3 ms(4)		3.8	4.7	mA
		L4986B, $T_{ON} = T_{ON\_MIN}$(3)		3.4	4.0	mA
		L4986B, HV*T_{ON} = 0.65 ms(4)		4.6	5.5	mA
I_{DIS}	Quiescent in disable	$V_{COMP} < V_{COMP\_DIS}$		450	600	µA
HIGH-VOLTAGE START-UP GENERATOR						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	800			V
V_{HV_START}	Start voltage	I_{VCC} < 100 µA	22	29	40	V
V_{CC_SO}	VCC switchover threshold		0.55	1	1.4	V
I_{HV_ON}	ON-state charge current	V_{HV} > 40 V, $V_{CC} < V_{CC\_SO}$	0.7	1	1.3	mA
		V_{HV} > 40 V, $V_{CC} > V_{CC\_SO}$, $V_{FB} < V_{FB\_HVSTUPOFF}$	5	7	10	mA
$V_{FB\_HVSTUPOFF}$	Generator shutdown threshold at FB pin		1.65	1.75	1.85	V
T_{TOUT}	Generator shutdown timeout	After V_{CC} exceeds V_{CC_ON} & $V_{FB} < V_{FB\_HVSTUPOFF}$	80	100	120	ms
I_{HV_OFF}	OFF-state current consumption	V_{HV} = 400 V		20	25	µA
AC BROWNOUT PROTECTION						
V_{HVPK_BO}	Brownout threshold	V_{HV} peak voltage falling(1)	94	100	106	V
V_{HVPK_BI}	Brown-in threshold	V_{HV} peak voltage rising(1)	103	110	117	V
T_{DB_ACBO}	Brownout debounce time		505	630	755	ms

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{DB_ACBI}	Brown-in debounce time	First time $V_{CC} > V_{CC\_ON}$	0.8	1	1.2	ms
			32	40	48	ms
X-CAPACITOR DISCHARGE FUNCTION						
V_{HV_MIN}	Peak residual voltage	$I_{HV\_DIS} > 5$ mA			45	V
I_{HV_DIS}	Discharge current	$V_{HV} = 45$ V	5			mA
T_{DECT_XCAP}	Detection time		51	64	77	ms
ERROR AMPLIFIER						
V_{REF}	Voltage feedback input threshold	$T_j = 25$ °C	2.47	2.5	2.53	V
		10 V < V_{CC} < 24.5 V(1)	2.45		2.57	V
I_{FB}	Input bias current	$V_{FB} = 0$ to 3 V	-0.1	0	0.1	µA
$V_{FBCLAMP}$	Internal clamp level	$I_{FB} = 1$ mA	3.0	3.3		V
gm	Transconductance gain	V_{REF} -150 mV < V_{FB} < V_{REF} +150 mV	160	200	240	µS
R_O	Output impedance		5			MΩ
I_{COMP}	Source current	$V_{COMP} = 3$ V, $V_{FB} = 1.9$ V	0.7	1	1.45	mA
	Sink current	$V_{COMP} = 3$ V, $V_{FB} = 3.0$ V	0.7	1	1.45	mA
V_{COMP}	Upper saturation voltage	$I_{SOURCE} = 0.2$ mA	5.0			V
	Lower clamp voltage	$V_{FB} = 3.0$ V	0.8		0.9	
DYNAMIC (D_OVP) and STATIC (S_OVP) OVERVOLTAGE PROTECTIONS						
V_{COMP_S}	Burst mode threshold S_OVP (Static OVP)	Voltage falling(1)	0.95	1.00	1.05	V
V_{COMP_R}	Restart threshold after S_OVP	Voltage rising(1)	1	1.05	1.1	V
V_{FB_S}	D_OVP disable threshold	10 V < V_{CC} < 24.5 V	2.595	2.675	2.755	V
V_{FB_R}	Restart threshold after D_OVP	10 V < V_{CC} < 24.5 V	2.44	2.55	2.65	V
DISABLE						
V_{COMP_DIS}	Disable threshold	Voltage falling(1)	0.65	0.7	0.75	V
V_{COMP_EN}	Enable threshold	Voltage rising(1)	0.85	0.9	0.95	V
I_{COMP_DIS}	Pull-up current at disable		8	12	16	µA
CURRENT SENSING						
I_{CS}	Leakage bias current	$V_{CS} = -0.5$ V		15	21	µA
		$V_{CS} = 0.235$ V	7.5	10	14	µA
V_{CS_OFS}	CS level shifter offset	CS = 0 V	3	10	17	mV
V_{CS_GAIN}	CS level shifter gain	C = -0.5 V	0.94	0.98	1.02	V/V
V_{CS_OCP1}	1st level Overcurrent threshold		-510	-490	-470	mV
T_{SS_OCP1}	1st level OCP threshold ramp up time		104	130	156	ms
T_{BLK}	Leading edge blanking	HV > 73 V rising	120	150	180	ns
		HV < 45 V falling	235	310	385	ns
$td_{(H-L)}$	Delay to output				110	ns
V_{CS_OCP2}	2nd level Overcurrent threshold		-0.80	-0.75	-0.70	V
V_{CS_ZCD}	Zero current threshold		-15	-10	-5	mV

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CURRENT SENSE DISCONNECTION						
V_{CSD}	Current Sense disconnection threshold	Voltage rising	165	200	235	mV
T_{CSD_DB}	Disconnection debounce time		8	10	12	µs
EQUIVALENT MULTIPLIER						
K_M	Equivalent multiplier gain	V_{HVPK} < 200 V(1)	0.405	0.44	0.475	V/V
		V_{HVPK} > 235 V(1)	0.092	0.10	0.108	V/V
THD CCM-OPTIMIZER						
K_{CCM}			0.51	0.55	0.59	H
FEEDBACK FAILURE PROTECTION/EXTERNAL BURST MODE (EBM)						
$V_{FB\_FF/EBM}$	Feedback failure protection (on FB) / External burst mode threshold	Voltage falling(1)	460	500	540	mV
		Hysteresis		50		mV
T_{FF/EBM_DB}	FFP/EBM debounce time		1.25	1.8	2.35	µs
I_{FB_EBM}	FB current during EBM	V_{FB} < $V_{FB\_FF/EBM}$	70	100	135	µA
	FB current at exit EBM	$V_{FB\_FF/EBM}$ < V_{FB} < V_{REF}	0.75	1	1.25	mA
SWITCHING FREQUENCY						
F_{SW}	Switching frequency (L4986A)	T_{ON} = 9µs, V_{HVPK} < 200 V	60	65	71	kHz
		T_{ON} = 3µs, V_{HVPK} > 235 V				
	Switching frequency (L4986B)	T_{ON} = 4.5µs, V_{HVPK} < 200 V	120	130	142	kHz
		T_{ON} = 1.5µs, V_{HVPK} > 235 V				
MAXIMUM ON-TIME						
T_{ON_MAX}	Maximum on-time	L4986A	32	40	50	µs
		L4986B	16	20	26	µs
MINIMUM OFF-TIME						
T_{OFF_MIN}	Minimum off-time	L4986A	0.75	1.0	1.35	µs
		L4986B	0.35	0.5	0.75	µs
GATE DRIVER						
V_{OL}	Output low voltage	I_{sink} = 200 mA			0.7	V
		I_{sink} = 5 mA			0.02	V
V_{OH}	Output high voltage	15V<VCC<24.5 V, I_{source} = 5mA	11	12	13	V
		V_{CC} = 9 V, I_{source} = 5 mA	7.85			V
I_{srcpk}	Peak source current			-0.7		A
I_{snkpk}	Peak sink current			1.5		A
t_f	Voltage fall Time	V_{GD} from 8 V to 1 V	3	7	15	ns
t_r	Voltage rise Time	V_{GD} from 1 V to 8 V	5	10	15	ns
	UVLO saturation	V_{CC} = 0 V to V_{CC_ON}, I_{sink} = 1mA			1.1	V
POWER GOOD						
V_{PGOOD_ON}	Power good turn-on threshold	Voltage falling(1)	2.300	2.375	2.450	V
V_{PGOOD_OFF}	Power good turn-off threshold	Voltage falling(1)	1.210	1.250	1.290	V
T_{PGOOD_DB}	Debounce time	Voltage rising on FB	40	50	60	µs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
		Voltage falling on PG_IN				
V_{PGOOD_CLAMP}	Clamp voltage PG_IN	I_{PG_IN} = 1 mA	3.0	3.3		V
I_{PG_IN}	Leakage	V_{PG_IN} > 200 mV		0.1	0.2	µA
$V_{PG\_OUT\_L}$	PG_OUT low voltage	I_{SINK} = 3 mA			0.28	V
I_{PG_OUT}	Leakage	V_{PG_OUT} = V_{CC} - 0.2 V			0.15	µA

1. *Parameters tracking each other.*
2. *The VCC pin is self-limited by an internal clamp when the device is in switching modality.*
3. *Equivalent to just before burst-mode condition.*
4. *Equivalent to full-load condition.*

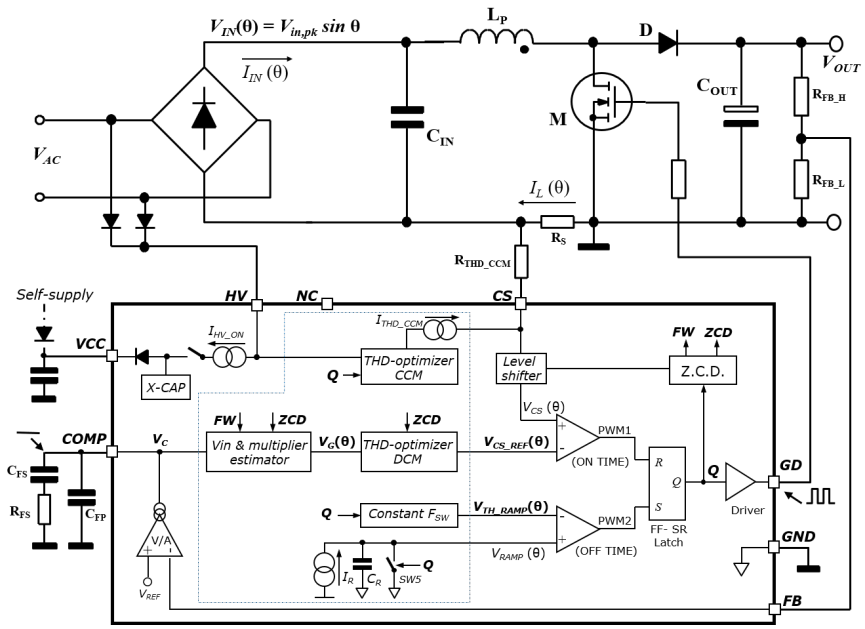
5 Application information

5.1 Theory of operation

The L4986A/B implements a conventional peak current mode control, based on fixed-off-time (FOT) control technique, with some proprietary circuitries that permit to ideally achieve the same performance of the more complex/expensive average current mode control.

Referring to Figure 4. Control loop connections, the power switch on-time (T_{ON}) is programmed by the output voltage control loop comparing the current sense signal V_{CS} with the internal current reference V_{CS_REF} in order to keep the V_{OUT} regulation; whereas the power switch off-time (T_{OFF}) is programmed by the "OFF-TIME modulator" circuitry in order to keep quasi-fixed the switching frequency F_{SW} in all operating conditions (see Section 5.2 OFF-time modulator for more details).

Figure 4. Control loop connections



The trans-conductance Error Amplifier V/A compares a portion of the output voltage V_{OUT}, brought at its inverting input externally available on pin FB via the resistor divider R_3-R_4, with an accurate internal reference V_{REF} (2.5 V typ.) connected to the non-inverting input, and generates an error signal V_C proportional to their difference. If the bandwidth of the error amplifier, essentially determined by the frequency compensation network connected between pin COMP and ground, is narrow enough – typically below 20 Hz – and a steady-state operation is assumed, the V_C error signal available at pin COMP can be regarded as a DC level, at least as a first approximation. The V_C voltage is then used by the "Vin & multiplier estimator" circuitry that, based also on the FW and ZCD signals (see Figure 5 and Figure 6 for more details), generates a voltage expressed by:

Equation 1

$$V_G\left(\theta\right) = V_C\ K_1\ \frac{V_{IN}(\theta)}{V_{OUT}} \quad (1)$$

where K_1 is the circuitry gain (constant term) and $V_{IN}(\theta) = V_{in,pk} sin\,\theta$ (with 0 ≤ θ ≤ π, as a result of the rectification operated by the input bridge) is the instantaneous line input voltage.

Equation 1 shows as the $V_G(\theta)$ voltage is proportional to the $V_{IN}(\theta)$ input voltage and to the V_C control voltage like in a standard current-mode PFC, but without using the standard multiplier block and without the AC line sensing.

The $V_G(\theta)$ voltage is then managed by the “THD-DCM optimizer” circuitry that acts as a simple gain (K_2) in CCM operation whereas in DCM operation opportunely shapes the $V_G(\theta)$ voltage in order to achieve ideally sinusoidal input current.

Considering the CCM operation, the $V_{CS\_REF}(\theta)$ voltage is then expressed by:

Equation 2

(2)

$$V_{CS\_REF}(\theta)^{CCM} = V_G\left(\theta\right)\ K_2 = \frac{K_M}{V_{OUT}} V_C\ V_{IN}\left(\theta\right)$$

where $K_M = K_1\ K_2$ is the equivalent multiplier gain (see Electrical characteristics table for details).

The internal current reference voltage $V_{CS\_REF}(\theta)$ is then compared with the current sense $V_{CS}(\theta)$ pin voltage (which is internally translated due to negative inductor current sensing) that is opportunely shaped by the “THD-CCM optimizer” in order to achieve sinusoidal input current in CCM operation.

In particular, referring to Figure 4 and Figure 5 during the power switch-on time the “THD-CCM optimizer” circuitry sources a current $I_{THD\_CCM}(\theta)$ to the CS pin, generating a voltage across the external R_{THD_CCM} resistor that is subtracted to the inductor current sense voltage $R_S\ I_L(\theta)$.

The resulting $V_{CS}(\theta)$ voltage, at external power switch turn-off condition, is then:

Equation 3

(3)

$$V_{CS}(\theta) = R_S\ I_{L,PK}(\theta) - R_{THD\_CCM}\ I_{THD_{CCM}}(\theta) = V_{CS\_REF}(\theta)$$

where the sourced $I_{THD\_CCM}(\theta)$ current is:

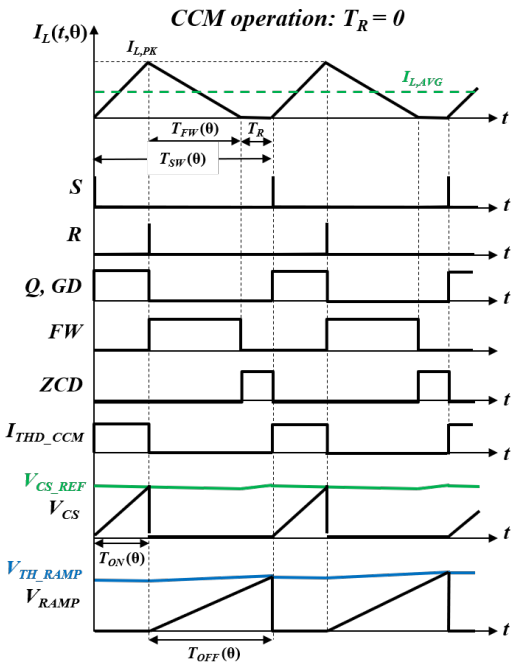
Equation 4

(4)

$$I_{THD\_CCM}(\theta) = \frac{L_P}{2\ K_{CCM}} \Delta I_L\left(\theta\right)$$

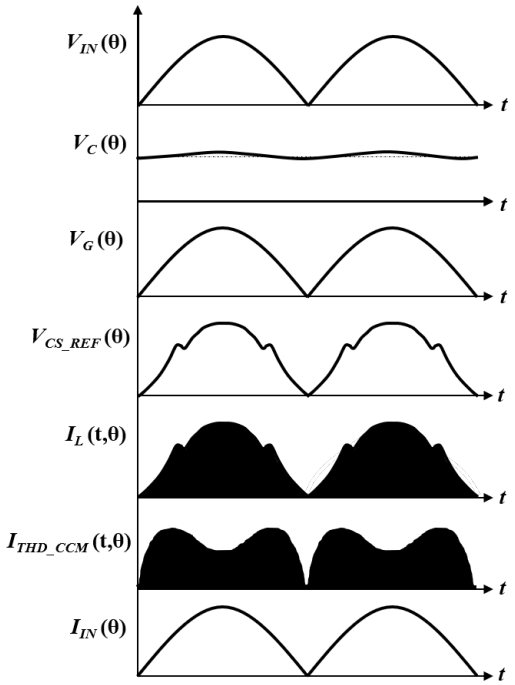
L_P is the inductor value, $\Delta I_L(\theta)$ is the inductor current ripple, K_{CCM} (0.55 typ.) is the circuitry gain.

Figure 5. Left key waveforms of the circuit in figure 4 – Switching cycle time scale



Switching cycle time scale

Figure 6. Right key waveforms of the circuit in figure 4 – Line cycle time scale



Line cycle time scale

Now considering that the input current $I_{IN}(\theta)$ of the converter is the average value of the inductor current in a switching cycle results:

Equation 5

$$I_{IN}(\theta)^{CCM} = I_{L,PK}(\theta) - \frac{\Delta I_L(\theta)}{2} \quad (5)$$

Selecting the THD-CCM optimizer resistor equal to:

Equation 6

$$R_{THD\_CCM} = K_{CCM}\frac{R_S}{L_P} \quad (6)$$

and replacing equations #2 and #4 in equation #3, after some calculations the inductor peak current results:

Equation 7

$$I_{L,PK}(\theta) = \frac{1}{R_S}\frac{K_M}{V_{OUT}} V_C \; V_{IN}(\theta) + \frac{\Delta I_L(\theta)}{2} \quad (7)$$

Finally, replacing equation #7 in equation #5, the input current of the converter results:

Equation 8

$$I_{IN}(\theta)^{CCM} = \frac{1}{R_S}\frac{K_M}{V_{OUT}} V_C \; V_{IN}(\theta) \quad (8)$$

which is sinusoidal and in phase with the $V_{IN}(\theta)$ input voltage (ideally zero-THD and unity-PF).

Considering the DCM operation (T_R>0), through geometrical consideration, the input current $I_{IN}(\theta)$ of the converter can be expressed by:

Equation 9

$$I_{IN}(\theta)^{DCM} = \frac{1}{2} I_{L,PK}(\theta)\frac{T_{ON}(\theta) + T_{FW}(\theta)}{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)} \quad (9)$$

Equation #9 shows that the term TR>0 introduces distortion if $I_{L,PK}(\theta)$ has a sinusoidal shape like in a standard PFC. Referring to Figure 4, the sinusoidal voltage $V_G\left(\theta\right) = V_C \; K_1 \; \frac{V_{IN}(\theta)}{V_{OUT}}$ is then opportunely shaped by the "THD-DCM" optimizer block, which generates the current reference voltage expressed by:

Equation 10

$$V_{CS\_REF}(\theta)^{DCM} = V_G(\theta)\frac{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)} \quad (10)$$

Replacing equation #1 in equation #10, and considering that in DCM operation the peak of the inductor current is $I_{L,PK}(\theta) = \Delta I_L(\theta)$, after some calculations results:

Equation 11

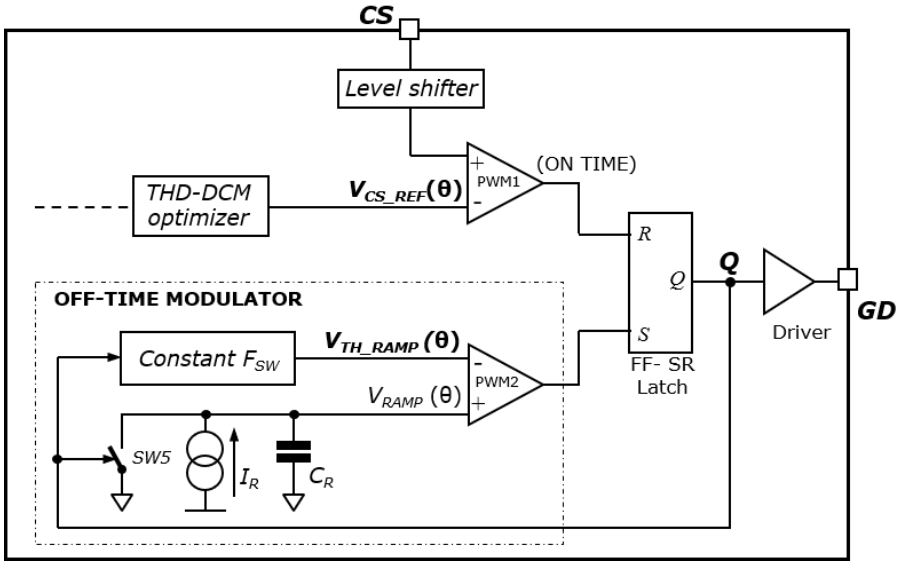
$$I_{IN}(\theta)^{DCM} = \frac{1}{R_S}\frac{K_M}{V_{OUT}} V_C \; V_{IN}(\theta) \quad (11)$$

which is sinusoidal and in phase with the $VI_N(\theta)$ input voltage (ideally zero-THD and unity-PF), and it has the same gain like in CCM operation.

5.2 OFF-time modulator

The device embeds a novel OFF-time modulator which is able to achieve quasi-fixed switching frequency in all operating conditions (CCM and DCM operation) and independent from the input/output voltage, the load conditions and the converter's parasitic as the existing modulators.

Figure 7. **OFF-time modulator - details**



Referring to Figure 7 , once the power switch ON-time is ended (Q signal goes low) the internal switch SW5 is open and the constant current generator I_R starts to charge linearly the capacitor C_R. The resulting voltage V_{RAMP} is compared with the voltage V_{TH_RAMP}, which is generated by the “Constant F_{SW}” circuitry based on the Q signal duration (T_{ON}). As soon as the ramp voltage V_{RAMP} reaches the V_{TH_RAMP} voltage, the flip-flop is set and the external power switch is turned on (Q signal goes high).

In other words, the power switch off-time (T_{OFF}) is modulated based on the on-time information (T_{ON}) to keep cycle-by-cycle constant the resulting switching frequency ($F_{SW}=1/T_{SW\_TARGET}$):

$T_{OFF} = T_{SW\_TARGET} - T_{ON}$.

Figure 8. **Left OFF-time modulator timing – Line cycle time scale**

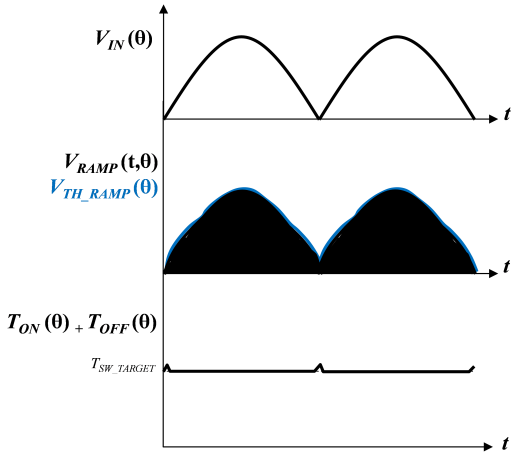
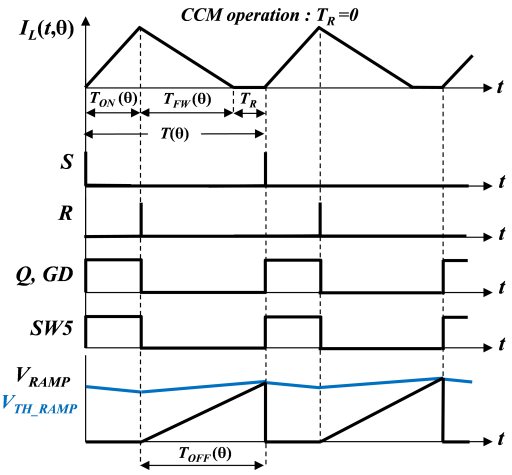


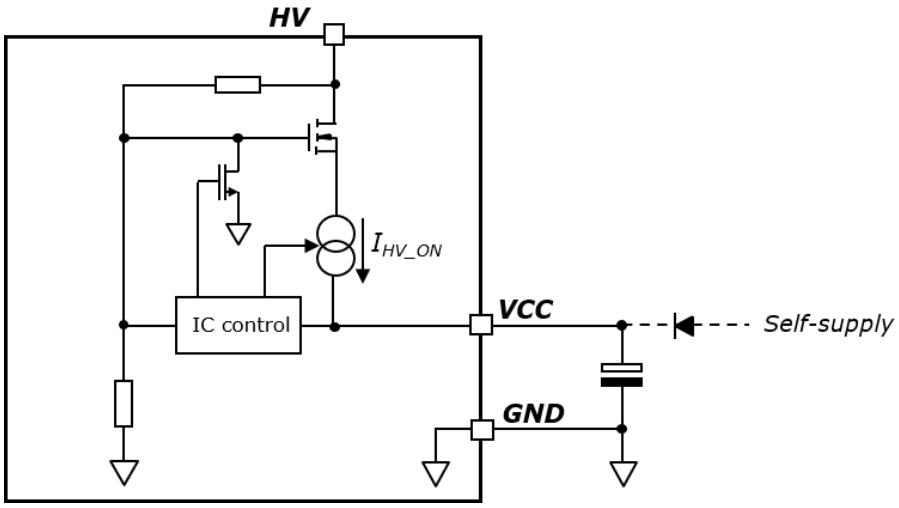
Figure 9. **Right OFF-time modulator timing – Switching cycle time scale**



5.3 High voltage startup

The device embeds a High Voltage (HV) start-up circuitry, based on a high voltage N-channel FET as shown in Figure 10, in order to supply the IC during the initial start-up phase before the self-supply winding is operating.

Figure 10. **Embedded high voltage start-up circuitry**



As soon as the voltage on the HV pin is higher than V_{HV_START} (29 V typ.), the HV start-up circuitry turns on and starts to source an I_{HV_ON} current (7 mA typ.). This current, minus the device consumption I_{START_UP} before startup (400 µA typ.), charges the external bypass capacitor connected between VCC pin and ground increasing its voltage almost linearly up to the device turn-on threshold V_{CC_ON} (14 V typ.). To protect the HV-start-up circuitry from excessive power consumption, e.g. for a short-circuit on the VCC pin, the I_{HV_ON} current sourced is 1 mA typical till the VCC pin voltage is lower than V_{CC_SO} (1 V typ.).

Once the VCC pin voltage reaches V_{CC_ON} the device starts operating and to guarantee a reliable startup of the system, the HV current generator I_{HV_ON} is kept on till the output voltage reaches 70% typ. of the programmed value (FB pin higher than V_{FB_HVSTUP} threshold). To protect the HV-start-up circuitry from excessive power consumption, e.g. in case of an overcurrent request, the HV current generator is in any case automatically turned off after the T_{TOUT} timeout (100 ms typ.)

After the start-up phase, the system application should guarantee $V_{CC} > V_{CC\_OFF}$. In fact, if the VCC pin voltage drops to V_{CC_OFF} the device shutdown and the HV-start-up is turned on to bring the VCC pin to a voltage V_{CC_ON} and restart the operations performing the soft-start.

5.4 Input line discharge (X-cap discharge function)

In order to guarantee the safety regulations such as IEC 61010-1/IEC 62368-1 without using the traditional discharge resistor in parallel to the X-capacitor, and thus saving also the associated power losses enabling ultra-low consumption in standby conditions, the device embeds an internal logic circuit that detects when the unit has been detached from the power line; if this event occurs then the high voltage start-up generator is turned on to discharge the X capacitors of the EMI filter to a safe level.

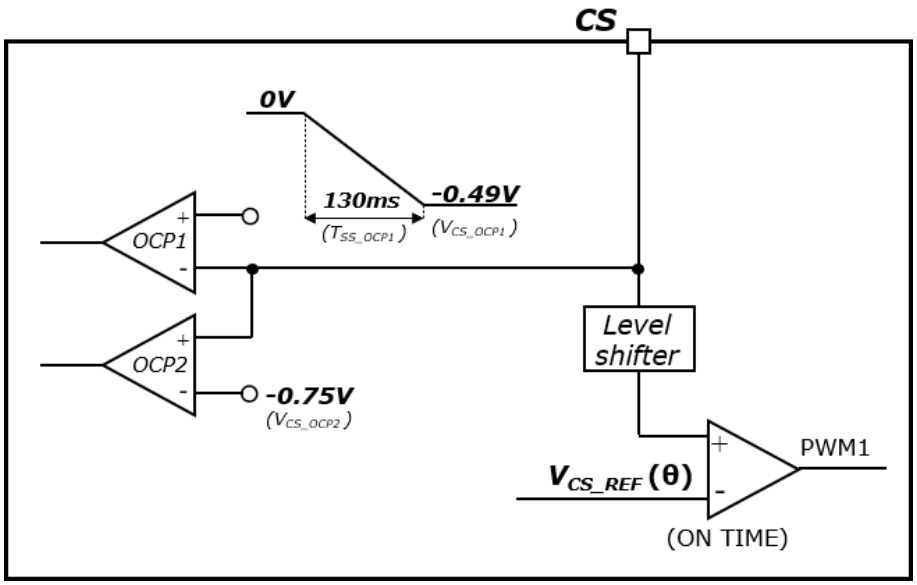
In particular, after a detection time T_{DECT_XCAP} (64 ms typ.) from the AC mains disconnection, the X-cap discharge operation is triggered and the internal HV current generator is turned on: a discharge current I_{HV_ON} (5 mA minimum) is drawn from the HV pin ensuring the X-cap discharge until the voltage on the HV pin falls below a safe level (45 V maximum, V_{HV_MIN} parameter in Section 4 Electrical characteristics, Table 5), within the regulation maximum discharging time.

5.5 Soft-start

To limit the in-rush current of the converter at the startup, the device implements a soft startup increasing the peak of the inductor current from zero up to the required value programmed by the control loop to regulate the output voltage.

In particular, the device changes the reference threshold of the first overcurrent comparator (OCP1) from zero up to V_{CS_OCP1} (-0.49 V typ.) in T_{SS_OCP1} time (130 ms typ.), as shown in Figure 11.

Figure 11. **Soft-start circuitry details**



5.6 No load operation (burst-mode function)

To avoid uncontrolled rise of the output voltage at light or zero load, when $V_{COMP} < V_{COMP\_S}$ (1 V typ.) the device stops the switching activity and reduces its power consumption. As soon as the $V_{COMP} > V_{COMP\_R}$ (1.05 V typical and in tracking with the threshold V_{COMP_S}) the device restarts the switching activity.

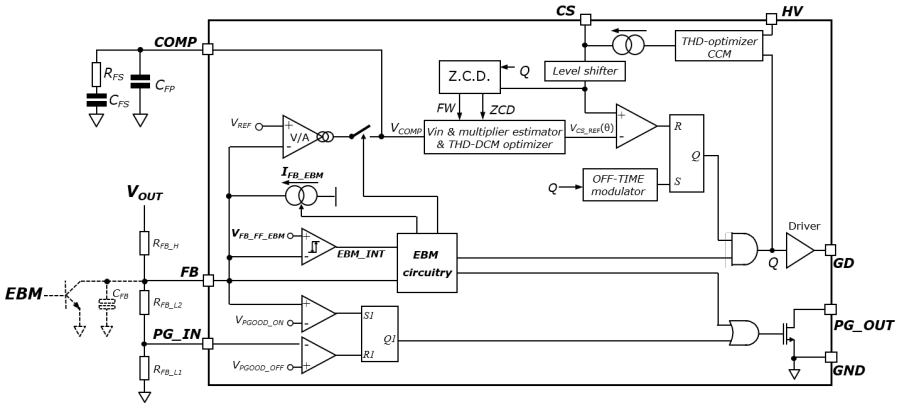
If the burst-mode condition is triggered when the gate driver GD is “high”, the device completes the current ON-time and the system stoppage takes place after GD falling edge.

During the burst-mode operation, the system application should guarantee $V_{CC} > V_{CC\_OFF}$. In fact, if the VCC pin voltage drops down to V_{CC_OFF}, the device shutdown and the HV-startup is turned on to bring the VCC pin to a voltage V_{CC_ON} and restart the operation performing the soft-start.

5.7 Idle operation (external burst-mode function)

The FB pin can be used to implement an external burst-mode (EBM), forcing the pin lower than the internal threshold $V_{FB\_FF/EBM}$ (500 mV typ.): the switching activity is stopped and the IC power consumption is reduced (Error Amplifier is also turned off and the COMP pin is forced to “high impedance”). The device restarts switching, without implementing the soft-start, as soon as the FB voltage exceeds the $V_{FB\_FF/EBM}$ threshold by 50 mV typ. De-bounce time T_{FF/EBM_DB} (1.8 µs typ.) is provided to avoid false triggering. Referring to Figure 12, it is worth noting that as soon as the device enters the EBM state (the internal signal EBM_INT is high) a weak pull-up current I_{FB_EBM} (100 µA typ.) is sourced from the FB pin in order to speed up the FB voltage rising edge when the external pull-down is released. In addition, once the FB voltage exceeds $V_{FB\_FF/EBM}$ + 50 mV the I_{FB_EBM} current of 100 µA is increased to 1 mA till the FB pin voltage reaches the final target of 2.5 V (internal V_{REF}). When using the EBM function, the suggested value of the FB filter capacitor C_{FB} is 3.3 nF.

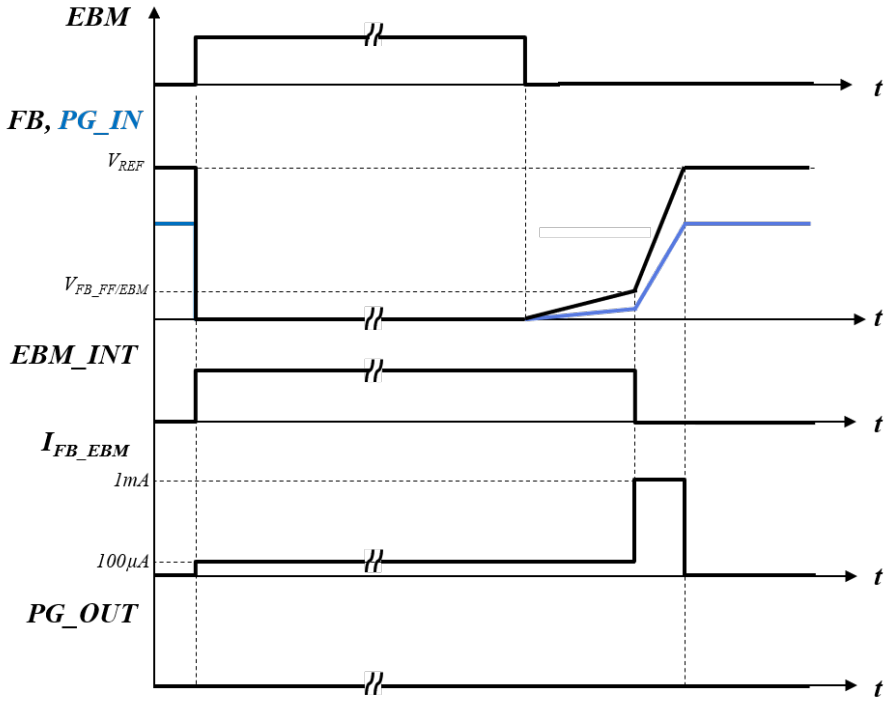
Figure 12. **External Burst-Mode (EBM) function – circuit details**



During the external burst-mode condition (FB < $V_{FB\_FF/EBM}$), the system application should guarantee V_{CC} > V_{CC_OFF} to minimize the power consumption. In fact, in case the VCC pin voltage approaches the device turn-off threshold the internal HV-start-up is turned on to bring V_{CC} voltage to the turn-on threshold V_{CC_ON}.

It is also worth noting that during this condition the PG_OUT state is “frozen” to avoid false PGOOD deactivation (PG_IN is proportional to FB pin that is forced low).

Figure 13. **External Burst-Mode (EBM) function – timing**

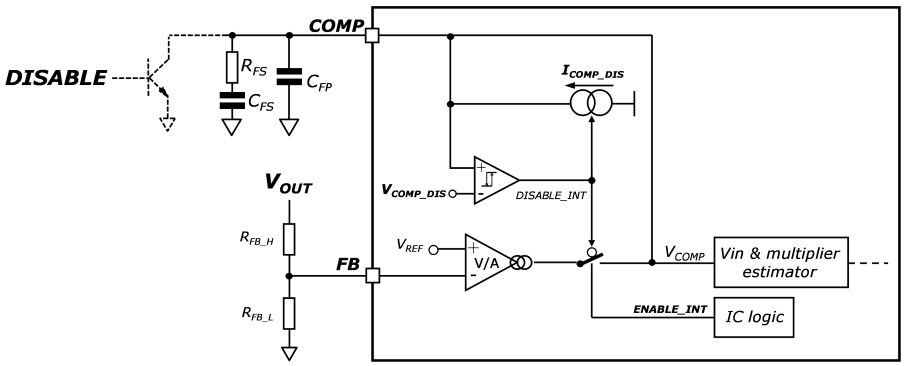


5.8 Disable operation (DISABLE function)

Forcing the COMP pin lower than the internal threshold V_{COMP_DIS} (0.7 V typ.), the device stops the operation and enters into low power consumption. The Error Amplifier is turned off and a weak internal pull-up current I_{COMP_DIS} (10 µA typ.) is activated. De-bounce time $T_{COMP\_DIS\_DB}$ (50 µs typ.) is provided to avoid false triggering.

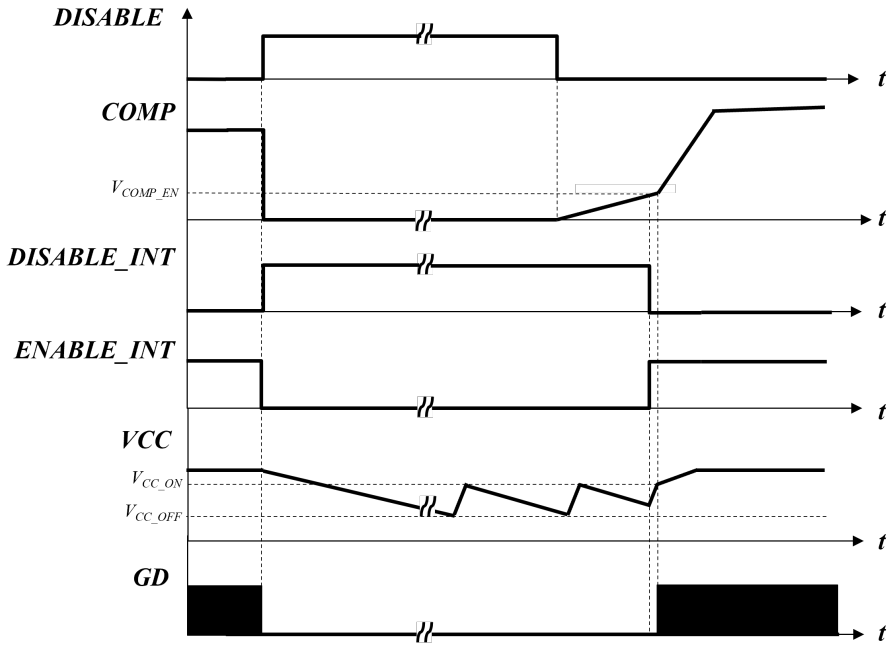
Referring to Figure 14, releasing the external pull-down the internal pull-up current I_{COMP_DIS} charges the compensation network connected between COMP pin and ground and the COMP voltage starts to increase. As soon as the COMP pin reaches the enable threshold V_{COMP_EN} (0.9V typ.), the device turns on the internal HV-startup current generator to bring VCC voltage to the turn-on threshold V_{CC_ON} and restarts the operation implementing the soft-start.

Figure 14. DISABLE function – circuit details



During the disable condition, due to the absence of energy transferred from the auxiliary winding, the internal HV-startup is intermittently turned on to keep the device supplied between V_{CC_OFF} and V_{CC_ON}.

Figure 15. DISABLE function – timing



5.9 Power Good (PGOOD function)

The PG_IN is an adjustable input comparator suitable for monitoring the PFC output voltage and, accordingly, driving a logic signal exiting from PG_OUT pin (open drain).

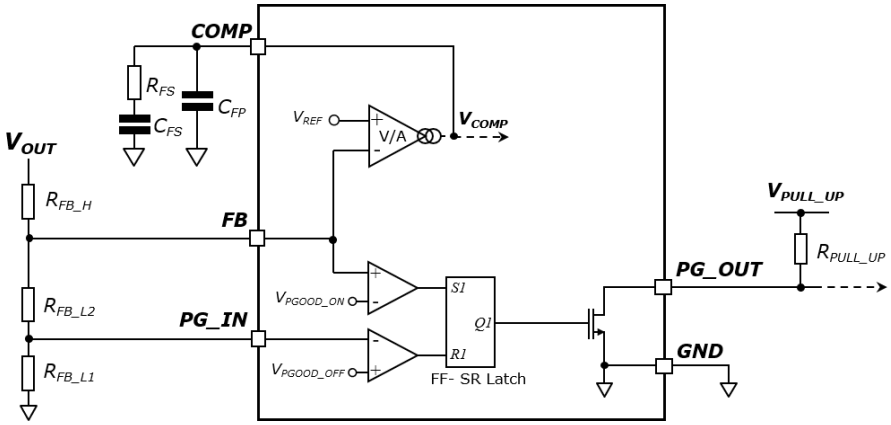
The PG_OUT is actively pulled to ground once the IC is turned on and the FB pin voltage exceeds the internal threshold V_{PGOOD_ON} (2.375 V typ.). Then, as soon as the PG_IN input voltage is lower than the internal threshold V_{PGOOD_OFF} (1.250 V typ.), the PG_OUT pin is set to high impedance.

De-bounce time T_{PGOOD_DB} (50 µs typ.) is provided to avoid false activation / deactivation.

The PGOOD functionality is also linked to the operating status: PG_OUT is set to high impedance if the device detects the CS disconnection.

Monitoring of the output voltage can be realized using the same resistors divider used to program the output voltage V_{OUT}, as shown in Figure 16.

Figure 16. PGOOD connections



As soon as the VCC pin reaches the V_{CC_ON} turn-on threshold, the device starts up and the PG_OUT pin is internally pulled-low as soon as the output voltage reaches 95% of the programmed voltage V_{OUT} (e.g. V_{PGOOD_ON} = 2.375 V vs. V_{REF} = 2.500 V target reference of the output voltage control loop).

Once the PG_OUT pin is pulled low the device starts to monitor the PG_IN pin voltage, which is proportional to the output voltage.

Equation 12

(12)

$$V_{PG\_IN} = V_{OUT}\frac{R_{FB\_L1}}{R_{FB\_H} + R_{FB\_L}}$$

where R_{FB_H} and R_{FB_L}= R_{FB_L1} + R_{FB_L2} resistors are previously selected to program the desired nominal output voltage V_{OUT_NOM}.

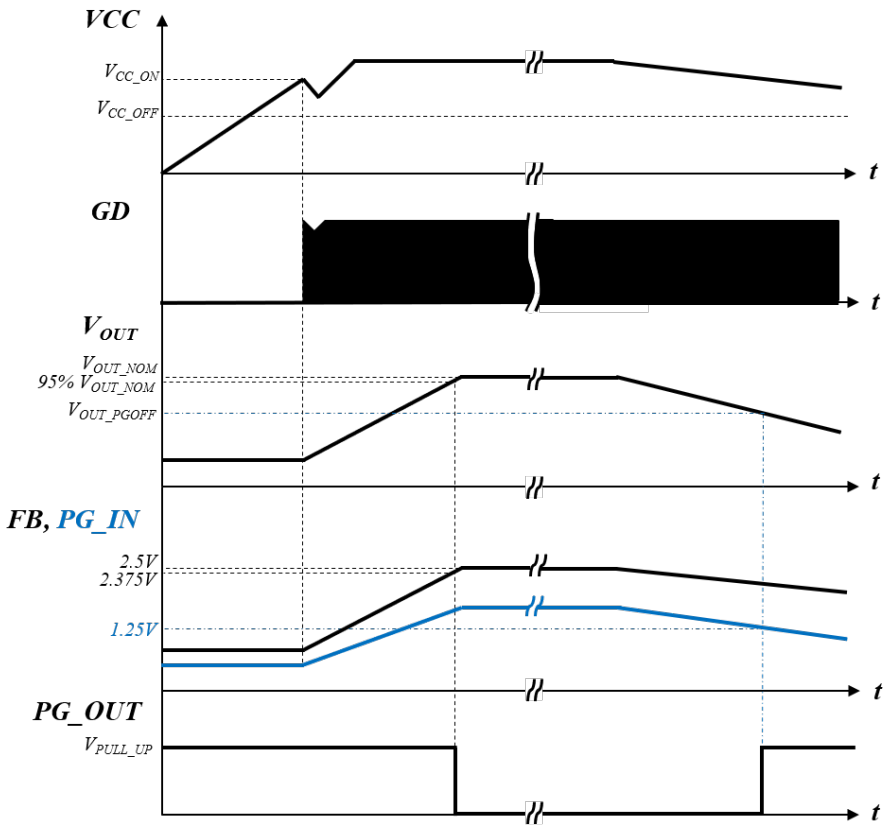
As soon as the PG_IN input voltage becomes lower than the internal threshold V_{PGOOD_OFF} (1.250 V typ.), the PG_OUT is deactivated: the corresponding output voltage V_{OUT_PGOFF} can be then programmed selecting opportunely the R_{FB_L1} resistor:

Equation 13

(13)

$$R_{FB\_L1} = \frac{V_{PGOOD\_OFF}}{V_{OUT\_PGOFF}}\left(R_{FB\_H} + R_{FB\_L}\right)$$

Figure 17. **PGOOD timing**



5.10 Protections

A comprehensive set of protections is embedded to ensure a high level of reliability of the final application without adding extra components and/or circuitry.

5.10.1 AC brown-in (BI function)

At startup, as soon as the VCC pin voltage reaches the V_{CC_ON} turn-on threshold the device monitors the AC line input voltage through the HV pin and starts the operation if the input voltage is higher than the V_{HVPK_BI} brown-in threshold (around 81 Vac). After the first startup, in case of a brown-out/brown-in cycle, as soon as the brown-in is detected the internal HV-startup is turned on to bring VCC voltage to the turn-on threshold V_{CC_ON}.

De-bounce time T_{DB_ACBI} of 1 ms typ. is provided to avoid false triggering at the first startup. After that, the de-bounce time is increased to 40 ms.

5.10.2 AC brownout (BO function)

During the normal operation, in order to protect the PFC pre-regulator from excessive RMS current, if the AC line voltage falls below the V_{HVPK_BO} brownout threshold (around 71 Vac) for at least 630 ms typ. (see T_{DB_ACBO} parameter in Table 5. Electrical characteristics), the switching activity is stopped.

5.10.3 Output overvoltage (OVP function)

To limit an output voltage overshoot, e.g. due to a heavy load release or at startup with light-load, the device stops the switching activity as soon as the instantaneous output voltage V_{OUT} is higher than 7% typ. in respect to the programmed value.

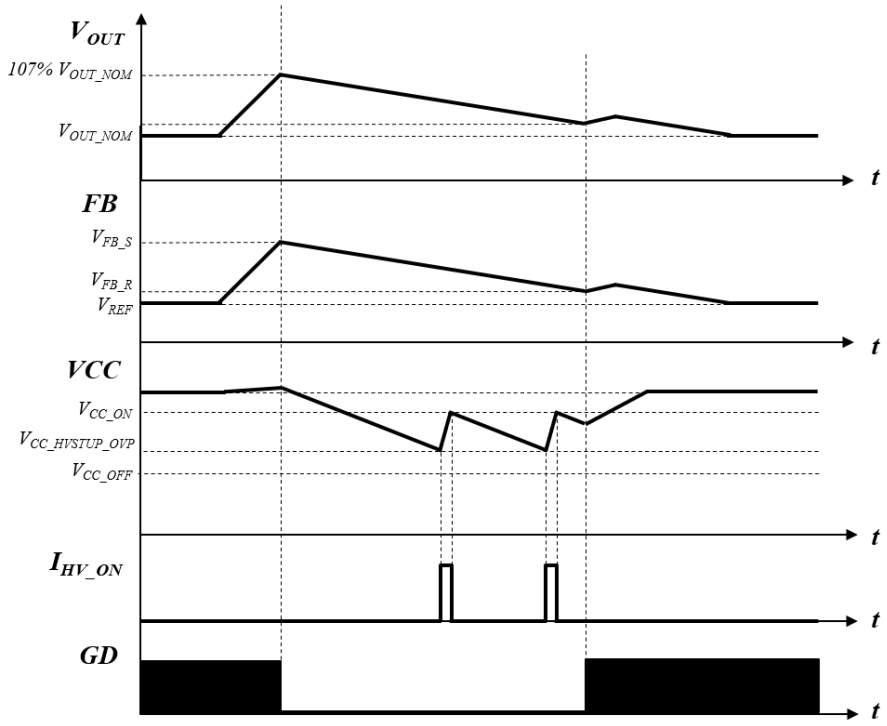
In fact, the device detects an overvoltage condition monitoring the FB pin which is proportional to the instantaneous value of the output voltage VOUT and in steady-state conditions sits at the internal reference of the error amplifier (V_{REF} = 2.5 V).

As soon as the FB voltage exceeds the steady-state value by 7% (VFB > VFB_S), the switching activity is stopped until it gets back close to it ($V_{FB} < V_{FB\_R}$).

De-bounce time T_{DOVP_DB} (50 µs typ.) is provided to avoid false activation of the protection.

During the OVP condition, to avoid undesired IC shutdown, as soon as the VCC pin voltage falls below the $V_{CC\_HVSTUP\_OVP}$ threshold (11.5 V typ.) the internal HV-startup is turned on to bring V_{CC} voltage to the turn-on threshold V_{CC_ON}.

Figure 18. OVP timing



5.10.4 Overcurrent (OCP1 function)

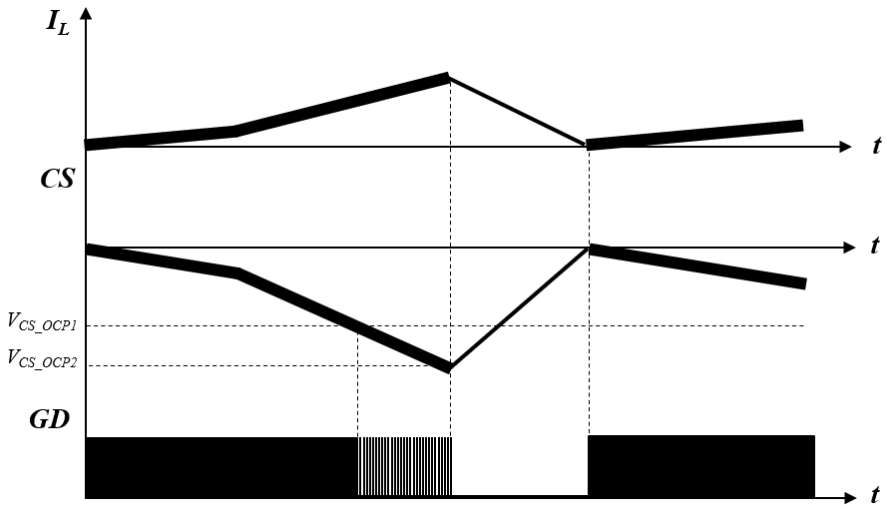
To limit the peak inductor current in case of extra request (e.g. heavy load changes), the device implements a cycle-by-cycle overcurrent protection. The device monitors the CS pin during the power switch on-time and as soon as the voltage on the CS pin goes below V_{CS_OCP1} (-0.49 V typ.), the internal overcurrent comparator is triggered and terminates the conduction cycle of the power switch before the normal PWM circuit does. In this way, the peak inductor current is limited to a maximum of $0.49/R_S$.

5.10.5 Inductor saturation detection (OCP2 function)

A second overcurrent level set at V_{CS_OCP2} (-0.75 V typ.) detects abnormal current values (e.g. due to boost inductor saturation) and, on this occurrence for two consecutive switching cycles, activates a safety procedure that immediately stops the converter activity until the current level reaches the zero-current threshold (V_{CS_ZCD}).

The zero-current threshold monitor allows safe operations also during current surges occurring at power-up or after a mains dip or missing cycle; in fact it allows switching start/restart only when the overcurrent event is definitively over.

Figure 19. **OCP2 timing**



5.10.6 Feedback failure detection

The device handles the possible disconnection of both output voltage feedback and input current monitoring. At startup, as soon as the VCC pin voltage reaches the V_{CC_ON} turn-on threshold, the device checks the FB and CS pins:

- if the FB pin voltage is lower than the internal $V_{FB\_FF/EBM}$ threshold (0.5 V typ.) a failure of the output divider resistor is assumed (e.g. R_{FB_H} resistor not mounted), then the device stops the switching activity and reduces its consumption.
  - De-bounce time T_{FF/EBM_DB} (1.8µs typ.) is provided to avoid false triggering.
- if the CS pin voltage is higher than the internal V_{CSD} threshold (200 mV typ.) a failure of the current sensing resistors is assumed (e.g. R_{THD_CCM} resistor not mounted and/or R_S resistor burned), then the device stops the switching activity and reduces its consumption. A recycle of V_{CC} between the turn-off threshold (V_{CC_OFF}) and the turn-on threshold (V_{CC_ON}) is needed to restart the converter.
  - De-bounce time T_{CSD_DB} (10 µs typ.) is provided to avoid false triggering .

5.11 Line feedforward

To keep the maximum output power deliverable by the converter almost constant with respect to the AC input voltage, a two-level discrete voltage feedforward is integrated in the controller. Basically, the AC input voltage is monitored through the HV pin and internally compared with a fixed threshold to properly set the value of equivalent multiplier gain K_M (see Table 5. Electrical characteristics for details). The proper operation of the converter, with the right K_M multiplier gain, is guaranteed for an AC input voltage below 142 Vrms and above 166 Vrms.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SSOP10 package information

Figure 20. **SSOP10 package dimensions**

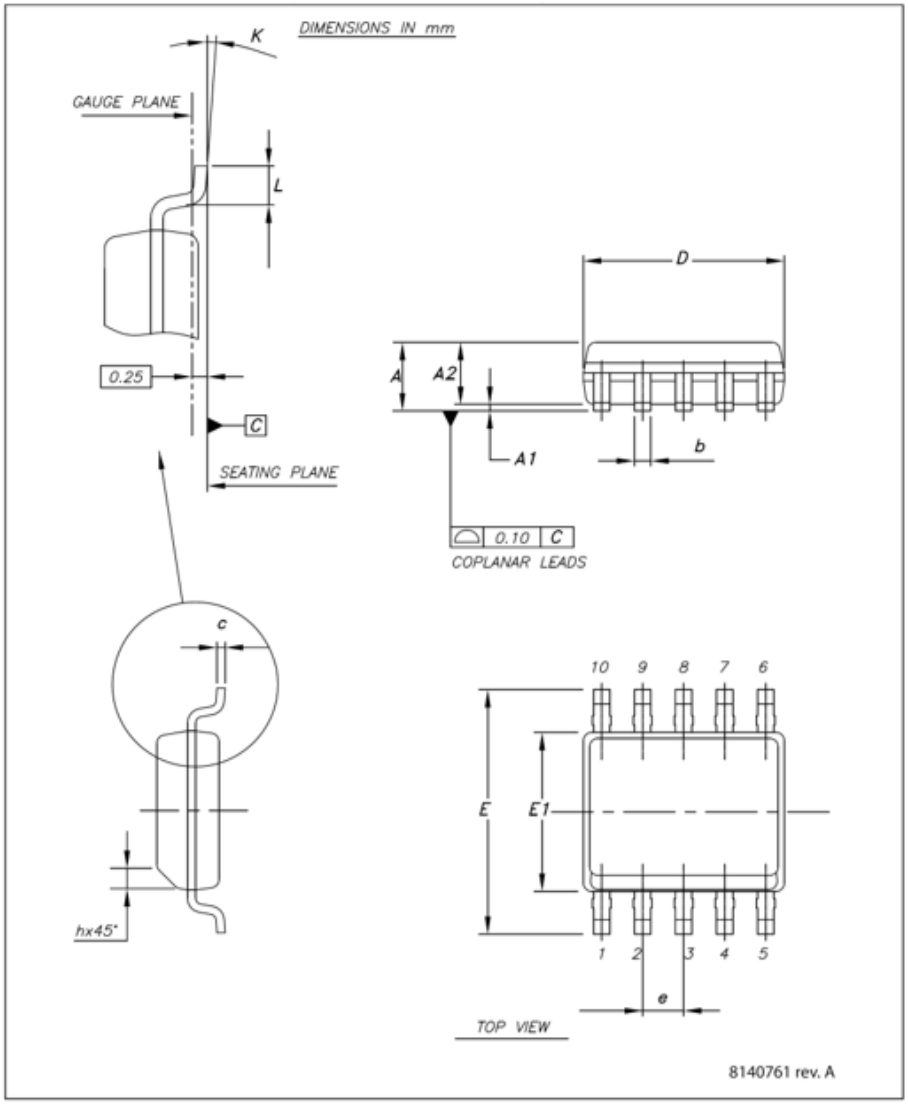


Table 6. **SSO10 package mechanical data**

Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25

Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e	-	1	-
h	0.25	-	0.50
L	0.40	-	0.90
K	0°	-	8°

7 Ordering information

Table 7. **Order codes**

Order code	Package	Package marking	Packaging
L4986A	SSOP10	L4986A	Tube
L4986B	SSOP10	L4986B	Tube
L4986ATR	SSOP10	L4986A	Tape and reel
L4986BTR	SSOP10	L4986B	Tape and reel

Revision history

Table 8. **Document revision history**

Date	Version	Changes
26-Jul-2021	1	Initial release.
11-Aug-2021	2	Updated Table 5. Electrical characteristics
20-Dec-2021	3	Updated V_{HVPK_BI} parameter value in Table 5 and Application Information section.

Contents

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