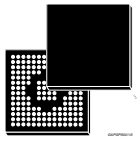
STA680

HD Radio™ baseband receiver

Datasheet - production data

LQFP144
(20x20x1.4 mm)



LFBGA 168 balls
(12x12x1.4 mm)

Features

- IBOC (in-band on-channel) digital audio broadcast signal decoding for AM/FM hybrid and all-digital modes
- Dual-channel HD 1.5 for background scanning and data services
- HD codec (HDC) audio decompression
- Metadata support for HD Radio reception
- MPS (main program service), SPS (supplemental program service) and PAD (program associated data) data decoding
- Advanced HD Radio feature support:
  - Conditional access (CA)
  - Apple ID3 tag
  - Multicasting
  - Electronic program guide (EPG)
  - Real-time traffic
  - Audio time shifting
- Variable input base-band data-rate I2S-like interface supporting 650, 675, 744.1875, 882, 912 kS/s data rates
- Secondary RF base-band interface for dual tuner applications
- Glueless interface to Synchronous SDRAM addressing up to 512 Mbit of SDRAM in x16 configuration
- Optional Serial Flash memory SPI interface for application code storage
- IIS serial audio interface with programmable sample rate converter
- Primary and secondary serial interfaces for based on industry standard IIC and SPI
- Several General purpose IOs
- One Internal clock oscillator and two internal PLLs
- External clock input
- 1.2 V core supply; 3.3 V I/O supply
- Automotive qualified in accordance with AEC-Q100

Description

The STA680 is an HD-radio base-band processor for car-radio applications. The STA680 functionality includes audio decompression and data processing, while multiple interfaces ensure flexible integration into the system.

The STA680 takes full advantage of HD 1.5 Radio benefits including CD-like audio quality from HD Radio FM broadcasts and FM-like audio quality using HD Radio AM, while program associated data or traffic information is received from the second channel.

Table 1. Device summary

Order code	Package[1]	Packing
STA680	LFBGA 168 balls (12x12x1.4 mm)	Tray
STA680TR	LFBGA 168 balls (12x12x1.4 mm)	Tape & Reel
STA680Q	LQFP144 (20x20mm)	Tray

1. ECOPACK® compliant.

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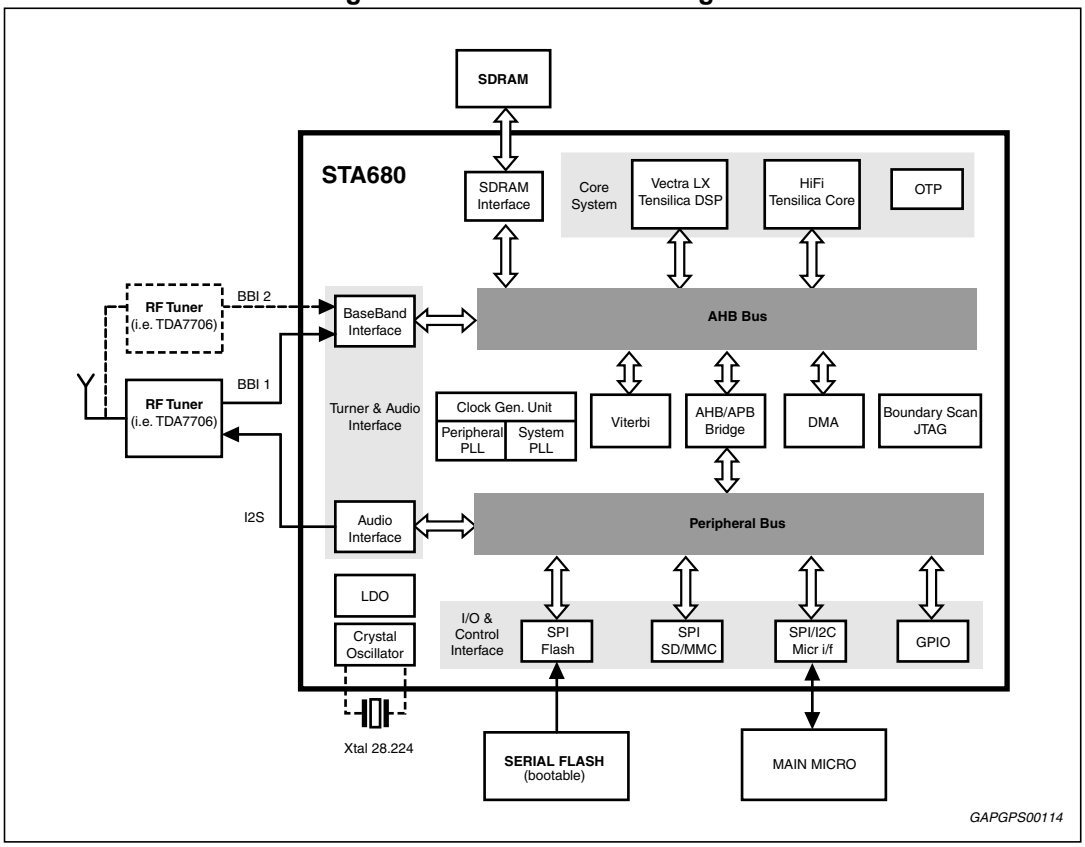
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



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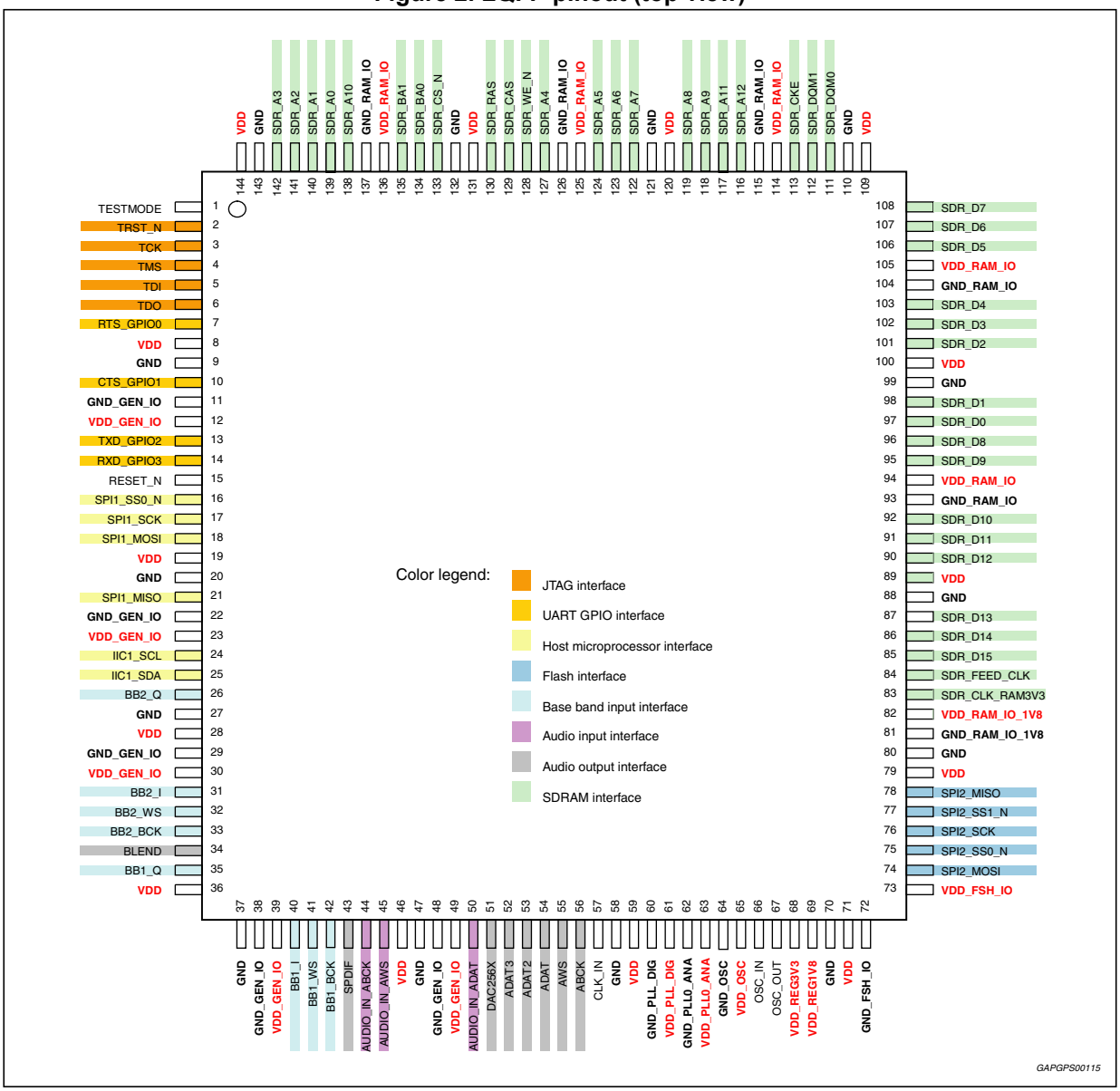
1.2 Pin description

The STA680 is available in two different packages targeting different application cost and complexity. It comes both in a 20x20mm LQFP package with 144 pins, and in a 12x12mm LFBGA with 168 balls with 0.8mm pitch.

1.2.1 LQFP description

Figure 2 presents the pinout of the STA680 for the LQFP package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 1.2.3*.

Figure 2. LQFP pinout (top view)



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1.2.2 LFBGA description

Figure 3 presents the ball-out of the STA680 for the LFBGA package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 1.2.3*.

Figure 3. LFBGA ball-out (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		GPIO6	BB2_BCK	BB2_I	GND_GEN_IO	IIC1_SDA	SPI1_MISO	SPI1_SCK	RESET_N	TXD_GPIO2	RTS_GPIO0	VDD_GEN_IO	TESTMODE	
B	GPIO5	BB1_Q	BLEND	BB2_WS	GND_GEN_IO	BB2_Q	IIC1_SCL	SPI1_MOSI	SPI1_SS0_N	RXD_GPIO3	CTS_GPIO1	VDD_GEN_IO	SDR_A3	TRST_N
C	BB1_WS	BB1_I	ADAT2	IIC2_SDA	GPIO7	IIC2_SCL	IIC1_DA	SPI3_MOSI	SPI3_MISO	SPI3_SCK	TDI	TCK	SDR_A1	SDR_A2
D	VDD_GEN_IO	VDD_GEN_IO	BB1_BCK	IIC2_DA	VDD	VDD			SPI3_SS_N	GPIO4	TDO	TMS	SDR_A10	SDR_A0
E	AUDIO_IN_ ABCK	SPDIF	ADAT3	VDD_PLL_DIG							VDD	MODEOP_FSH	SDR_BA0	SDR_BA1
F	AUDIO_IN_ ADAT	AUDIO_IN_ AWS	GND_PLL_ DIG	GND_PLL_ DIG		GND	GND	GND	GND		VDD	MODEOP_GEN	SDR_RAS_N	SDR_CS_N
G	AWS	ADAT	DAC256X			GND	GND	GND	GND			SDR_CAS_N	SDR_WE_N	VDD_RAM_IO
H	GND_GEN_IO	GND_GEN_IO	ABCK			GND	GND	GND	GND			SDR_A4	SDR_A5	GND_RAM_IO
J	VDD_OSC	GND_OSC	GND_PLL1_ ANA	GND_PLL0_ ANA		GND	GND	GND	GND		VDD	VDD	SDR_A7	SDR_A6
K	OSC_OUT	CLK_IN	VDD	VDD_REG3V3							VDD	VDD	SDR_A9	SDR_A8
L	OSC_IN	GND_OSC	VDD	VDD_REG3V3	VDD_FSH_IO	GND_FSH_IO			VDD_RAM_IO _1V8	GND_RAM_IO _1V8	GND_RAM_IO	GND_RAM_IO	SDR_A12	SDR_A11
M	VDD_PLL1_ ANA	VDD_PLL0_ ANA	SPI2_SS1_N	SPI2_SS2_N	SPI2_SS3_N	RFU	SDR_D13	SDR_D10	VDD_RAM_IO	VDD_RAM_IO	GND_RAM_IO	GND_RAM_IO	SDR_DQM1	SDR_CKE
N	VDD_REG1V8	VDD_REG1V8	SPI2_MOSI	SPI2_SCK	SDR_CLK_ RAM3V3	SDR_D15	SDR_D12	SDR_D9	SDR_D0	SDR_D2	SDR_D4	SDR_D6	SDR_DQM0	
P			SPI2_SS0_N	SPI2_MISO	SDR_FEED_ CLK	SDR_D14	SDR_D11	SDR_D8	SDR_D1	SDR_D3	SDR_D5	SDR_D7		

Color legend:

Ball unused
Ball not present
JTAG interface
UART GPIO interface
Host micro-processor interface
Memory card interface
Flash interface
Base band input interface
Audio Input interface
Audio Output interface
SDRAM interface

GAPGPS00116

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1.2.3 Pin list

The *Table 2* describes the primary function and behavior of the STA680 pins.

Table 2. Pins description

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Test							
1	A13	TESTMODE	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Factory test mode enable
Standard 1149.1 JTAG interface							
2	B14	TRST_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG active-low test reset
3	C12	TCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	JTAG test clock
4	D12	TMS	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG test mode state
5	C11	TDI	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG test data in
6	D11	TDO	O	-	1.8 V or 3.3 V	Generic IO supply	JTAG test data out
GPIO & UART interfaces							
7	A11	RTS_GPIO0	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART ready to send / GPIO bit 0
10	B11	CTS_GPIO1	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART clear to send / GPIO bit 1
13	A10	TXD_GPIO2	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART transmit data / GPIO bit 2
14	B10	RXD_GPIO3	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART receive data / GPIO bit 3
Not bonded	D10	GPIO4	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 4
Not bonded	B1	GPIO5	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 5
Not bonded	A2	GPIO6	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 6
Not bonded	C5	GPIO7	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 7
Reset							
15	A9	RESET_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Device active-low reset

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Host processor interfaces							
16	B9	SPI1_SS0_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 active-low slave select
17	A8	SPI1_SCK	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial clock
18	B8	SPI1_MOSI	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial data master out/slave in
21	A7	SPI1_MISO	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial data master in/slave out
24	B7	IIC1_SCL	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 serial clock line
25	A6	IIC1_SDA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 serial data line
Not bonded	C7	IIC1_DA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 data acknowledged
Not bonded	C6	IIC2_SCL	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
Not bonded	C4	IIC2_SDA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
Not bonded	D4	IIC2_DA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
IIS tuner interfaces							
40	C2	BB1_I	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface serial I data
35	B2	BB1_Q	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface serial Q data
41	C1	BB1_WS	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface word strobe
42	D3	BB1_BCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface bit clock
31	A4	BB2_I	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface serial I data
26	B6	BB2_Q	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface serial Q data
32	B4	BB2_WS	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface word strobe
33	A3	BB2_BCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface bit clock

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
IIS audio input interface							
45	F2	AUDIO_IN_AWS	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
44	E1	AUDIO_IN_ABCK	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
50	F1	AUDIO_IN_ADAT	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Reserved
Audio output interfaces							
55	G1	AWS	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio output word strobe
56	H3	ABCK	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio output clock
54	G2	ADAT	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output serial data
53	C3	ADAT2	O	-	1.8 V or 3.3 V	Generic IO supply	Reserved
52	E3	ADAT3	O	-	1.8 V or 3.3 V	Generic IO supply	Reserved
43	E2	SPDIF	O	-	1.8 V or 3.3 V	Generic IO supply	Reserved
34	B3	BLEND	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output blend output
51	G3	DAC256X	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output oversampling clock
Clock & oscillator							
57	K2	CLK_IN	I	-	1.8 V or 3.3 V	Generic IO supply	Reference digital clock
66	L1	OSC_IN	ana	-	1.8 V	Osc supply	28,224MHz crystal in or digital clock input
67	K1	OSC_OUT	ana	-	1.8 V	Osc supply	Crystal output
SPI Flash interface							
78	P4	SPI2_MISO	I	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial data master in/slave out
74	N3	SPI2_MOSI	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial data master out/slave in
75	P3	SPI2_SS0_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 active-low slave select 0
77	M3	SPI2_SS1_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	Reserved
Not bonded	M4	SPI2_SS2_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	Reserved

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Not bonded	M5	SPI2_SS3_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	Reserved
76	N4	SPI2_SCK	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial clock
SPI SD/MMC interface							
Not bonded	C9	SPI3_MISO	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
Not bonded	C8	SPI3_MOSI	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
Not bonded	D9	SPI3_SS_N	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
Not bonded	C10	SPI3_SCK	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Reserved
SDRAM interface							
84	P5	SDR_FEED_CLK	I	-	3.3 V	SDRAM IO supply	Feedback clock from SDRAM interface
83	N5	SDR_CLK_RAM 3V3	O	-	3.3 V	SDRAM IO supply	Clock to SDRAM for 3.3 V interface
97	N9	SDR_D0	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 0
98	P9	SDR_D1	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 1
101	N10	SDR_D2	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 2
102	P10	SDR_D3	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 3
103	N11	SDR_D4	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 4
106	P11	SDR_D5	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 5
107	N12	SDR_D6	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 6
108	P12	SDR_D7	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 7
96	P8	SDR_D8	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 8
95	N8	SDR_D9	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 9
92	M8	SDR_D10	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 10
91	P7	SDR_D11	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 11

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
90	N7	SDR_D12	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 12
87	M7	SDR_D13	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 13
86	P6	SDR_D14	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 14
85	N6	SDR_D15	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 15
111	N13	SDR_DQM0	O	-	3.3 V	SDRAM IO supply	Low-byte data input/output mask
112	M13	SDR_DQM1	O	-	3.3 V	SDRAM IO supply	High-byte data input/output mask
128	G13	SDR_WE_N	O	-	3.3 V	SDRAM IO supply	Active-low write enable
129	G12	SDR_CAS_N	O	-	3.3 V	SDRAM IO supply	Active-low column address strobe
130	F13	SDR_RAS_N	O	-	3.3 V	SDRAM IO supply	Active-low row address strobe
113	M14	SDR_CKE	O	-	3.3 V	SDRAM IO supply	Clock enable
133	F14	SDR_CS_N	O	-	3.3 V	SDRAM IO supply	Active-low chip select
134	E13	SDR_BA0	O	-	3.3 V	SDRAM IO supply	Bank select address 0
135	E14	SDR_BA1	O	-	3.3 V	SDRAM IO supply	Bank select address 1
139	D14	SDR_A0	O	-	3.3 V	SDRAM IO supply	Address bit 0 to SDRAM
140	C13	SDR_A1	O	-	3.3 V	SDRAM IO supply	Address bit 1 to SDRAM
141	C14	SDR_A2	O	-	3.3 V	SDRAM IO supply	Address bit 2 to SDRAM
142	B13	SDR_A3	O	-	3.3 V	SDRAM IO supply	Address bit 3 to SDRAM
127	H12	SDR_A4	O	-	3.3 V	SDRAM IO supply	Address bit 4 to SDRAM
124	H13	SDR_A5	O	-	3.3 V	SDRAM IO supply	Address bit 5 to SDRAM
123	J14	SDR_A6	O	-	3.3 V	SDRAM IO supply	Address bit 6 to SDRAM
122	J13	SDR_A7	O	-	3.3 V	SDRAM IO supply	Address bit 7 to SDRAM

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
119	K14	SDR_A8	O	-	3.3 V	SDRAM IO supply	Address bit 8 to SDRAM
118	K13	SDR_A9	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
138	D13	SDR_A10	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
117	L14	SDR_A11	O	-	3.3 V	SDRAM IO supply	Address bit 11 to SDRAM
116	L13	SDR_A12	O	-	3.3 V	SDRAM IO supply	Address bit 12 to SDRAM
Supplies							
Not bonded	F12	MODEOP_GEN	I	Pull-up	3.3 V	SDRAM IO supply	Define the opereting voltage of the "Generic I/O" supply group. If tied low the I/Os work at 1.8V else they work at 3.3V. Default value is 3.3V.
Not bonded	E12	MODEOP_FSH	I	Pull-up	3.3 V	SDRAM IO supply	Define the opereting voltage of the "Flash I/O" supply group. If tied low the I/Os work at 1.8V else they work at 3.3V. Default value is 3.3V.
8, 19, 28, 36, 46, 59, 71, 79, 89, 100, 109, 120, 131, 144	D5, D6, E11, F11, J11, J12, K3, K11, K12, L3	VDD	n/a	-	1.2 V	Core supply	Power supply for core logic
9, 20, 27, 37, 47, 58, 70, 80, 88, 99, 110, 121, 132, 143	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	GND	n/a	-	-	Core supply	Ground for core logic

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
11, 22, 29, 38, 48	A5, B5, H1, H2	GND_GEN_IO	n/a	-	-	Generic IO supply	Generic I/Os ground
12, 23, 30, 39, 49	A12, B12, D1, D2	VDD_GEN_IO	n/a	-	1.8 V or 3.3 V	Generic IO supply	Generic I/Os power supply
72	L6	GND_FSH_IO	n/a	-	-	Flash IO supply	Ground for Flash Interface I/Os
73	L5	VDD_FSH_IO	n/a	-	1.8 V or 3.3 V	Flash IO supply	Power supply for Flash Inteface I/Os
93, 104, 115, 126, 137	H14, L11, L12, M11, M12	GND_RAM_IO	n/a	-	-	SDRAM IO supply	Ground for SDRAM Interface I/Os
94, 105, 114, 125, 136	G14, M9, M10	VDD_RAM_IO	n/a	-	3.3 V	SDRAM IO supply	Power supply for SDRAM Interface I/Os
60	F3, F4	GND_PLL_DIG	n/a	-	-	PLL digital supply	Ground for PLL digital part
61	E4	VDD_PLL_DIG	n/a	-	1.2 V	PLL digital supply	Power supply for PLL digital part
62	J4	GND_PLL0_ANA	n/a	-	-	PLL analog supply	Ground for PLL0 analog part (2)
62	J3	GND_PLL1_ANA	n/a	-	-	PLL analog supply	Ground for PLL1 analog part (2)
63	M2	VDD_PLL0_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL0 analog part(3)
63	M1	VDD_PLL1_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL1 analog part (3)
64	J2, L2	GND_OSC	n/a	-	-	Osc supply	Ground for oscillator core
65	J1	VDD_OSC	n/a	-	1.8 V	Osc supply	Power supply for oscillator core
68	K4, L4	VDD_REG3V3	n/a	-	3.3 V	LDO supply	Voltage regulator input power supply@3.3 Volt
69	N1, N2	VDD_REG1V8	n/a	-	1.8 V	LDO supply	Voltage regulator output power supply@1.8 Volt

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Table 2. Pins description (continued)

Pin #	Ball#	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
82	L9	VDD_RAM_IO _1V8	n/a	-	1.8 V	n/a	Reserved - connect to 1.8 V supply
81	L10	GND_RAM_IO _1V8	n/a	-	-	n/a	Reserved - Connect to ground
Others							
Not bonded	M6	RFU	n/a	-	n/a	n/a	Reserved for future use - do not connect

1. Each input pin has a pull-up/down resistor to its default value. Unless otherwise specified, unused pins can be left unconnected after verifying that the impedance value of the pull-up/down resistor (see *Table 20*) is sufficient to guarantee noise immunity in user application environment.
2. In the LQFP package GND_PLL0_ANA and GND_PLL1_ANA are bonded together.
3. In the LQFP package VDD_PLL0_ANA and VDD_PLL1_ANA are bonded together.

1.2.4 I/Os supply groups

The STA680 I/O signals can be grouped into three different supply domains, as shown in (see *Table 2*):

- Generic IO supply
- Flash IO supply
- SDRAM IO supply group

In the LQFP package option all three groups must be supplied with 3.3 V.

In the LFBGA package the three supply groups can independently operate at 3.3 V or 1.8 V.

- The SDRAM_IO supply group must always be supplied with 3.3 V.
- The MODEOP_GEN pin selects the operating voltage of the Generic_IO supply group. If it is shorted to ground then all the I/O signals belonging to the Generic_IO supply group will work at 1.8 V; if the MODEOP_GEN pin is left floating or is tied to 3.3 V all the group I/Os will operate at 3.3 V.
- The MODEOP_FSH pin selects the operating voltage of the Flash_IO supply group. If it is shorted to ground then all the I/O signals belonging to the Flash_IO supply group will work at 1.8 V; if the MODEOP_FSH pin is left floating or is tied to 3.3 V the Flash Interface I/Os will operate at 3.3 V.

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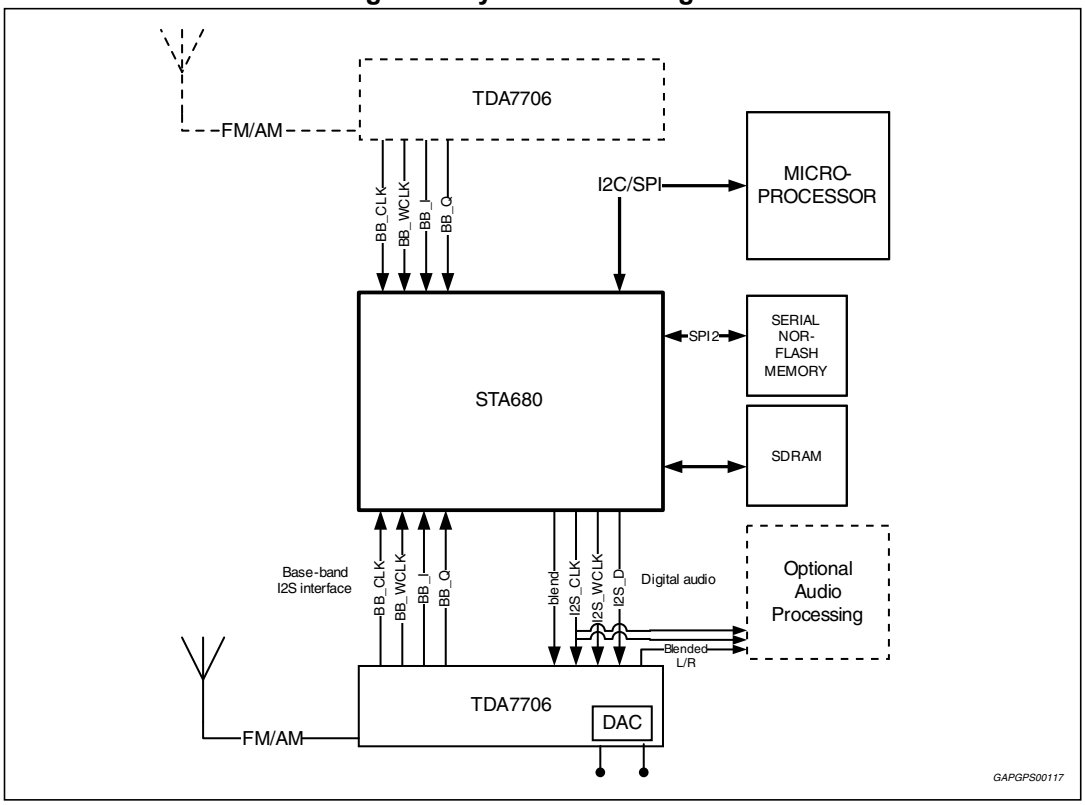
2 General description

The STA680 is a system-on-chip designed for demodulating and decoding HD Radio signals.

The STA680 is the base-band signal processor needed by an HD Radio receiver: it includes the OFDM demodulator, error correction, audio and data decoding of the digital channel.

Figure 4. System block diagram



The architecture of STA680 consists of a mixed hardware/software implementation. Computation-intensive functional blocks are implemented using custom logic. Software implementation is more efficient for functional blocks where flexibility is needed.

2.1 Receiver system overview

Such flexibility enables the STA680 to support both the HD 1.0 single-channel, and HD 1.5 double-channel applications, as shown in *Figure 4*. *Figure 5* shows the internal simplified block diagram of the STA680.

The STA680 receives the digital base-band signal from the digital tuner (e.g. TDA7706) and extracts the HD-encoded audio and data services as shown in *Figure 5*. STA680 is compatible with conventional base-band radio reception tuners (e.g. TDA7706).

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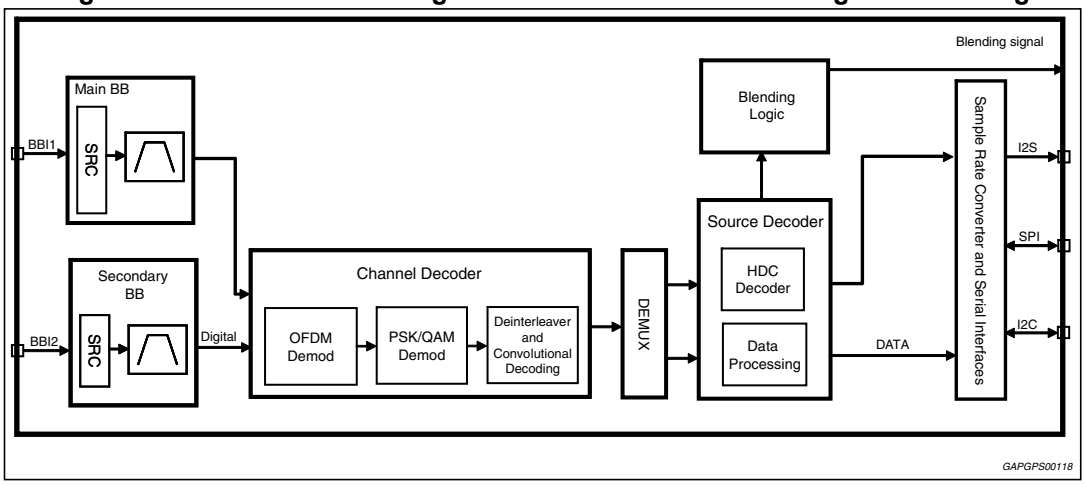
Figure 5. Functional block diagram for HD Radio demodulating and decoding



2.2 HD Radio processing

The STA680 HD Radio decoder performs the processing of the IBOC signal. The native internal processing data rate is 744.1875 kS/s for FM and 46.51171875 kS/s for AM.

The input I^2S base-band interface accepts several input sample rates thanks to the availability of a reconfigurable sample rate converter.The supported rates are: 650 kS/s, 675 kS/s, 882 kS/s and 912 kS/s.

The STA680 is responsible for the detection, acquisition and demodulation of the IBOC signal. This processing is mainly performed inside the Vectra DSP core. The demodulated signal is then passed to the Hi-Fi processor for decoding and handling of data services. The digital 44.1 kHz decompressed audio is streamed out by means of the Digital Audio Interface.

The STA680 requires a 4Mwords x16bits external SDRAM (with up to 32Mword x16bits supported) for data storage in order to process the HD Radio stream

2.3 Dual channel HD 1.5 Radio processing

The STA680 is capable of simultaneously demodulating two different HD Radio streams. This feature enables the device to decode the main HD Radio audio stream in parallel with the data service broadcasted by a different radio channel (for instance this feature allows to continue receiving traffic information provided by one radio station while listening to music from a different station).

The implementation of the dual stream HD Radio processing requires that two AM/FM RF tuners be connected to the STA680, as shown in *Figure 4*

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2.4 Overview of main functional blocks

2.4.1 Adjacent channel filter

This module performs digital filtering of the IBOC channel. It receives the complex base-band I/Q IBOC signal input from the tuner and pre-conditions the signal for subsequent modem processing.

2.4.2 HiFi2 core

The HiFi2 is a signal processing engine specifically designed to provide high quality 24-bit audio processing. The HiFi2 uses the Tensilica Xtensa LX engine with additional useful hardware capabilities such as:

- Specialized instructions for 24-bit Audio MAC & stream coding
- Dual MAC (each supports 24 x 24 and 32 x 16 bit format)
- Huffman Encode / Decode and truncate functions
- Two way Single-Instruction-Multiple-Data arithmetic and logic operations

2.4.3 Vectra core

The Vectra LX is on-chip a powerful, configurable 32-bit RISC engine optimized for DSP with VLIW capabilities. The Vectra LX includes eight MAC units, sixteen 160-bit vector operation registers, and a number of SIMD arithmetic instructions. Custom instructions in the Vectra are tailored to DSP applications such as filters and FFTs. The Vectra processor has been further configured with specific instructions for efficient performance on the HD Radio application.

2.4.4 DMA

A ten-channel DMA controller is attached to the AHB bus to allow the Vectra and HiFi2 processor cores to efficiently move large data-blocks.

2.4.5 Hardware accelerator (VITERBI)

The complex convolutional Viterbi hardware accelerator supports both K constants of 7 and 9, for IBOC digital FM and AM processing respectively.

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3 Operation and general remarks

3.1 Clock schemes

The STA680 needs an external clock source to drive the internal Phase Locked Loops (PLLs) that generate the clocks needed by the DSP cores and their peripherals.

The STA680 accepts several external reference clock sources, as listed below:

- The reference clock can be supplied through the use of an external crystal or as a digital signal coming from an external IC.
- The reference clock can have different frequencies and different input pins can be used.

The selection of the clock input mode is performed during the power-on phase of the device by latching the value of the pins ADAT3, BLEND and DAC256X on the rising edge of the RESET_N signal (see *Section 3.2*); these values shall be selected according to *Table 3*.

Table 3. Reference clock configuration

[ADAT3, BLEND, DAC256X]	Clock type	Input pin	Clock frequency (MHz)
[0,0,0] (1)	Crystal	OSC_IN	28.224
[0,0,1]	Digital	OSC_IN or CLK_IN (2)	23.3472
[0,1,0]	Digital	OSC_IN or CLK_IN (2)	36.48
[0,1,1]	Digital	OSC_IN or CLK_IN (2)	2.9184
[1,0,0]	Digital	BB1_BCK(3)	10.4
[1,0,1]	Digital	BB1_BCK(3)	10.8
[1,1,0]	Digital	BB1_BCK(3)	14.112
[1,1,1]	Digital	AUDIO_IN_ABCK(3)	2.9184

1. Default setting.
2. When using OSC_IN pin to input the reference clock the CLK_IN pin must be connected to ground and vice versa.
3. When using BB1_BCK or AUDIO_IN_ABCK to input the reference clock it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to high value (3.3 V or 1.8 V depending on the configuration).

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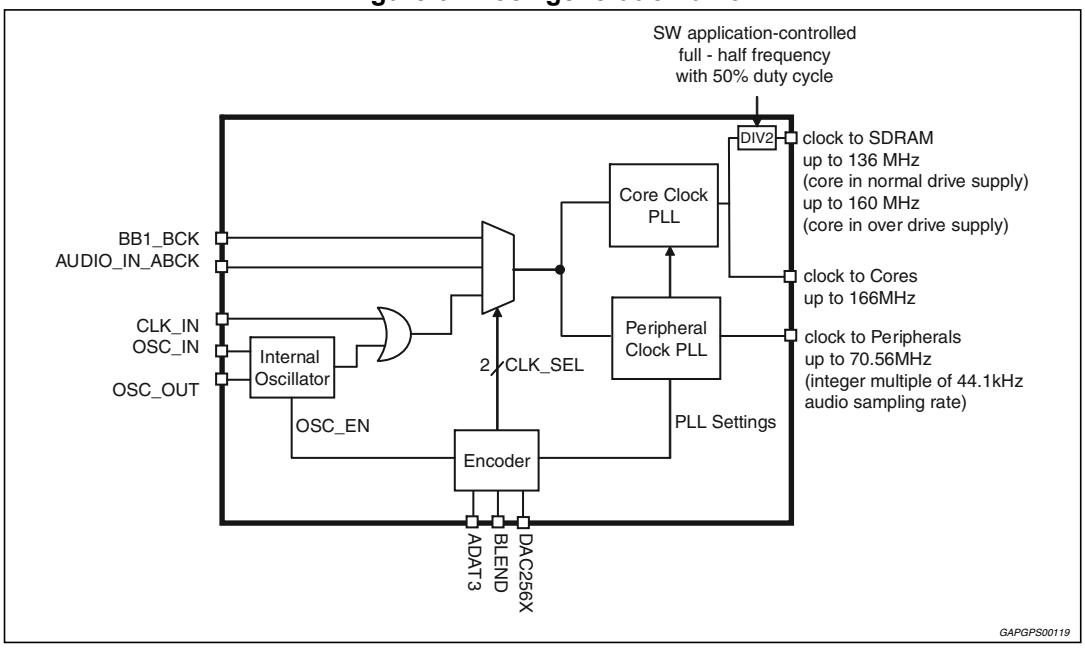
Figure 6 shows a simplified version of the internal clock generation unit.

Figure 6. Clock generation unit



Clock generation unit

Some remarks on the clock input pin follows:

- OSC_IN is always a 1.8 V input pin.
- CLK_IN, BB1_BCK and AUDIO_IN_ABCK are 3.3 V for the LQFP package, whereas they can be configured as either 3.3 V or 1.8 V pins for the LFBGA (see *Section 1.2.4*)
- When the clock is fed through the CLK_IN pin, the OSC_IN pin must be connected to ground (and vice versa).
- The BB1_BCK pin is the bit clock of the digital interface to the baseband Tuner. When this pin is selected as input for the reference clock, the selected clock frequency must be chosen compatibly with the Primary baseband Interface settings (see *Section 5.2*):
  - 10.4 MHz = 16 * 2 * 650 kHz → BBI set to 650 Ksample/s
  - 10.8 MHz = 16 * 2 * 675 kHz → BBI set to 675 Ksample/s
  - 14.112 MHz = 16 * 2 * 882 kHz → BBI set to 882 Ksample/s
- The AUDIO_IN_ABCK pin is the bit clock of the digital audio input interface to the Tuner. When this pin is selected as the reference clock source, the STA680 Input Serial Audio Interface must be configured as follows:
  - Slave mode
  - Input sample rate = 45.6 kHz
  - Word length = 32 bit

  With this settings the reference clock frequency is 2.9184 MHz = 32 * 2 * 45.6 kHz.
- When the device reference clock comes from BB1_BCK or AUDIO_IN_ABCK it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to its high value (3.3 V or 1.8 V depending on the configuration).

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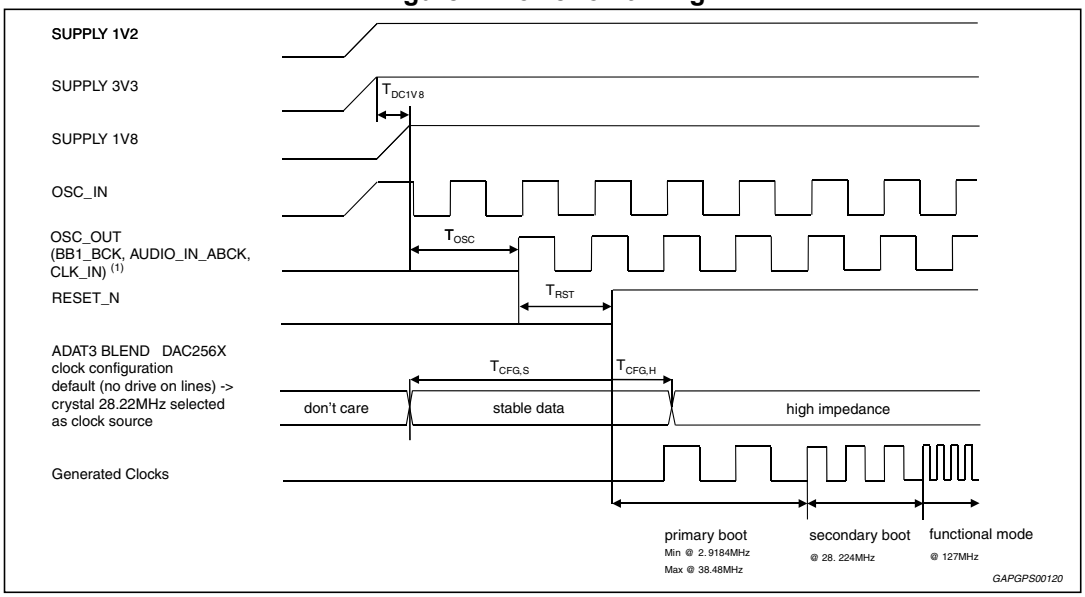
3.2 Power on

This chapter describes the power-on procedure for the cold start (i.e. when the device is not supplied before being turned on). *Figure 7* and *Table 4* show the timing for the cold start power up sequence.

Boot pins are latched at startup. Their default value is logic 0, in case logic 1 is needed a 6K2 pull-up resistor should be connected on the corresponding boot line. After reset release, the boot selection lines become outputs.

Figure 7. Power on timing



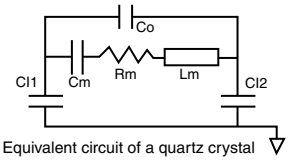
1. In case the Reference Clock is fed through BB1_BCK, AUDIO_IN_BCK or CLK_IN the Power On timing diagram is the same as *Figure 7* where OSC_OUT is substituted by the external supplied stable reference clock.

Table 4. Power on timing parameters

Symbol	Parameter	Min	Max	Unit
$T_{ramp-up}$	External supply ramp-up time	Same ramp-up time for 3.3 V and 1.2 V supply		-
T_{DC1V8}	DC1V8 regulator start-up time	-	1	ms
T_{OSC} (1)	Oscillator start-up time	-	400	µs
T_{RST}	Reset release time	2	-	ms
$T_{CFG,S}$	Setup time for clock configuration	0.1	-	µs
$T_{CFG,H}$	Hold time for clock configuration	10	-	ns

1. The oscillator start-up time depends on the crystal connected to the internal oscillator. The given value is estimated for a crystal with characteristic shown in *Figure 8*.

Figure 8. Crystal characteristics



Model	Value
Rm	50 Ohm
Lm	1.33 mH
Cm	26 fF
CO	7 pF
Ci = Cl1 = Cl3	38pF (33pF + 5pF parasitic)

GAPGPS00121

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4 Power supply ramp-up phase

The external power supply circuit on the board has to ensure that all the power supplies are ramped up to their specified levels The ramp up phase of each power domain should start at the same time.

The RESET_N pin must be kept low from the beginning.

For normal applications, the TESTMODE pin (Factory test mode enable, see *Table 3*) must be connected to ground.

4.1 Oscillator setting time

Once the power supply has reached the operating level, the internal voltage regulator gets functional after T_{DC1V8} = 1ms (see *Table 4*) and starts supplying the 1.8 V voltage to internal IPs such as PLLs and Crystal Oscillator.

The PLL is powered up but not yet functional since the internal logic keeps it in bypass mode until a stable clock is available and STA680 has entered the secondary boot phase.

As shown in *Figure 7*, if an external crystal is connected to the internal oscillator this will output a correct waveform after T_{OSC} = 400 µs (see*Table 4*).

Alternatively, if no crystal is used, a digital clock must be supplied according to the instructions detailed in *Section 3.1*. In this case the Power On timing diagram is the same as *Figure 7* where OSC_OUT is substituted by the external supplied stable reference clock (alternatively BB1_BCK, AUDIO_IN_BCK or CLK_IN).

The RESET_N pin must be kept low for an additional T_{RST} = 2 ms both when using a crystal and when using an external reference clock.

As described in *Section 3.1* the internal clock configuration is defined by the status of the pins ADAT3, BLEND and DAC256X; this is latched on the rising edge of the RESET_N signal.

The voltage of the three pins must be stable from at least T_{CFG} = 0.1 µs before the rising edge of the RESET_N signal.

4.2 Boot sequence

Once the RESET_N signal has been released and the power up sequence correctly executed, the STA680 enters the boot procedure, which consists of two phases:

1. device setup
2. application authentication and download.

During the first phase, the STA680 executes the on-chip primary boot code contained in the Boot ROM.

The primary boot synchronizes the internal cores, initializes the SPI and IIC interfaces and automatically selects the secondary boot code source by looking for a pre-defined pattern into UART1, Flash, SPI1, IIC1 and IIC2.

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Once the source of the secondary boot code has been identified, the STA680 executes the following steps:

1. code authentication
2. SDRAM initialization
3. secondary boot code download to SDRAM.

In order to decrease the boot time during the secondary phase, the STA680 performs the setup of the PLLs and sets the internal clock frequency to 28.224 MHz (see *Figure 7*). Subsequently it downloads and validates the application code either from the external Flash memory or from the host microcontroller. This ends the boot procedure.

4.3 Normal operation mode

After the execution of the boot code, the device enters the normal operation mode by jumping to the main program loop.

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5 Digital I/O and memory interfaces

5.1 Interfaces: LQFP vs. LFBGA

The STA680 connectivity depends on the selected package[a]. The differences between the two package options are listed in *Table 5*.

Table 5. Interface list

Interface name	Direction	LQFP	LFBGA
Baseband interface 1	I	√	√
Baseband interface 2 (data only)	I	√	√
I^2S audio input	I	√	√
I^2S audio output (six channels)	O	√	√
I^2C primary interface (Micro)	I/O	√	√
I^2C secondary Interface	I/O	x	√
SPI micro interface	I/O	√	√
SPI Flash interface (double chip select)	I/O	√	√
SPI Flash interface extension (up to 4 chip select)	I/O	x	√
SPI SD/MMC	I/O	x	√
SDRAM interface	I/O	√	√
S/PDIF interface	O	√	√
UART interface	I/O	√	√
4 GPIO lines	I/O	x	√
JTAG test interface (boundary scan only)	I/O	√	√

a. STA680 firmware determines actual feature availability. Refer to the STA680 firmware Release Notes.

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5.2 Base-band I^2S interface

The STA680 has two digital Base-Band Interfaces (BBI1 and BBI2).

The tuners receive the analog signals from the antenna, sample them, perform down conversion and channel selection, and transmit the digital base-band streams to the STA680 by means of BBI1 and BBI2

Each BB interface consists of four wires: two serial data lines (I/Q), one bit clock line and one frame clock line. The serial data is always transmitted with the MSB first and a 16-bit word length. The complex base-band signal needs to be at zero IF.

Most common data rates are supported by using the internal base-band sample rate converter. The allowed base-band interface data rates are:

- 650 kS/s,
- 675 kS/s,
- 882 kS/s
- 912 kS/s.

Table 6. describes the pin functionality of both BBI1 and BBI2.

Table 6. Baseband interfaces pin list

Pin name	Designation	Type	Drive
BB1_WS	Primary baseband interface word strobe	I	-
BB1_BCK	Primary baseband interface bit clock	I	-
BB1_I	Primary baseband interface serial I data	I	-
BB1_Q	Primary baseband interface serial Q data	I	-
BB2_WS	Secondary baseband interface word strobe	I	-
BB2_BCK	Secondary baseband interface bit clock	I	-
BB2_I	Secondary baseband interface serial I data	I	-
BB2_Q	Secondary baseband interface serial Q data	I	-

The base-band interface supports the modes shown in *Figure 9* Timing information for the protocols shown in *Figure 9* is detailed in *Table 7*.

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Figure 9. BBI waveforms and timings

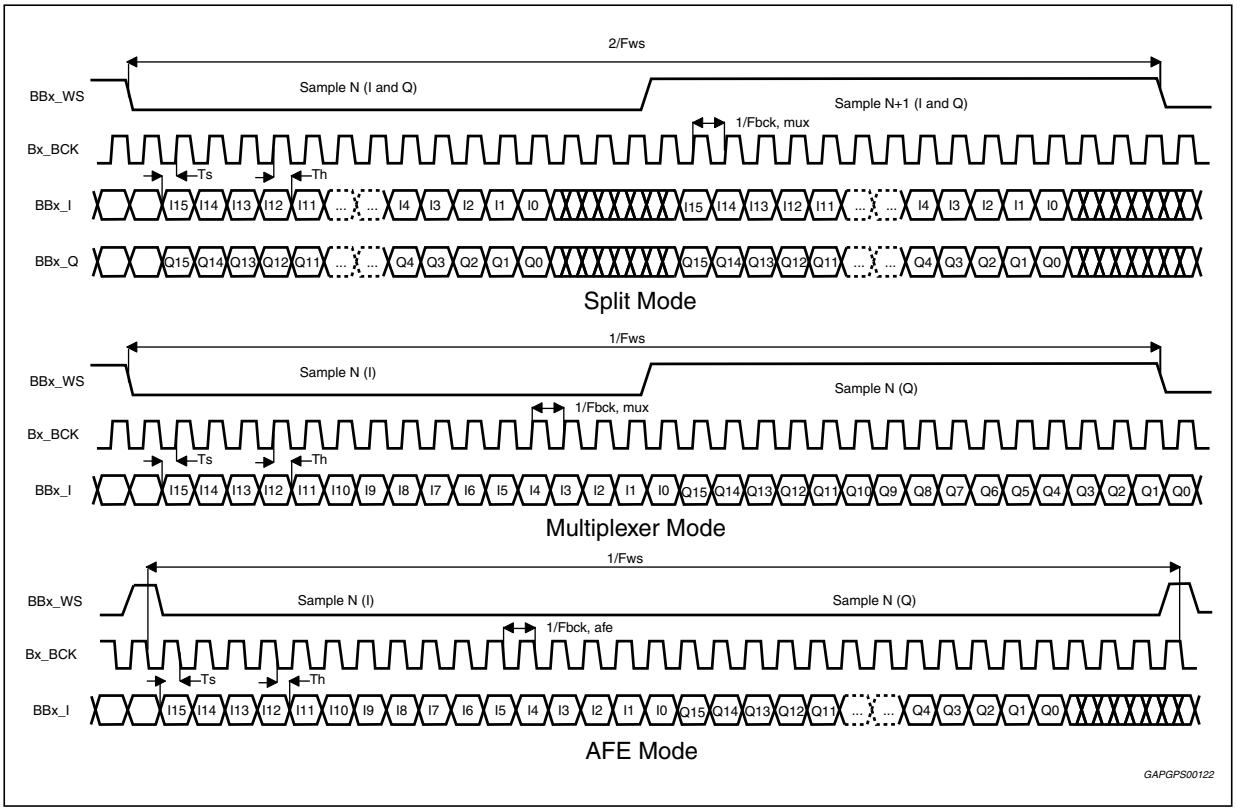

Table 7. BBI timing values

Symbol	Parameter	Working Rate					Unit
Fws	Word Strobe	650	675	744.1875	882	912	kHz
Fbck,split	Bit clock in SPLIT mode	16 x Fws					kHz
Fbck,mux	Bit clock in MUX mode	32 x Fws					kHz
Fbck,afe	Bit clock in AFE mode	32 x Fws					kHz
Th	Data hold time	4					ns
Ts	Data setup time	8					ns

5.3 Base-band I²S interface frequency diversity

When the STA680 is paired with the TDA7706 tuner it can benefit from the supported base-band interface frequency diversity that allows to improve the EMI robustness of the system.

The frequency diversity technique allows the base-band data-rate to be varied at run-time depending on the frequency of the tuned station, thus moving the intrinsic radiation of the BBI digital lines away from the signal of interest.

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5.4 Audio interface (AIF)

The STA680 uses a stereo I^2S interface for sending the decoded digital audio back to the tuner, where the blending with the legacy AM/FM demodulated audio occurs.

The receivers and transmitters can be used either in master mode, running with the STA680 internal audio frequency of 44.1 kHz or in slave mode running with a frequency determined by the external device. In slave mode, the internal Audio Sample Rate Converter (ASRC, see *Chapter 5.4.2*) adapts the external data rate (from 44.1 to 48 kSps) to the internal one.

Table 8. AIF pin list

Pin name	Designation	Type	Drive
AWS	Digital audio output word strobe	I/O	4mA
ABCK	Digital audio output clock	I/O	4mA
ADAT	Digital audio output serial data	O	4mA
DAC256X	Digital audio output oversampling clock (256 x Fs)	O	4mA
BLEND	Digital audio output blend output	O	4mA

5.4.1 Output serial audio interface (SAI)

The output serial audio interface is used to send the decoded audio from the HD Radio Decoder to an external IC (e.g. TDA7706).

The output SAI is an I2S interface which provides audio samples in stereo at a 44,1 kS/s data rate in master mode. In slave mode, other sample rates (from 44.1 to 48kSps) are supported by means of the internal ASRC (see *Section 5.4.2*).

The output SAI interface is composed by three lines: one data line and two clock lines.

The output SAI supports a 32x or 64x bit clock with 16-bit precision audio data. The 32x clock mode has no bit padding. The 64x clock mode adds 16-bits zero padding at the end of the 16-bit audio data. *Figure 10* shows timing diagrams for the supported modes.

An oversampled audio master-clock is also available for directly interfacing the STA680 to an external DAC. *Table 8* shows the timing values for the output SAI interface.

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Figure 10. Serial audio interface waveforms and timings

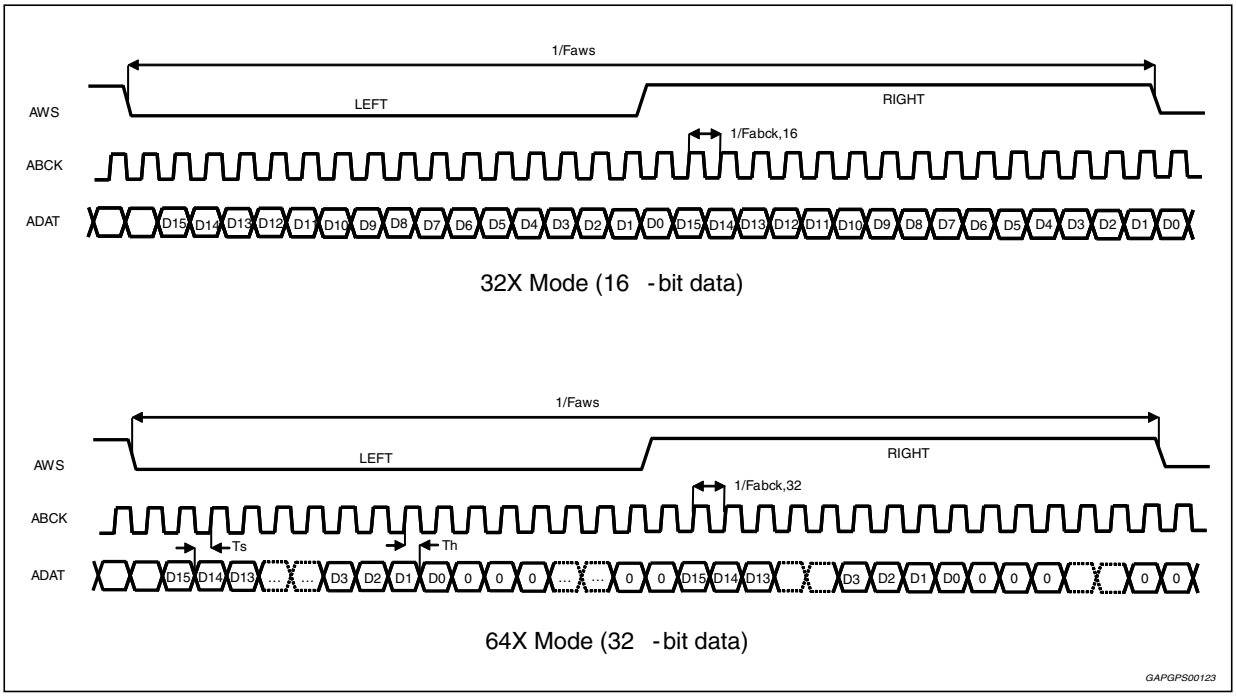

Table 9. Serial audio interface timing values

Symbol	Parameter	Working rate			Unit
Faws	Word strobe	44.1 ±10 Hz	45.6 ±15 Hz	48 ±15 Hz	kHz
Fabck,16	Bit clock for 16-bit data	32 x Faws			MHz
Fabck,32	Bit clock for 32-bit data	64 x Faws			MHz
Th	Data hold time	5			ns
Ts	Data setup time	20			ns

5.4.2 Audio sample rate converter (ASRC)

The STA680 embeds a stereo channel sample rate converter to be used in combination with either the output (one single data-line) or the input SAI. The ASRC has a Total Harmonic Distortion plus Noise (THD+N) level at 1 kHz smaller than -85 dB (0.0056%).

The supported data rates are:

- 44,100 (± 10 Hz),
- 45,600 (± 15 Hz)
- 48,000 (± 15 Hz)

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5.5 Serial peripheral interfaces (SPI)

The STA680 provides two serial peripheral interfaces:

- SPI1 is intended for communicating with the Host Microcontroller.
- SPI2 interfaces the STA680 to the external flash memory

The maximum SPI clock frequency in master mode is 25 MHz.

In slave mode the maximum input clock frequency is a function of the internal peripheral clock.

In particular the maximum frequency is $F_{SPI} = \frac{F_{perif}}{8}$, where F_{perif} 56.448MHz

(for STA680-51001569-05000033-C0002.000 firmware version) is the frequency of the clock feeding the peripheral bus and blocks.

Figure 11 shows the timing diagrams and waveform for the three SPI interfaces.

Figure 11. SPI interface timings diagrams and waveforms

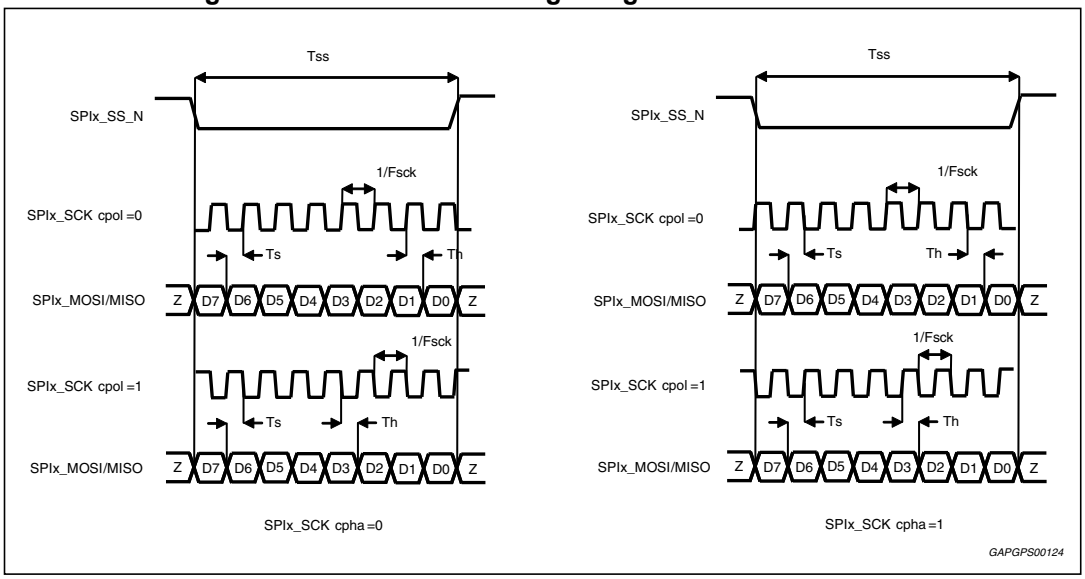

Table 10 shows the timing values for the SPI interface.

Table 10. SPI interface timing values

Symbol	Parameter	Working rate		Unit
		Min.	Max.	
Tss	Chip select	8/Fsck	-	ns
Fsck	Serial bit clock, slave mode	1.076	8000	kHz
Fsck	Serial bit clock, master mode	1.076	25000	kHz
Th	Data hold time	7	-	ns
Ts	Data setup time	15	-	ns

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5.5.1 Host micro serial peripheral interface (SPI1)

SPI1 is used to interface the STA680 with a host processor interface.

The communication with the host-microcontroller can alternatively be performed via I^2C as described in *Section 5.6.1*.

The Host Micro SPI is a slave only interface.

For the relevant pin description see *Table 11*.

Table 11. Host micro SPI pin list

Pin name	Designation	Type	Drive
SPI1_MISO	Host Micro SPI data master in/slave out	O	4mA
SPI1_MOSI	Host Micro SPI data master out/slave in	I	-
SPI1_SCK	Host Micro SPI clock	I	4mA
SPI1_SS_N	Host Micro SPI active-low slave select 1	I	4mA

5.5.2 Flash serial peripheral interface (SPI2)

SPI2 is typically used for connecting the STA680 to an external Flash memory where the boot code and configuration parameters could be stored. The minimum required capacity for this purpose is 1 Mbit. SPI2 is master-only.

Up to 4 chip select lines are available on the STA680 with the BGA package. For the relevant pin description see *Table 12*.

Table 12. Flash SPI pin list

Pin name	Designation	Type	Drive
SPI2_MISO	Flash SPI data master in/slave out	I	-
SPI2_MOSI	Flash SPI data master out/slave in	O	4mA
SPI2_SCK	Flash SPI clock	O	4mA
SPI2_SS_N	Flash SPI active-low slave select 1	O	4mA
SPI2_SS1_N	Flash SPI active-low slave select 2	O	4mA
SPI2_SS2_N	Flash SPI active-low slave select 3 (1)	O	4mA
SPI2_SS3_N	Flash SPI active-low slave select 4 (1)	O	4mA

1. Only available in BGA package.

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5.6 I²C interfaces

The STA680 features two I²C interfaces. For the relevant pin description see *Table 13*.

Table 13. Host and auxiliary I²C interface pin list

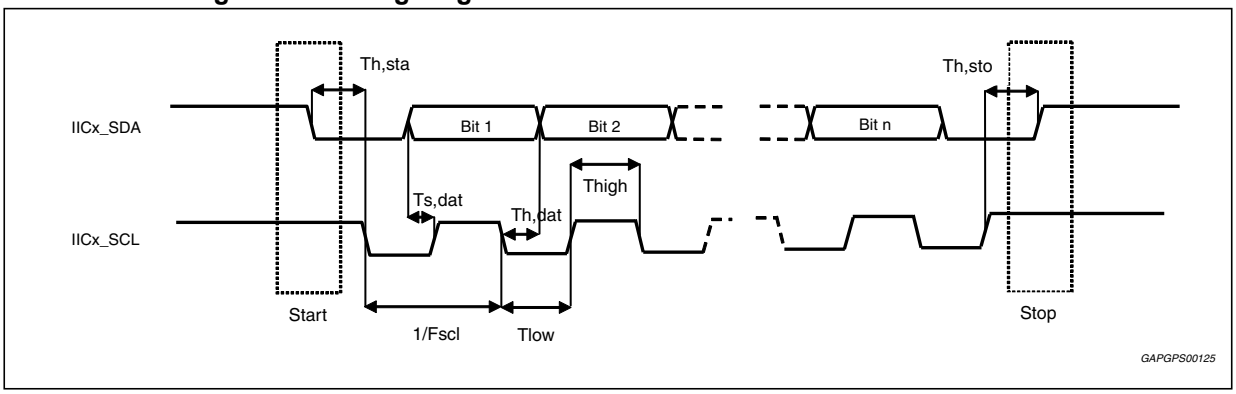
Pin name	Designation	Type	Drive
IIC1_SCL	Host Micro I²C interface serial clock line	I/O	4mA
IIC1_SDA	Host Micro I²C interface serial data line	I/O	4mA
IIC1_DA (1)	Host Micro I²C interface data acknowledged	I/O	4mA
IIC2_SCL	Auxiliary I²C interface serial clock line	I/O	4mA
IIC2_SDA	Auxiliary I²C interface serial data line	I/O	4mA
IIC2_DA (1)	Auxiliary I²C interface data acknowledged	I/O	4mA

1. Only available in BGA package.

The data pin of the I²C interface is an open drain driver and it needs a resistive pull- up as required by Philips' I²C specification.

Figure 12 shows timing diagrams and waveform for the two I²C interface.

Figure 12. Timing diagrams and waveform for the two I²C interfaces



In *Table 14* the timing values for the I²C interfaces are reported.

Table 14. I²C interface timing values

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
Fscl	SCL clock frequency	-	100	-	400	kHz
Tlow	Low period of SCL clock	4.7	-	1.3	-	µs
Thigh	High period of SCL clock	4	-	0.6	-	µs
Th, dat	Data hold time	5	-		-	µs
Ts, dat	Data setup time	250	-	100	-	µs
Th, sta	Hold time for start condition	4	-	0.6	-	µs
Ts, sto	Setup time for stop condition	4	-	0.6	-	µs

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5.6.1 Host micro I^2C interface (I2C1)

I2C1 is used to connect the STA680 to the host microcontroller to transmit commands, diagnostic information, and data.

The I2C1 interface is a standard bi-directional I^2C interface.

The I2C1 interface supports 7-bit addressing and 8-bit data. It can run in both standard mode (serial clock frequency up to 100 kHz) and fast mode (up to 400 kHz). The I^2C device addresses are reported in *Table 15*.

An additional control line called IIC1_DA is provided as an extension of the I^2C standard. This line is used as a flag to show the host controller that data is available and it can be polled by the host micro in either master or slave modes.

Table 15. I2C1 interface device address

I2C1	Primary address	Secondary address
Read Address	00101111b (0x2F)	00101101b (0x2D)
Write Address	00101110b (0x2E)	00101100b (0x2C)

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5.7 SDRAM interface

The SDRAM interface supports up to 32M x 16 SDRAM; both standard and mobile protocols are accepted. For the relevant pin description see *Table 16*

Table 16. SDRAM Interface pin description

Pin Name	Designation	Type	Drive
SDR_D[0:15]	SDRAM interface data bus	I/O	4 mA
SDR_A[0:12]	SDRAM interface address bus	O	4 mA
SDR_BA[0:1]	Bank address	O	4 mA
SDR_CAS_N	Active-low column address strobe	O	8 mA
SDR_RAS_N	Active-low row address strobe	O	8 mA
SDR_WE_N	Active-low write enable	O	8 mA
SDR_CS_N	Active-low chip select	O	8 mA
SDR_DQM0	low-byte data input/output mask	O	4 mA
SDR_DQM1	high-byte data input/output mask	O	4 mA
SDR_CKE	Clock enable	O	4 mA
SDR_CLK_RAM3V3	Clock to SDRAM for 3.3 V interface	O	8 mA
SDR_FEED_CLK	Feedback clock from SDRAM	I	8 mA

The minimum required SDRAM size for single channel application is 64 Mbit while for a dual channel application at least 128 Mbit are needed.

Figure 13 shows the timing diagrams and waveform for the SDRAM interface.

Figure 13. Timing diagrams and waveform for the SDRAM interface

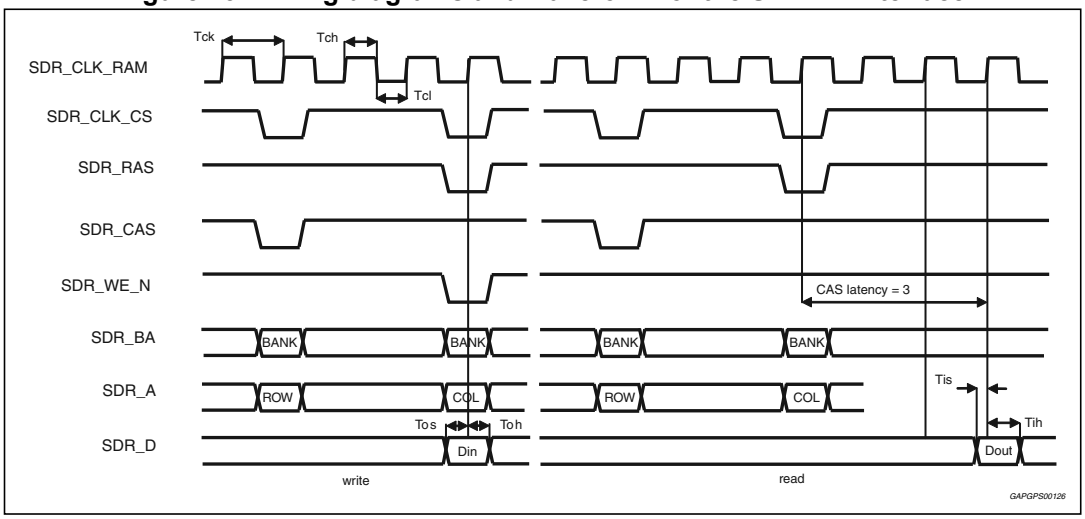

Table 17 reports the timing values for the SDRAM interface

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Table 17. SDRAM interface timing values

Symbol	Parameter	Condition	Software application	Min.	Max.	Unit
Tck	SCL clock period	Core in normal drive	Full rate	7.35	-	ns
			Half rate	12.05	-	
		Core in overdrive	Full rate	6.25	-	
			Half rate	12.05	-	
Tch	CLK high level width	-	-	2.5	-	ns
Tcl	CLK low level width	-	-	2.5	-	ns
Toh	Data out hold time	-	-	0.9	-	ns
Tos	Data out setup time	-	-	1.5	-	ns
Tis	Data In setup time	-	-	0.8	-	ns
Tih	Data In hold time	-	-	1.6	-	ns
Tt	Transition time	-	-	-	1.2	ns

For power saving and reduced interference on the board, the SDRAM speed is programmed to work at half speed with respect to the internal data processing:

- Full Rate SW application: the SDRAM interface works at the same frequency as the internal data processing;
- Half Rate SW application: the SDRAM interface works at half frequency with respect to the internal data processing

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6 Electrical specifications

6.1 Absolute maximum ratings

Table 18. Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
VDD	Core supply voltage	-	-	1.47	-	V
VDD_GEN_IO	Generic IO supply voltage	-	-	3.6	-	V
VDD_FSH_IO	Flash IO supply voltage	-	-	3.6	-	V
VDD_RAM_IO	SDRAM IO supply voltage	-	-	3.6	-	V
VDD_OSC	Osc 1V8 supply voltage	-	-	1.95	-	V
VDD_PLL_ANA	PLL analog supply voltage	-	-	2.75	-	V
VDD_PLL_DIG	PLL digital supply voltage	-	-	1.47	-	V
VDD_SAF	SAF core supply voltage	-	-	1.47	-	V
V_i	Voltage on input pin	-	-0.5	-	VDDIO+0.5	V
V_o	Voltage on output pin	-	-0.5	-	VDDIO+0.5	V
V_{ESD}	ESD absolute minimum withstand voltage	R = 1.5 kΩ; C = 1.5 pF Human Body Model, BGA package	>|±1000|			V
		Charged device mode, BGA package	>|±500|			
		R = 1.5 kΩ; C = 1.5 pF Human Body Model, LQFP package	>|±1000|			
		Charged device mode, LQFP package	>|±450|			

6.2 Thermal data

Table 19. Thermal data

Symbol	Parameter	Test condition	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	LQFP package, JEDEC 2s2p PCB, free air	42	°C/W
		BGA package, JEDEC 2s2p PCB, free air	44	
T_{stg}	Storage temperature	-	-55 to 150	°C
T_{amb}	Operating ambient temperature	-	-40 to 85	°C
$T_{j,\ max}$	Maximum junction temperature	-	125	°C

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6.3 Operating conditions

Table 20. DC electrical characteristics

Symbol	Parameter	Test condition			Min.	Typ.	Max.	Unit
VDD	Core supply voltage	Normal drive			1.14	1.2	1.26	V
		Over drive			1.33	1.4	1.47	V
VDD_GEN_IO	Generic IO supply voltage	-			3.14	3.3	3.46	V
VDD_FSH_IO	Flash IO supply voltage	-			3.14	3.3	3.46	V
VDD_RAM_IO	SDRAM IO supply voltage	-			3.14	3.3	3.46	V
VDD_RAM_IO_1V8	Supply for the SDRAM clock at 1.8V	-			1.71	1.8	1.89	V
VDD_OSC	Oscillator analog supply voltage	-			1.71	1.8	1.89	V
VDD_PLL_ANA	PLL analog supply voltage	-			1.71	1.8	1.89	V
VDD_PLL_DIG	PLL digital supply voltage	Normal drive			1.14	1.2	1.26	V
		Over drive			1.33	1.4	1.47	V
VDD_SAF	SAF supply voltage	Normal drive			1.14	1.2	1.26	V
		Over drive			1.33	1.4	1.47	V
I_{1V2}	Current from 1.2 V supply	HD 1.0(1)	T_{amb}=25°C	VDD=1.20V	-	90	-	mA
			T_{amb}= 85°C	VDD=1.26V	-	-	149	mA
		HD 1.5(2)	T_{amb}=25°C	VDD=1.20V	-	110	-	mA
			T_{amb}= 85°C	VDD=1.26V	-	-	180	mA
I_{3V3}	Current from 3.3 V supply	HD 1.0	T_{amb}= 25°C	VDD_IO(3)=3.3V	-	32	-	mA
			T_{amb}= 85°C	VDD_IO= 3.46V	-	-	41	mA
		HD 1.5	T_{amb}= 25°C	VDD_IO = 3.3V	-	50	-	mA
			T_{amb}= 85°C	VDD_IO= 3.46V	-	-	70	mA
Pd	Power dissipation	HD 1.0	T_{amb}= 25°C	typical supply	-	214	-	mW
			T_{amb}= 85°C	max supply	-	-	330	mW
		HD 1.5	T_{amb}= 25°C	typical supply	-	297	-	mW
			T_{amb}= 85°C	max supply	-	-	469	mW
Iil	Low level input leakage current(4)	Vi = 0V			-	-	1.9	µA
Iih	High level input leakage current(4)	Vi = VDD_GEN_IO(5)			-	-	1.9	µA

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Table 20. DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Ilpu	High level input leakage current on pull up(6)	Vi = VDD_GEN_IO(5)	-	-	2.9	µA
Ilpd	Low level input leakage current on pull-down(7)	Vi = 0V	-	-	10	µA
Rpu	Equivalent pull-up resistance(8)	1.8 supply mode V_i = 0.1V	104	-	360	kΩ
		3.3 supply mode V_i = 0.1V	52	-	180	
Rpd	Equivalent pull-down resistance(9)	1.8 supply mode V_i = 1.7V	104	-	360	kΩ
		3.3 supply mode V_i = 3.5V	52	-	180	
Vil	Low level input voltage	1.8 supply mode	-0.3	-	0.35 · VDD_IO_GEN	V
		3.3 supply mode	-0.3	-	0.7	V
Vih	High level input voltage	1.8 supply mode	0.65 · VDD_GEN_IO	-	VDD_GEN_IO +0.3	V
		3.3 supply mode	2.0	-	VDD_GEN_IO +0.3	V
Vhyst	Input hysteresis voltage	3.3 supply mode	50	-	-	mV
Voh	Output high voltage	Ioh =XmA(10)	VDD_GEN_IO – 0.4V	-	-	V
Vol	Output low voltage	Iol =XmA(10)	-	-	0.3	V
Ilatchup	Injection current	Maximum operating junction temperature 105 °C	100	-	-	mA
Iil_ram	Low level input leakage current(4)	Vi = 0V	-	-	4	µA
Iih_ram	High level input leakage current(4)	Vi = VDD_RAM_IO	-	-	4	µA
Ilpu_ram	High level input leakage current on pull up(6)	Vi = VDD_RAM_IO	-	-	4	µA
Ilpd_ram	Low level input leakage current on pull-down(7)	Vi = 0V	-	-	-	µA
Ipu_ram	Pull-up current	Vi = 0.1V	40		150	µA
Rpu_ram	Equivalent pull-up resistance(8)	Vi = 0.1V	23	-	87	kΩ

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Table 20. DC electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Vil_ram	Low level input voltage	-		0.8	-	-	V
Vih_ram	High level input voltage	-		-	-	2	V
Vhyst_ram	Schmitt trigger hysteresis	-		300	-	800	mV
Voh_ram	High level output voltage	Ioh = -XmA(10)		VDD_RAM_IO -0.4	-	-	V
Vol_ram	Low level output voltage	Iol =XmA(10)		-	-	0.3	V
Idc	3V3 to 1V8 DC regulator output current	-		-	-	100	mA
C_L	Output load for triple voltage pads (1.8V and 3.3V)	1.8 V supply mode for 4mA buffer	40 MHz	-	-	30	pF
		3.3 V supply mode (for both 4mA and 8mA)	60 MHz	-	-	30	pF
			75 MHz	-	-	20	pF
$C_{L,3V3}$	Output load for 3.3V pads	4 mA buffer	140MHz	-	-	10	pF
		8 mA buffer	140MHz	-	-	20	pF
$C_{L,\ DC}$	DC regulator output load(11)	-		2.2	-	4.7	µF

1. Current consumption and power dissipation measured for single channel software application (HD 1.0) running at 127MHz on core and 65 MHz on SDRAM interface with FW version STA680-51001569-0D000003-C0004.000.
2. Current consumption and power dissipation measured for dual channel software application (HD 1.5) running at 127MHz on core and 130 MHz on SDRAM interface with FW version STA680-51001569-0D000033-C0004.000.
3. VDD_IO generally refers to the supply of the VDD_GEN_IO, VDD_FSH_IO and VDD_RAM_IO groups.
4. Performed on all the input pins excluded the pull-down and pull-up ones.
5. VDD_GEN_IO may be VDD_FHS_IO or VDD_GEN_IO depending on interface considered.
6. Performed only on the Input pins with pull up.
7. Performed only on the Input pins with pull down.
8. Guaranteed by Ipu measurements.
9. Guaranteed by Ipd measurements.
10. XmA = 4mA for a BD4, 8mA for BD8 pad type.
11. Dielectric=X7R ESRmax=100ohm, 2.2µF +-5% or any above 3µF+-10% but less than 4.7µF+-10%.It is also recommended to distribute the 2.2µF capacitance on the board by placing equivalent number of smaller capacitance value (for example, 470nF) near each VDD_REG1V8 supply pad.

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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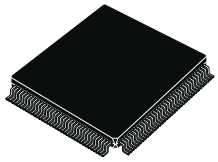
Figure 14. LQFP144 (20x20x1.4 mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.6890	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP144 (20x20x1.40mm)
Low profile plastic **Q**uad **F**lat **P**ackage

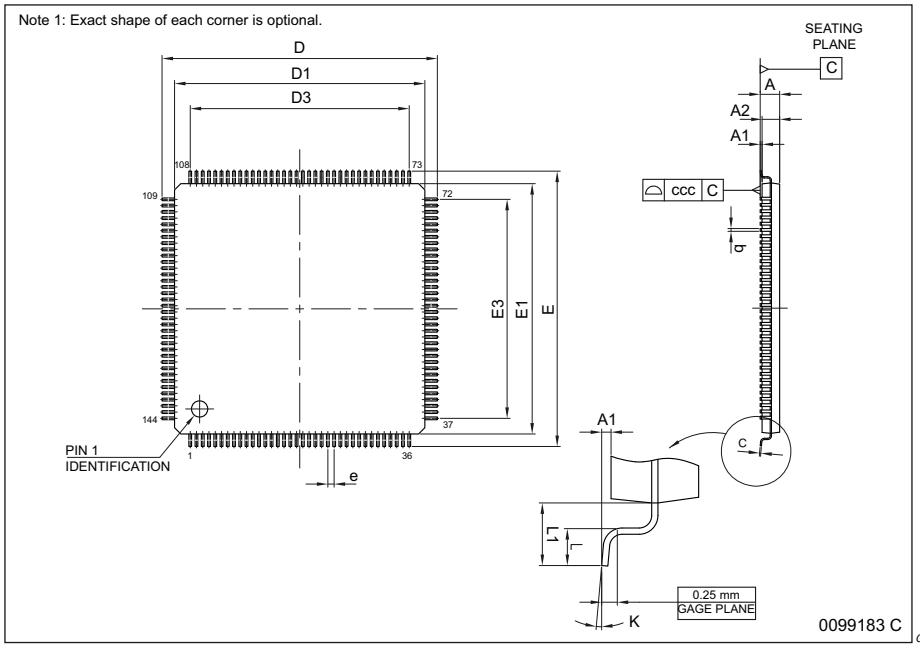


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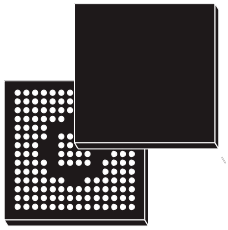
Figure 15. LFBGA 168 balls (12x12x1.4 mm) mechanical data and package dimensions

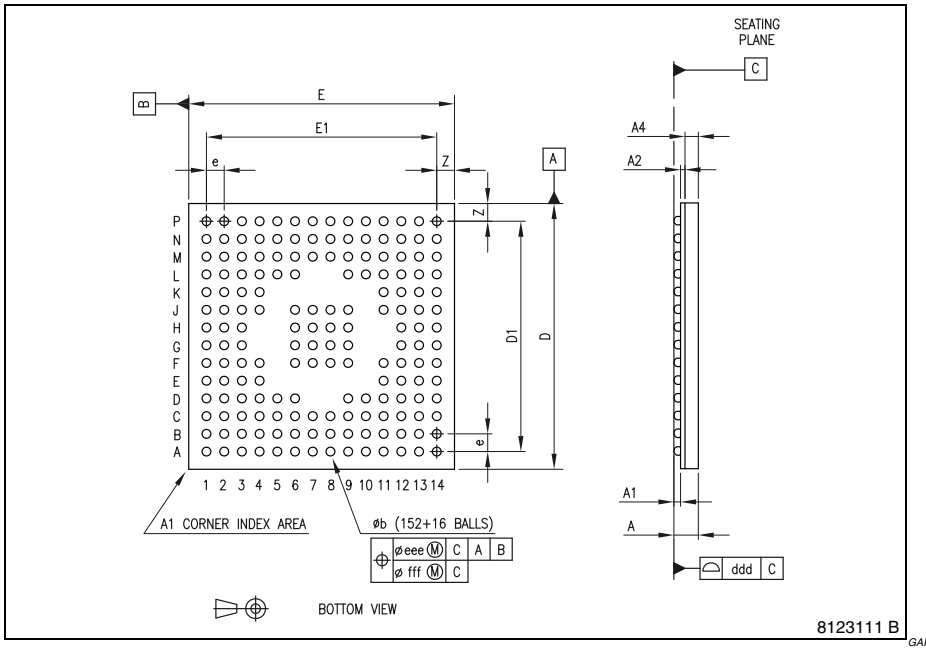
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.400			0.0551
A1	0.210			0.0083		
A2		0.200			0.0078	
A4			0.800			0.0315
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	11.850	12.000	12.150	0.4665	0.4724	0.4783
D1		10.400			0.4094	
E	11.850	12.000	12.150	0.4665	0.4724	0.4783
E1		10.400			0.4094	
e		0.800			0.0315	
Z		0.800			0.0315	
ddd			0.100			0.0039
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 12 x 12 x 1.4mm

LFBGA 168 balls
Low profile **F**ine Pitch **B**all **G**rid **A**rray



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8 Revision history

Table 21. Document revision history

Date	Revision	Changes
25-Jul-2008	1	Initial release.
19-Dec-2008	2	Update ECOPACK® information in *Section 7 on page 40*.
31-Jul-2009	3	Added *Section 2: HD Radio™ system on page 7*. Changed *Table 2, 4, 7, 12, 13, 13, 17 and 20.* Changed *Figure 14*, *15*, *6*, *3*, *8* and *11*. Add *Figure 10: Crystal characteristics on page 26*.
09-Nov-2010	4	Document status promoted from preliminary data to datasheet. Modified *Features*. and *Description on page 1*. Modified the flow of the sections. Modified *Section 1: Block diagram and pin description*. Add *Section 2: General description*. Changed *Figure 7: Power on timing* and updated *Table 4: Power on timing parameters*. Modified *Section 5.5: Serial peripheral interfaces (SPI)*. Updated *Section 6: Electrical specifications*.
01-Feb-2011	5	Updated *Table 20: DC electrical characteristics*.
23-Mar-2012	6	Modified *Section 2.1: Receiver system overview on page 17*. Modified *Section 2.3: Dual channel HD 1.5 Radio processing on page 18*. Modified *Figure 7: Power on timing on page 22*. Modified *Section 4.1: Oscillator setting time on page 23*. Modified *Table 6: Baseband interfaces pin list on page 26*. Modified *Table 11: Host micro SPI pin list on page 31*. Modified *Section 5.6: I^2C interfaces on page 32*. Modified *Table 15: I2C1 interface device address on page 33*.
26-Nov-2012	7	Modified *Table 18: Absolute maximum ratings on page 36*. Modified *Table 19: Thermal data on page 36*. Modified *Table 20: DC electrical characteristics on page 37*.
17-Sep-2013	8	Updated disclaimer.
18-Dec-2013	9	Updated *Table 1: Device summary on page 1*.

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