STMPE1600

16-bit port expander with ultra-low power consumption Xpander Logic™

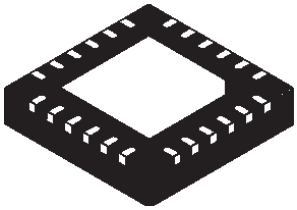
Datasheet –production data

Features

- 16 GPIOs which default to 16 inputs on power-up
- Serial I^2C interface (0 to 400 kHz) to the host with noise filter
- Operating voltage 1.65 V - 3.6 V
- I/O voltage 1.65 V - 3.6 V
- Interrupt output pin
- Internal power-on-reset
- Wakeup feature on each I/O
- Up to 8 devices sharing the same bus
- (3 address pins)
- 8 mA current drive/sink on each GPIO at 3.3 V
- < 1µA suspend current
- ESD protection exceeds 2 KV HBM per JESD22-A114
- Latch-up testing exceeding 100 mA
- Package: QFN24 (4 x 4 mm with 0.5 mm pitch)

Applications

- Portable media players
- Game consoles
- Mobile phones
- Smart phones



QFN24
(4 x 4 mm)

Description

The STMPE1600 is a GPIO (general purpose input/output) port expander able to interface a main digital ASIC via the two-line bidirectional bus (I2C). A separate GPIO expander IC is often used in mobile multimedia platforms to solve the problems of the limited amount of GPIOs typically available on the digital engine.

I/O expanders provide a simple solution when additional I/O are needed for several interface functions such as sensors, pushbuttons, LEDs, fans, etc.

The STMPE1600 offers great flexibility as each I/O can be configured as input or output. The device has been designed with very low quiescent current and includes a wakeup feature for each I/O, to optimize the power consumption of the device.

Table 1. Device summary

Order code	Package	Packing
STMPE1600QTR	QFN24	Tape and reel

This is information on a product in full production. www.st.com

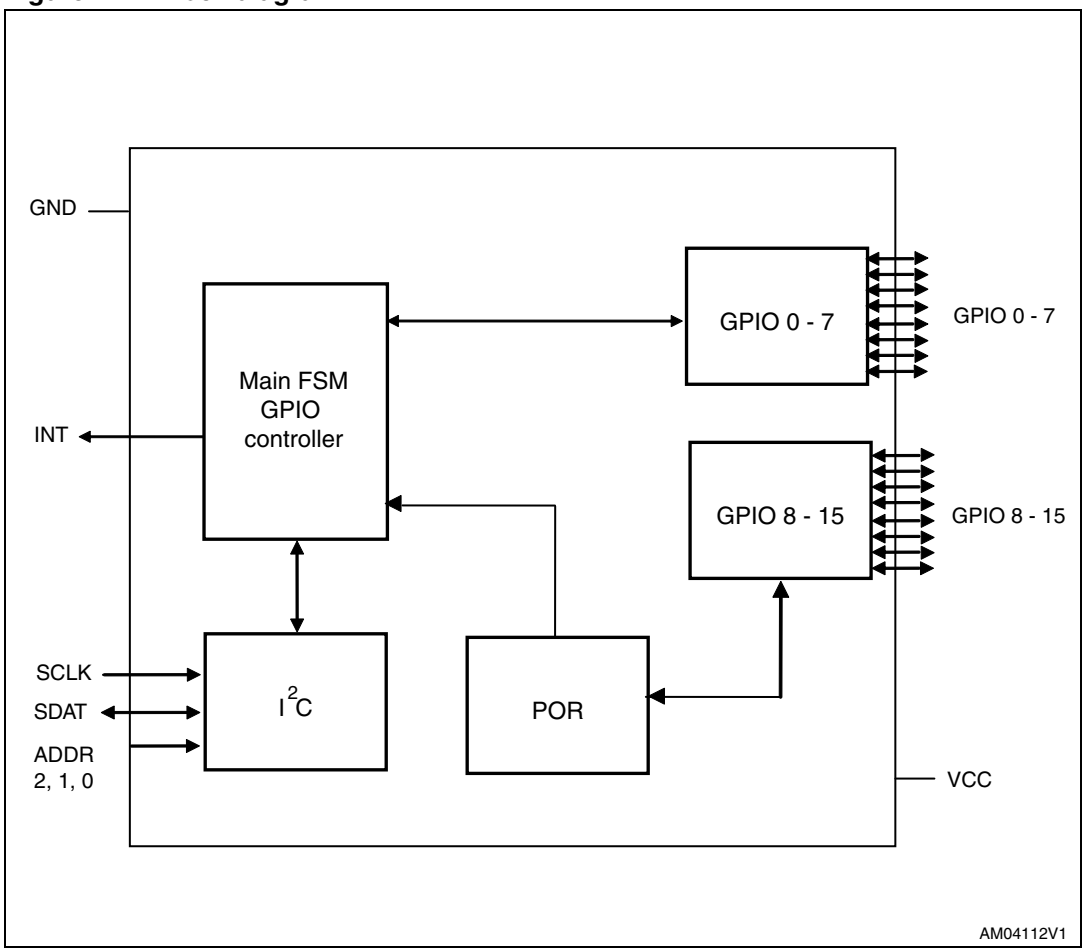
Contents

1 STMPE1600 functional overview

The STMPE1600 device consists of the following blocks:

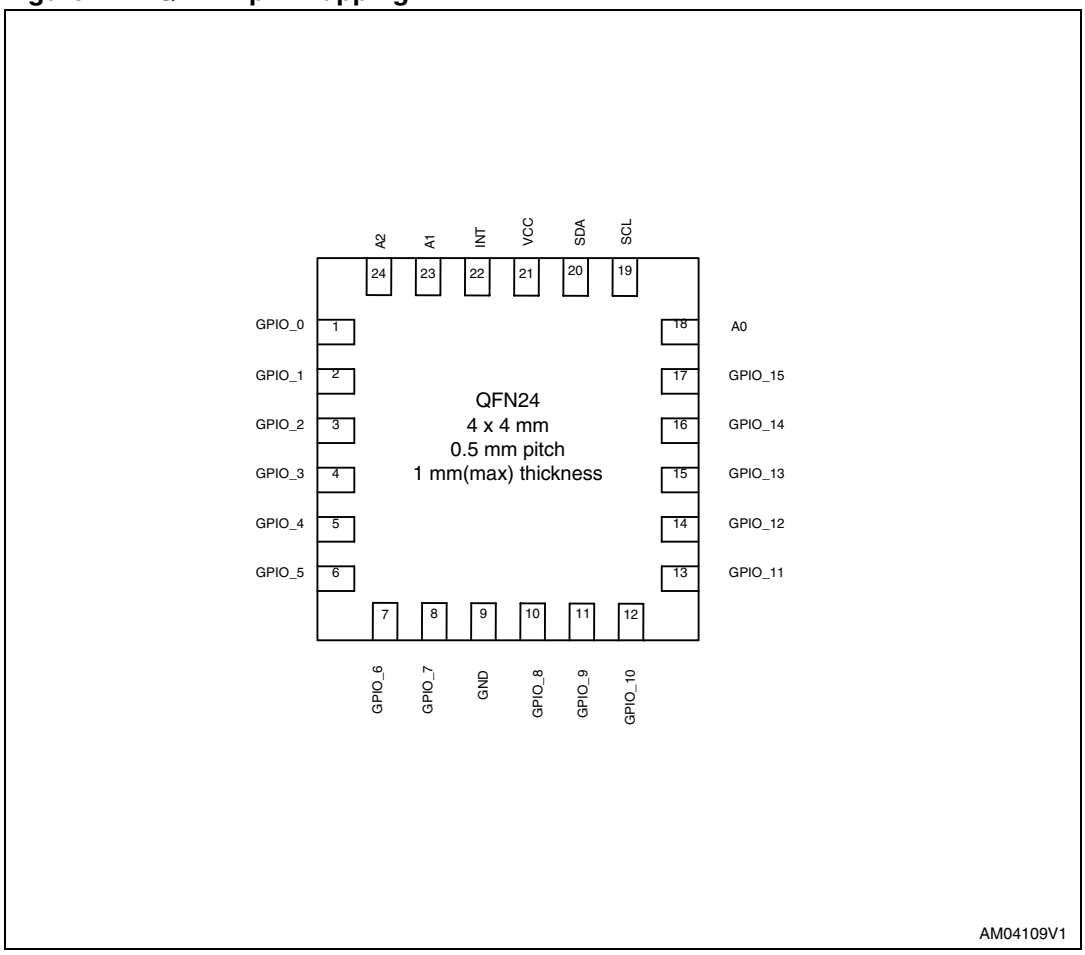
- Main FSM GPIO controller
- I^2C interface
- POR
- GPIOs

Figure 1. Block diagram



1.1 Pin assignment

Figure 2. QFN24 pin-mapping



1.2 Pin assignment (QFN24 package)

Table 2. Pin assignment

Pin number	Name	Type	Function
1	GPIO_0	IO	GPIO 0
2	GPIO_1	IO	GPIO 1
3	GPIO_2	IO	GPIO 2
4	GPIO_3	IO	GPIO 3
5	GPIO_4	IO	GPIO 4
6	GPIO_5	IO	GPIO 5
7	GPIO_6	IO	GPIO 6
8	GPIO_7	IO	GPIO 7
9	GND	-	Ground connection
10	GPIO_8	IO	GPIO 8
11	GPIO_9	IO	GPIO 9

Table 2. Pin assignment

Pin number	Name	Type	Function
12	GPIO_10	IO	GPIO 10
13	GPIO_11	IO	GPIO 11
14	GPIO_12	IO	GPIO 12
15	GPIO_13	IO	GPIO 13
16	GPIO_14	IO	GPIO 14
17	GPIO_15	IO	GPIO 15
18	A0	I	I^2C address 0. Up to 8 such devices can be addressed.
19	SCL	I	I^2C Clock. Fail-safe
20	SDA	IO	I^2C Data. Fail-safe
21	VCC	-	Power supply for I^2C and digital core and GPIOs
22	INT	O	Interrupt output pin. Fail-safe
23	A1	I	I^2C address 1. Up to 8 such devices can be addressed.
24	A2	I	I^2C address 2. Up to 8 such devices can be addressed.

2 I²C block

2.1 I²C module

The STMPE1600 is interfaced to the main processor using an I²C bus.

2.1.1 I²C address

The addressing scheme of STMPE1600 is designed to allow up to 8 devices to be connected to the same I²C bus. The slave device address is a 7-bit or 10-bit address where they are 42h, 43h, 44h, 45h, 46h, 47h, 48h and 49h (equivalent values in 7-bit and 10-bit addressing).

Figure 3. Addressing scheme

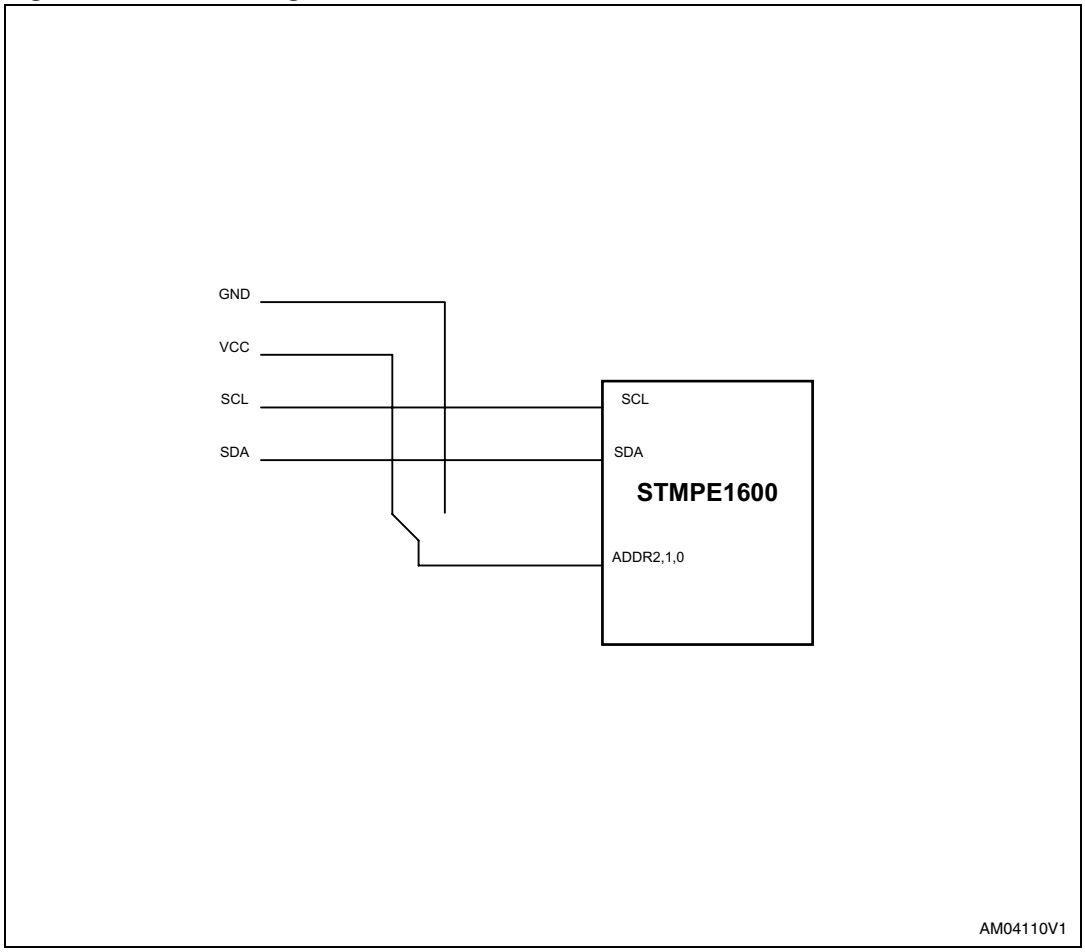


Table 3. Eight programmable slave addresses

A2	A1	A0	Slave device address (7-bit or 10-bit addressing)
0	0	0	42h
0	0	1	43h
0	1	0	44h
0	1	1	45h
1	0	1	46h
1	0	1	47h
1	1	0	48h
1	1	1	49h

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/Write bit (R/$\overline{W}$). The bit is set to 1 for Read and 0 for write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledge on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

Figure 4. I²C timing

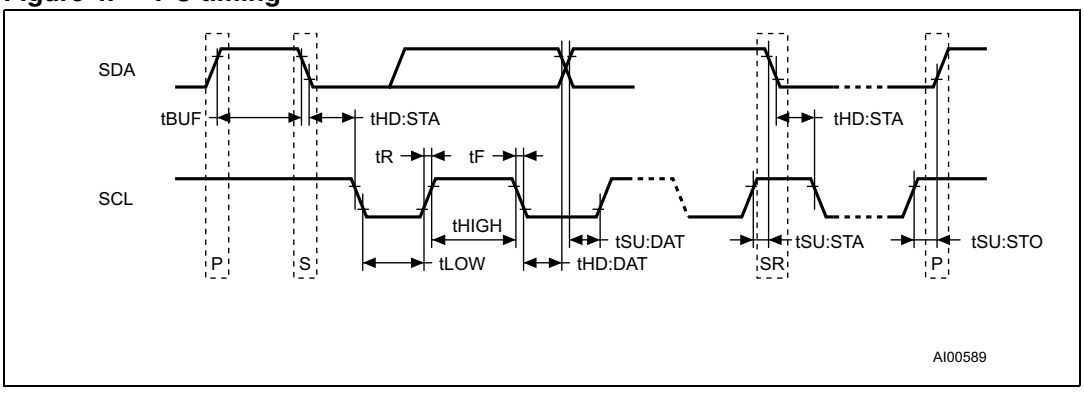


Table 4. I²C bus timing

Symbol	Parameter	Min	Typ	Max	Uni
f_{SCL}	SCL clock frequency	0	–	400	kHz
t_{LOW}	Clock low period	1.3	–	–	µs
t_{HIGH}	Clock high period	600	–	–	ns
t_F	SDA and SCL fall time	–	–	300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock is generated)	600	–	–	ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start period)	600	–	–	ns
$t_{SU:DAT}$	Data setup time	100	–	–	ns
$t_{HD:DAT}$	Data hold time	0	–	–	µs
$t_{SU:STO}$	STOP condition setup time	600	–	–	ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	–	–	µs

3 I²C features

The features that are supported by the I²C interface are as below:

- I²C slave device
- Operates from 1.65 V to 3.6 V
- Compliant to Philips I²C specification version 2.1
- Supports standard (up to 100Kbps) and fast (up to 400Kbps) modes
- 7-bit and 10-bit device addressing modes with up to 8 slave device addresses
- General call
- Start/Restart/Stop
- Address up to 8 STMPE1600 devices via I²C

Start condition

A Start condition is identified by a falling edge of SDA while SCL is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

Stop condition

A Stop condition is identified by a rising edge of SDA while SCL is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I2C transaction. A Stop condition at the end of a write command stops the write operation to registers.

Acknowledge bit

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDA after sending eight bits of data. During the ninth bit, the receiver pulls the SDA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDA in high state if it would to not acknowledge the receipt of the data.

Data input

The device samples the data input on SDA on the rising edge of the SCL. The SDA signal must be stable during the rising edge of SCL and the SDA signal must change only when SCL is driven low.

Figure 5. Read and write modes (random and sequential)

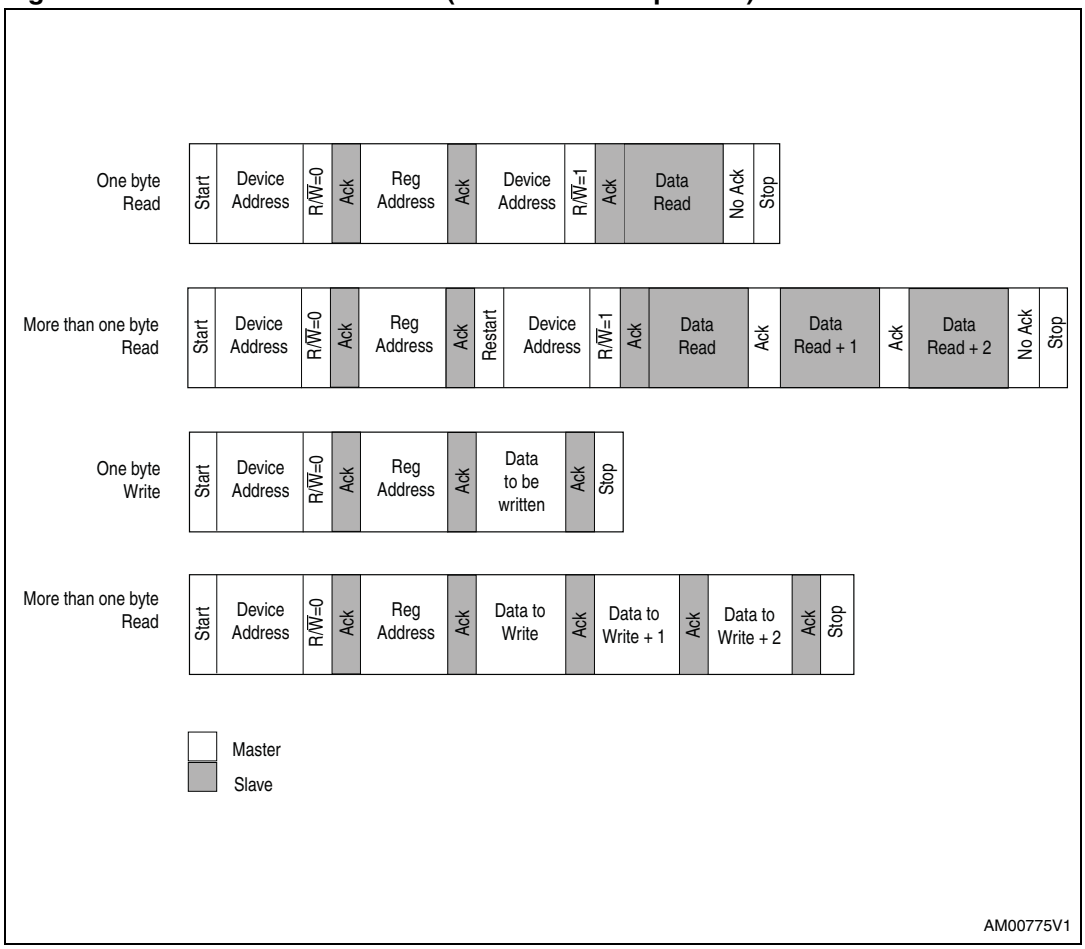


Table 5. Operating modes

Mode	Byte	Programming sequence
Read	≥1	Start, Device address, R/$\overline{W}$ = 0, Register address to be read
		Restart, Device address, R/$\overline{W}$ = 1, Data Read, Stop
		If no Stop is issued, the Data Read can be continuously performed. If the register address falls within the range that allows an address auto-increment, then the register address auto-increments internally after every byte of data being read.
Write	≥1	Start, Device address, R/$\overline{W}$ = 0, Register address to be written, Data Write, Stop
		If no Stop is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then the register address auto-increments internally after every byte of data being written in. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operation. Refer to the memory map table for the address ranges that are auto and non-increment.

Read operation

A write is first performed to load the register address into the Address Counter but without sending a Stop condition. Then, the bus master sends a reStart condition and repeats the Device Address with the R/W bit set to 1. The slave device acknowledges and outputs the content of the addressed byte. If no more data is to be read, the bus master must not acknowledge the byte and terminates the transfer with a Stop condition. If the bus master acknowledges the data byte, then it can continue to perform the data reading. To terminate the stream of data byte, the bus master must not acknowledge the last output byte and follow by a Stop condition. If the address of the register written into the Address Counter falls within the range of addresses that has the auto-increment function, the data being read will be coming from consecutive addresses, with the internal Address Counter automatically increments after each byte output. After the last memory address, the Address Counter 'rolls-over' and the device continue to output data from the memory address of 0x00. Similarly, for the address of register that falls within non-increment range of addresses, the output data byte comes from the same address (which is the address pointed by the Address Counter).

Acknowledgement in read operation

For the above read command, the slave device waits, after each byte read, for an acknowledgement during the ninth bit time. If the bus master does not drive the SDA to low state, then the slave device terminates and switches back to its idle mode, waiting for the next command.

Write operations

A write is first performed to load the register address into the Address Counter without sending a Stop condition. After the bus master receives an acknowledgement from the slave device, it may start to send a data byte to the register (pointed by the Address Counter). The slave device again acknowledges and the bus master terminates the transfer with a Stop condition. If the bus master would like to continue to write more data, it can just continue write operation without issuing the Stop condition. Whether the Address Counter auto increments or not after each data byte write, depends on the address of the register written into the Address Counter. After the bus master writes the last data byte and the slave device acknowledges the receipt of the last data, the bus master may terminate the write operation by sending a Stop condition. When the Address Counter reaches the last memory address, it 'rolls-over' on the next data byte write.

General call

A general call address is a transaction with the slave address of 0x00 and R/W = 0. When a general call address is made, the device responds to this transaction with an acknowledgement and behaves as a slave-receiver mode. The meaning of a general call address is defined in the second byte sent by the master-transmitter.

Table 6. General call

R/$\overline{W}$	Second Byte Value	Definition
0	0x06	2-byte transaction in which the second byte tells the slave device to reset and write (or latch in) the 1-bit programmable part of the slave address.
0	0x04	2-byte transaction in which the second byte tells the slave device not to reset and write (or latch in) the 1-bit programmable part of the slave address.
0	0x00	Not allowed as second byte.

Note: All other second byte values will be ignored.

3.1 Turning I^2C block OFF and ON

The STMPE1600 operates entirely on the I^2C clock. When there is no activity on the I^2C bus, current consumption of the device is extremely low. However, when there is activity on the I^2C bus, current consumption increases, even if the I^2C traffic is not directed to the assigned address.

The host system may choose to shut-down the I^2C block in the STMPE1600, if no access to the registers is required. This feature allows the current consumption to drop to the minimum. Host system turns OFF the I^2C block by writing '1' into the I2C_SHDN bit. The I2C block will shut down on the next valid clock edge of the I^2C clock signal. In this state, the device cannot be accessed by I^2C, as the I^2C has shut down completely.

To turn ON the I^2C block, system host must reset the STMPE1600 in order to re-activate the I^2C block either by removing V_{CC} and bringing it back again. Or by using GPIO_0 for wake-up function.

4 Register map

Table 7. Register map

Address	Register name	Size (bit)	Function
0x00	Chip ID LSB	8	0x00
0x01	Chip ID MSB	8	0x16
0x02	Version ID	8	Revision number (0x01)
0x03	SystemControl	8	Reset and interrupt control
0x04-0x07	Reserved		Reserved
0x08	IEGPIOR	8	GPIO interrupt enable register LSB
0x09		8	GPIO interrupt enable register MSB
0x0A	ISGPIOR	8	GPIO interrupt status register LSB
0x0B		8	GPIO interrupt status register MSB
0x10	GPMR	8	GPIO monitor pin state register LSB
0x11		8	GPIO monitor pin state register MSB
0x12	GPSR	8	GPIO set pin state register LSB
0x13		8	GPIO set pin state register MSB
0x14	GPDR	8	GPIO set pin direction register LSB
0x15		8	GPIO set pin direction register MSB
0x16	GPPIR	8	GPIO polarity inversion register LSB
0x17		8	GPIO polarity inversion register MSB
0x18-0xFF	Reserved		Reserved

5 System control register

SYS_CTRL System control register

7	6	5	4	3	2	1	0
SOFT RESET	I2C_SHDN	Wakeup_En	RESERVED	RESERVED	INT_Enable	RESERVED	INT_Polarity
RW	RW	RW	–	–	RW	–	RW

Address: 0x03

Type: RW

Reset: 0x00

Description: System control register.

[7] SOFT RESET:
Writing '1' to this bit causes a soft reset
Cleared by hardware.

[6] I2C_SHDN:
Writing '1' to this bit shuts down the I2C block on the next valid I2C clock.
In shut-down mode, only 2 possible ways exist to re-activate the device:
- Remove and reconnect Vcc
- Wake_up through the GPIO_0 pin if programmed as a hot-key and if Wakeup Enable bit of this register is enabled
All GPIO states remain the same on entering shut-down mode.

[5] Wakeup_En:
Wakeup Enable bit
'1' to enable GPIO_0 as clock gating signal during shutdown
'0' to disable the above

[4] RESERVED

[3] RESERVED

[2] INT_Enable:
'1' to enable interrupt output
'0' to disable interrupt output
When the interrupt output is disabled, it is in floating condition but it does not consume current

[1] RESERVED

[0] INT_Polarity:
Interrupt polarity
'1' for active High
'0' for active LOW

6 Interrupt system

The STMPE1600 can be configured to generate an interrupt when there is a logic transition on any of the GPIO configured as an input.

IEGPIOR Interrupt enable GPIO mask register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEG15	IEG14	IEG13	IEG12	IEG11	IEG10	IEG9	IEG8	IEG7	IEG6	IEG5	IEG4	IEG3	IEG2	IEG1	IEG0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0x08, 0x09

Type: RW

Reset: 0x00

Description: Interrupt enable GPIO mask register (IEGPIOR)

The IEGPIOR register is used to enable the interruption from a particular GPIO interrupt source to the host. The IEG[15:0] bits are the interrupt enable mask bits corresponding to the GPIO[15:0] pins.

[15:0] IEG[x]: Interrupt enable GPIO mask (where x = 15 to 0)
Writing a '1' to the IE[x] bit will enable the interruption to the host.

7 Interrupt status GPIO register (ISGPIOR)

ISGPIOR Interrupt status GPIO mask register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISG15	ISG14	ISG13	ISG12	ISG11	ISG10	ISG9	ISG8	ISG7	ISG6	ISG5	ISG4	ISG3	ISG2	ISG1	ISG0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0x0A, 0x0B

Type: RW

Reset: 0

Description: Interrupt status GPIO register (ISGPIOR)

The ISGPIOR register monitors the status of the interruption from a particular GPIO pin interrupt source to the host. Regardless of the IEGPIOR bits are enabled or not, the ISGPIOR bits are still updated. The ISG[15:0] bits are the interrupt status bits corresponding to the GPIO[15:0] pins.

[15:0] ISG[x]: Interrupt status GPIO (where x = 15 to 0)

Read:

Interrupt Status of the GPIO[x]. Reading the register will clear any bits that has been set to ‘1’

Write:

Writing to this register has no effects

8 GPIO controller

A total of 16 GPIOs are available in the STMPE1600 port expander IC. The GPIO controller contains the registers that allow the host system to configure each of the pins into either a GPIO (input or output), or into one of the alternate functions. Unused GPIOs should be configured as outputs to minimize the power consumption.

A group of registers are used to control the exact function of each of the 16 GPIOs. The registers and their respective address are listed in the following table.

Table 8. GPIO controller registers

Address	Register name	Description	Auto-increment (during sequential R/W)
0x10	GPMR	GPIO monitor pin state register	Yes
0x12	GPSR	GPIO set pin state register	Yes
0x14	GPDR	GPIO set pin direction register	Yes
0x16	GPPIR	GPIO polarity inversion register	Yes

Note: Once the last register address 0x16-0x17 location is accessed, the locations of 0x18 to 0xFF are reserved. After 0xFF location, the pointer rolls over to the 0x00 register address location.

All GPIO registers are named as GPxx, where:

xx represents the functional group.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO-15	IO-14	IO-13	IO-12	IO-11	IO-10	IO-9	IO-8	IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

The function of each bit is shown in the following table:

Table 9. GPIO bit function

Register name	Function
GPIO monitor pin state	Reading this bit yields the current state of the bit. Writing has no effect.
GPIO set pin state	Writing ‘1’ to this bit causes the corresponding GPIO to go to ‘1’ state. Writing ‘0’ to this bit causes the corresponding GPIO to go to ‘0’ state.
GPIO set pin direction	‘0’ sets the corresponding GPIO to input state, and ‘1’ sets it to output state. All bits are ‘0’ on reset.
GPIO polarity inversion	Writing a ‘1’ enables polarity inversion on the Input Port. Writing a ‘0’, the input port polarity is retained. The reset value is 0.

On power-up reset, all GPIOs are set as input.

9 Polarity inversion register

PINV **Polarity inversion register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PINV 15	PINV 14	PINV 13	PINV 12	PINV 11	PINV 10	PINV9	PINV8	PINV7	PINV6	PINV5	PINV4	PINV3	PINV2	PINV1	PINV0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: 0x16, 0x17

Type: RW

Reset: 0

Description: Polarity inversion register.

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the Input Port Data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input Port Data polarity is retained. This is for Active HIGH or Active LOW operation register. The polarity of the read register can be inverted with this register.

[15:0] PINV[x]: Polarity inversion register (where x = 15 to 0)

Writing a '1' to the PINV[x] bit will enable polarity inversion on the Input Port. Writing a '0', the input port polarity is retained. The reset value is 0.

9.1 Power supply

The STMPE1600 operates with a single power supply VCC that ranges from 1.65V to 3.6V. The GPIO remains valid until the V_{CC} is removed. When the V_{CC} is removed, the GPIO is reset.

9.2 Reset

The STMPE1600 is equipped with an internal POR circuit that holds the device in reset state, until the V_{CC} supply input is valid. The internal POR is tied to the V_{CC} supply pin.

In the duration when reset pin is asserted, all GPIO are reset and default to input states.

9.3 Fail safe conditions

The STMPE1600_IOs (SDA, SCL, INT, A2, A1, A0) are fail-safe IOs that support 4 mA current drive.

Table 10. Fail safe conditions

V_{CC} (core and IO supply)	Condition
Present	Normal operating condition
Absent	Complete power-down condition

Note that “present” state implies that the supply is present. The “absent” state implies that the power is lost (grounded) condition. In the fail-safe condition, the leakage current flowing into the STMPE1600 device is prevented.

Fail Safe condition

When chip supply is 0 V and when V_{IO} (SDA, SCL, INT, A2, A1, A0) is 3.6 V, this is classified as a fail-safe condition. In this case, the chip is protected and the current per I/O is limited to a very small value.

Overvoltage condition

The second condition is the overvoltage condition which occurs when V_{CC} = 1.65 V and V_{IO} = 3.6 V. In this condition, the current drawn by the device per IO can be 10 µA (typical) and 25 µA (worst case). This device should not be operated under this condition.

So it is recommended to operate the IO at the same voltage as the supply voltage (either 1.8 V or 3.3 V). Also the fail safe IOs are special IOs which can have a voltage present while the supply voltage V_{CC} is 0 V. Current will be limited from the fail safe IOs when supply voltage V_{CC} is 0 V.

10 Maximum rating

Stressing the device above the ratings listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device’s reliability.

Table 11. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5	V
V_{IO}	GPIO supply voltage	4.5	V
V_{ESD}	ESD protection on each GPIO pin (HBM)	2	kV

Table 12. Thermal data

Symbol	Parameter	Value	Unit
$Ø_{JA}$	Thermal resistance junction-ambient	TBD	°C/W
T_{OPR}	Operating temperatire	-40 to 85	°C
T_J	Storage temperature	-65 to 155	°C

10.1 DC electrical characteristics

Table 13. Supplies

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{CC}	Core supply voltage		1.65	–	3.6	V
Icc_{400kHz}	Operating current with I^2C CLK = 400 kHz with full traffic density	SCL_running at 400 kHz V_{CC} = 1.8 - 3.3 V 100% traffic density I/O = inputs No peripheral activity or no load	–	200	500	µA
Icc_{100kHz}	Operating current with I^2C CLK = 100 kHz with full traffic density	SCL running at 100 kHz V_{CC} = 1.8 - 3.3 V 100% traffic density I/O=inputs No peripheral activity or no load	–	135	200	µA

Table 13. Supplies (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$Icc_{(normal)}$	Normal mode operating current	SCL running at 400KHz Vcc=1.8-3.3V 1% traffic density No peripheral activity or no load	–	10	15	µA
$Icc_{(suspend)}$	Standby operating current	No I^2C activity (SCL=0kHz) V_{CC} = 1.8 - 3.3 V V_{inputs}=GND or V_{CC} No peripheral activity or no load I/O=inputs	–	0.25	1	µA
$Icc_{(powerdown)}$	Power down current	I^2C block OFF V_{CC} =1.8 - 3.3 V	–	0.25	1	µA
$I_{IO(fail\ safe)}$	Fail-safe IO current	V_{CC}=0 V Vio (fail safe)= 3.6 V	–	0.25	1	µA

Table 14. Input/outputs

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{IL}	Input voltage low state	V_{CC} = 1.65 - 3.6 V	–	–	0.2Vcc	V
V_{IH}	Input voltage high state	V_{CC} = 1.65 - 3.6 V	0.8Vcc	–	–	V
V_{hyst}	Schmitt trigger hysteresis			0.2	–	V
I_{IL}	Input low leakage current	V_I = GND	–	–	1	µA
I_{IH}	Input high leakage current	V_I = V_{CC}	–	–	-1	µA
V_{OL}	Output voltage low state	V_{CC} = 1.65 - 3.6 V, I_{OL}= 8 mA	–	–	0.15Vcc	V
V_{OH}	Output voltage high state	V_{CC} = 1.65 - 3.6 V, I_{OL} = 8 mA	0.85Vcc	–	–	V

Table 15. Digital inputs (A2, A1, A0 pins)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{IL}	Low-level input voltage		–	–	0.2Vcc	V
V_{IH}	High-level input voltage		0.8Vcc	–	–	V
I_L	Leakage current	$V_I = V_{CC}$ or GND	-1	–	1	µA

Table 16. Interrupt (INT pin)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
I_{OL}	Open-drain low-level output current	V_{OL}= 0.4 V	–	4	–	mA
V_{OL}	Output voltage low state	V_{CC} = 1.8 - 3.3 V, I_{OL}= 4 mA	–	–	0.15Vcc	V
V_{OH}	Output voltage high state	V_{CC} = 1.8 - 3.3 V, I_{OL}= 4 mA	0.85Vcc	–	–	V

Table 17. Input (SCL), Input/Output (SDA)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{IL}	Low-level input voltage		–	–	0.2Vcc	V
V_{IH}	High-level input voltage		0.8Vcc	–	–	V
I_L	Leakage current	$V_I = V_{CC}$ or GND	-1	–	1	µA
V_{OL} (I^2C)	Output voltage low state	V_{CC} = 1.8 - 3.3 V, I_{OL}= 4 mA	–	–	0.15Vcc	V
V_{OH} (I^2C)	Output voltage high state	V_{CC} = 1.8 - 3.3 V, I_{OL}=4 mA	0.85Vcc	–	–	V

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 6. Package outline for QFN24 (4 x 4 x 1 mm) - 0.5 mm pitch

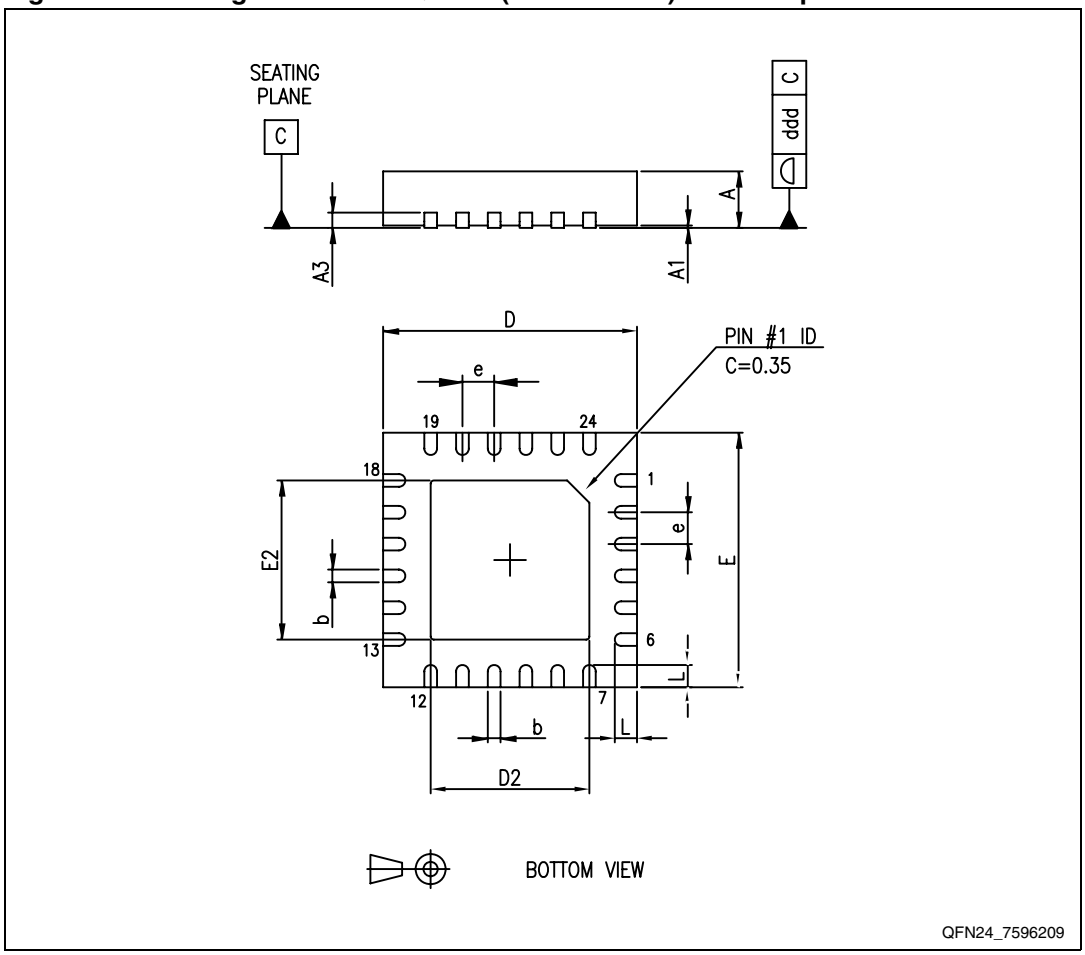
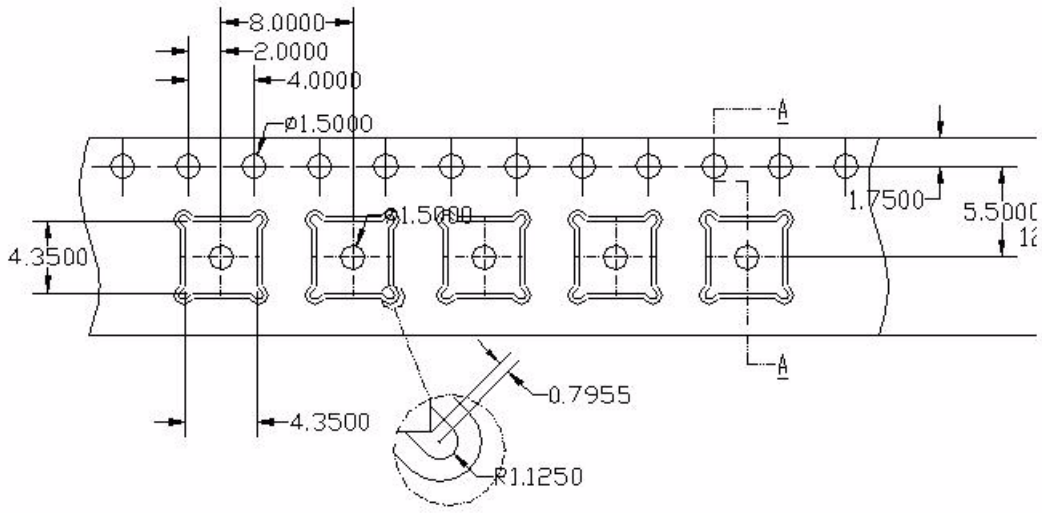


Table 18. Package mechanical data for QFN24 (4 x 4 x 1 mm) - 0.5 mm pitch

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	–	0.20	–
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.40	2.50	2.60
E	3.85	4.00	4.15
E2	2.40	2.50	2.60
e	–	0.50	–
L	0.30	0.40	0.50
ddd	–	–	0.08

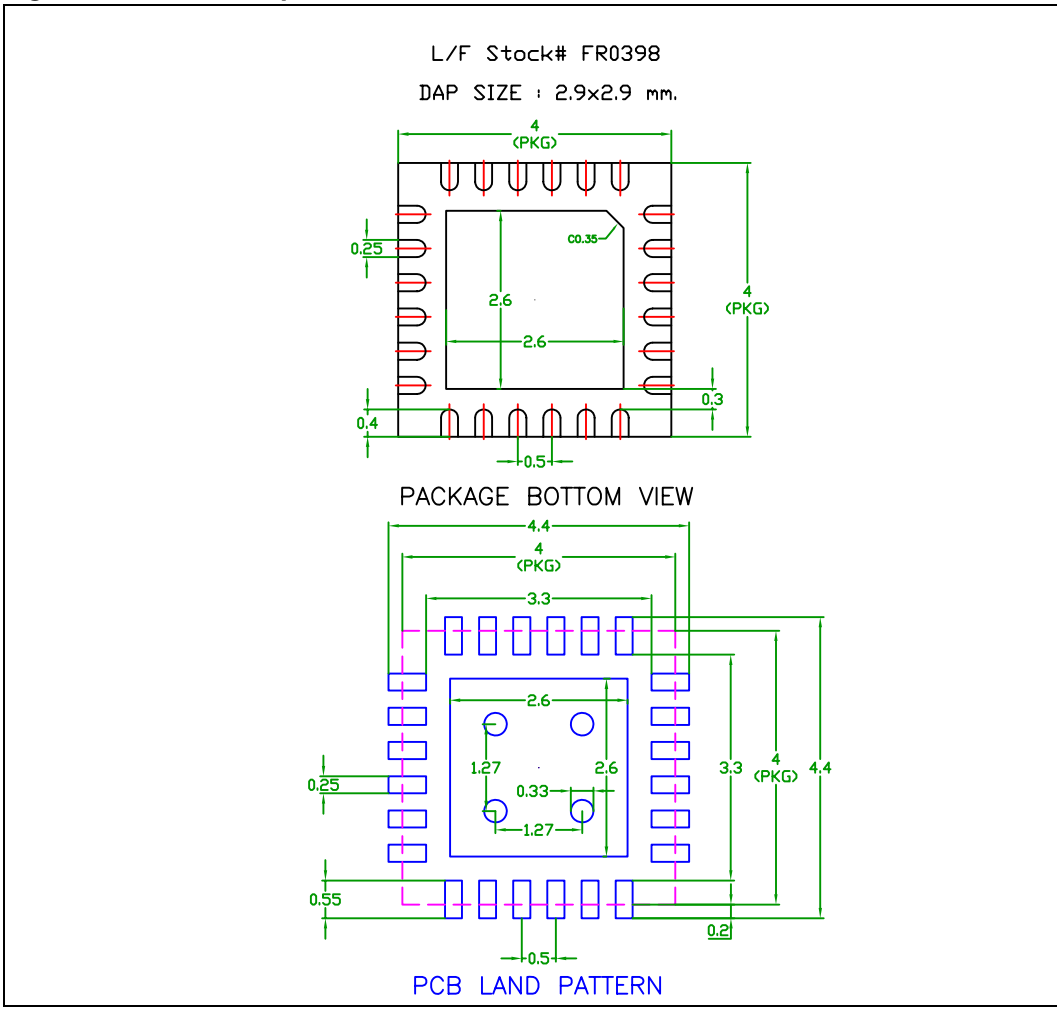
Figure 7. STMPE1600 top side marking information

Figure 8. Carrier tape and reel info



Reel size is 13-inch with 4000 units per reel.

Figure 9. PCB land pattern



12 Revision history

Table 19. Document revision history

Date	Revision	Changes
26-Mar-2010	1	Initial release.
08-Jan-2013	2	Document status has been promoted from “Preliminary data” to “Datasheet”.
05-Feb-2013	3	Updated *Figure 7*.

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